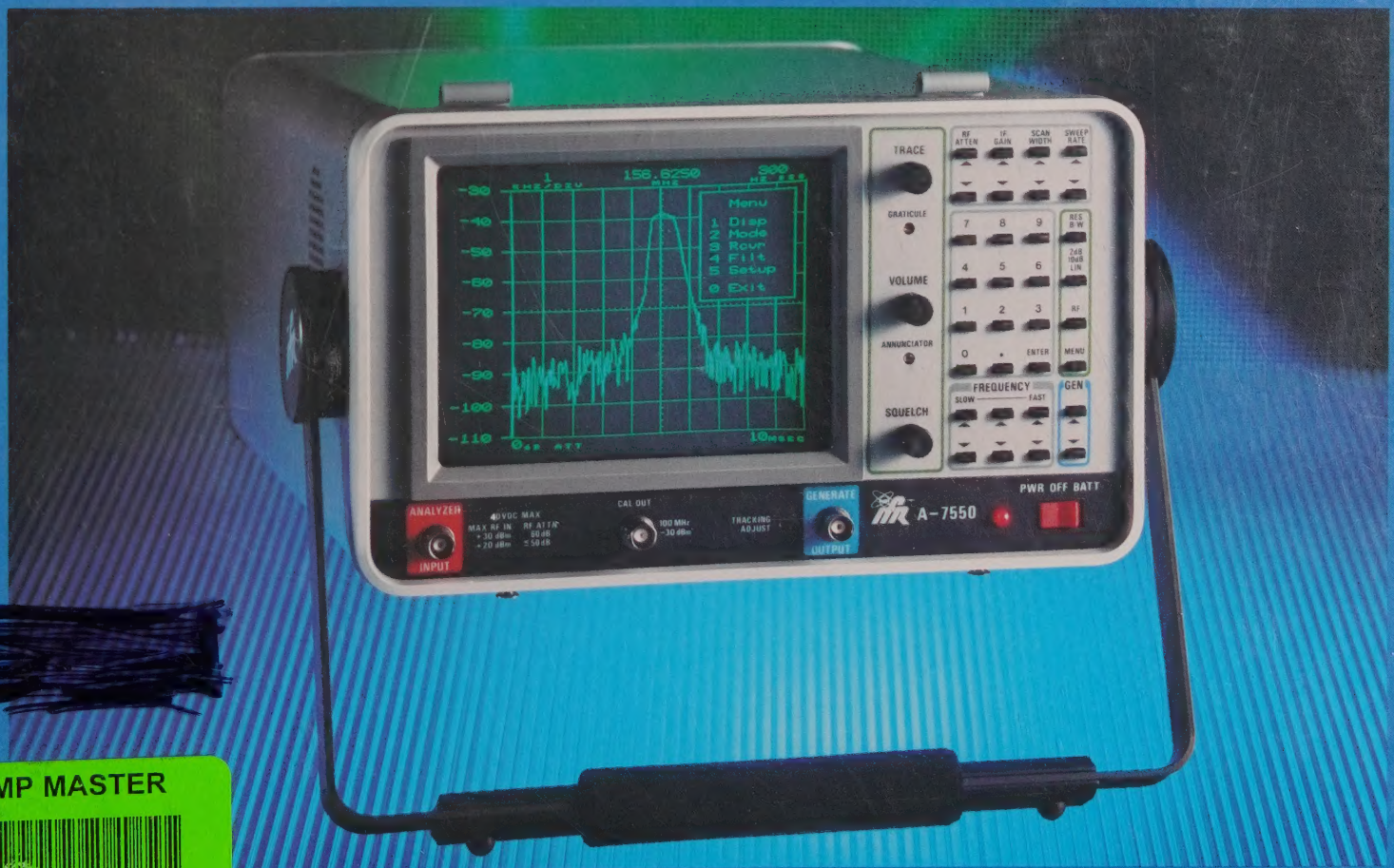
MAINTENANCE MANUAL

ifr INC

A-7550
SPECTRUM ANALYZER



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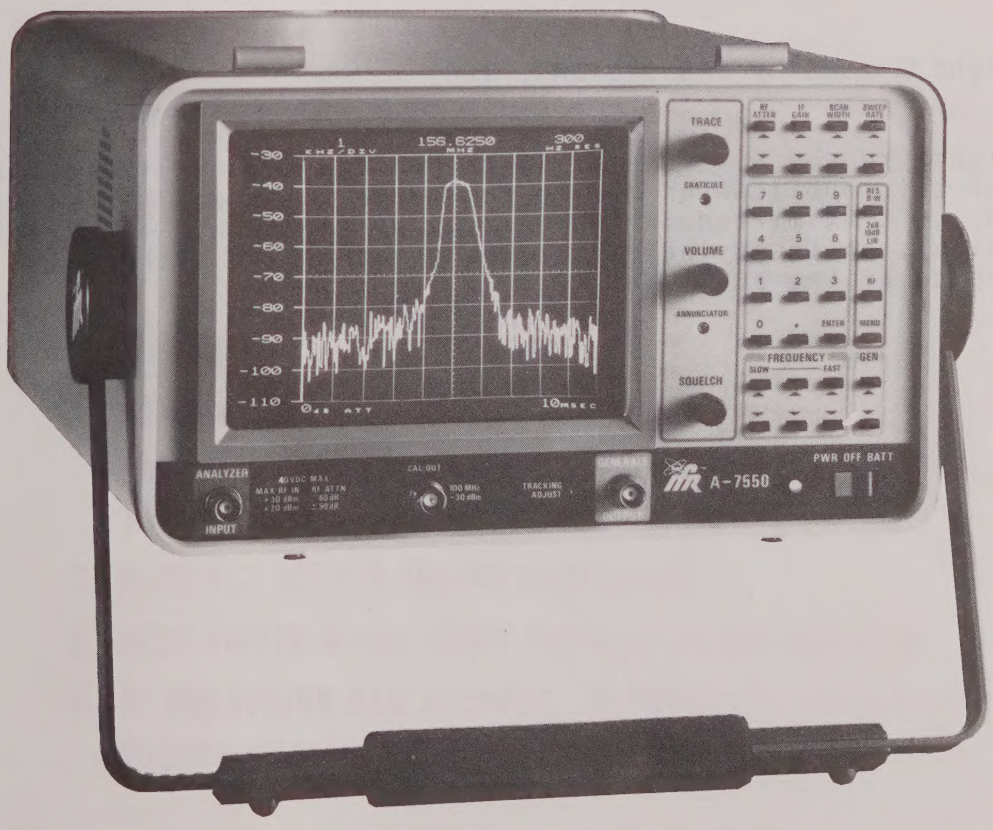
MAINTENANCE MANUAL

A-7550
SPECTRUM ANALYZER



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WARNING:

HIGH VOLTAGE EQUIPMENT

THIS EQUIPMENT CONTAINS CERTAIN CIRCUITS AND/OR COMPONENTS OF EXTREMELY HIGH VOLTAGE POTENTIALS, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. WHEN PERFORMING ANY OF THE PROCEDURES CONTAINED IN THIS MANUAL, HEED ALL APPLICABLE SAFETY PRECAUTIONS.

RESCUE OF SHOCK VICTIMS

1. DO NOT ATTEMPT TO PULL OR GRAB THE VICTIM
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER.
3. IF YOU CANNOT TURN OFF ELECTRICAL POWER, PUSH, PULL OR LIFT THE VICTIM TO SAFETY USING A WOODEN POLE, A ROPE OR SOME OTHER DRY INSULATING MATERIAL.

FIRST AID

1. AS SOON AS VICTIM IS FREE OF CONTACT WITH SOURCE OF ELECTRICAL SHOCK, MOVE VICTIM A SHORT DISTANCE AWAY FROM SHOCK HAZARD.
2. SEND FOR DOCTOR AND/OR AMBULANCE.
3. KEEP VICTIM WARM, QUIET AND FLAT ON HIS/HER BACK.
4. IF BREATHING HAS STOPPED , ADMINISTER ARTIFICIAL RESUSCITATION. STOP ALL SERIOUS BLEEDING.

CAUTION

INTEGRATED CIRCUITS AND SOLID STATE DEVICES SUCH AS MOS FETs, ESPECIALLY CMOS TYPES, ARE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGES RECEIVED FROM IMPROPER HANDLING, THE USE OF UNDERGROUND TOOLS, AND IMPROPER STORAGE AND PACKAGING. ANY MAINTENANCE TO THIS UNIT MUST BE PERFORMED WITH THE FOLLOWING PRECAUTIONS:

1. BEFORE USE IN A CIRCUIT, KEEP ALL LEADS SHORTED TOGETHER EITHER BY THE USE OF VENDOR-SUPPLIED SHORTING SPRINGS OR BY INSERTING LEADS INTO A CONDUCTIVE MATERIAL.

2. WHEN REMOVING DEVICES FROM THEIR CONTAINERS, GROUND THE HAND BEING USED WITH A CONDUCTIVE WRISTBAND.

3. TIPS OF SOLDERING IRONS AND/OR ANY TOOLS USED MUST BE GROUNDED.

4. DEVICES MUST NEVER BE INSERTED INTO OR REMOVED FROM CIRCUITS WITH POWER ON.

5. PC BOARD, WHEN TAKEN OUT OF THE SET, MUST BE LAID ON A GROUNDED CONDUCTIVE MAT OR STORED IN A CONDUCTIVE STORAGE BAG.

NOTE

Remove any built-in power source, such as a battery, before laying PC Boards on conductive mat or storing in conductive bag.

6. PC BOARDS, IF BEING SHIPPED TO THE FACTORY FOR REPAIR, MUST BE PACKAGED IN A CONDUCTIVE BAG AND PLACED IN A WELL-CUSHIONED SHIPPING BOX.

THE USE OF SIGNAL GENERATORS FOR MAINTENANCE AND OTHER ACTIVITIES CAN BE A SOURCE OF ELECTROMAGNETIC INTERFERENCE TO COMMUNICATION RECEIVERS, WHICH CAN CAUSE DISRUPTION AND INTERFERENCE TO COMMUNICATION SERVICE OUT TO A DISTANCE OF SEVERAL MILES.

USERS OF THIS EQUIPMENT SHOULD SCRUTINIZE ANY OPERATION WHICH RESULTS IN RADIATION OF A SIGNAL (DIRECTLY OR INDIRECTLY) AND SHOULD TAKE NECESSARY PRECAUTIONS TO AVOID POTENTIAL COMMUNICATION INTERFERENCE PROBLEMS.

LIST OF EFFECTIVE PAGES

The manual pages listed below which are affected by a current change or revision, are so identified by a revision number and an asterisk.

Date of issue for original and changed pages are:

Original ..... 0 ..... October 1, 1988

TOTAL NUMBER OF PAGES IN THIS MANUAL IS 266 CONSISTING OF FOLLOWING:

Page No.	Change No.
Title Page	0
Copyright Page	0
Warning Page	0
Caution Page	0
A	0
B Blank	0
i thru ix	0
x Blank	0
1-1 thru 1-5	0
1-6 Blank	0
2-1 thru 2-50	0
3-1 thru 3-5	0
3-6 Blank	0
3-7 thru 3-37	0
3-38 Blank	0
4-1 thru 4-2	0
4-3 Blank	0
4-4 thru 4-17	0
4-18 Blank	0
Template Page	0
4-19 thru 4-67	0
4-68 Blank	0
5-1 thru 5-55	0
5-56 Blank	0
A-1 thru A-4	0
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C-1 thru C-3	0
C-4 Blank	0
D-1 thru D-3	0
D-4 Blank	0
D-5 thru D-6	0
E-1 thru E-4	0
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G-1 thru G-4	0
H-1 thru H-2	0

PREFACE

SCOPE

This manual contains maintenance instructions for the A-7550 Spectrum Analyzer for units with Serial Numbers 2400 and beyond (i.e., software versions 2.0/3.0 and up). The information in this manual enables the technicians to:

A. Service, test, repair or replace any major assembly or module within the set.

B. Maintain the operating condition of the set to expected performance standards.

C. Understand the principles of operation as they relate to the overall operation of the set as well as to understand individual circuits.

ORGANIZATION

This manual is divided into five major sections and eight appendices.

SECTION 1 - INTRODUCTION

Briefly describes the electrical and mechanical configuration of the A-7550 Spectrum Analyzer, intended to familiarize the technician with the overall structure of the set.

SECTION 2 - THEORY OF OPERATION

Describes the A-7550 Spectrum Analyzer circuit theory at three levels of complexity: a simplified overview, a functional theory of interactive modules, and a detailed theory of each module. Appropriate block diagrams accompany each discussion.

SECTION 3 - PERFORMANCE EVALUATION

Contains "covers on" functional checkout procedures for evaluating the performance of the A-7550 Spectrum Analyzer. Each mode of operation and major function is checked in these procedures.

SECTION 4 - CALIBRATION

Contains step-by-step calibration procedures for use at normal calibration intervals or for making repairs and module replacements.

SECTION 5 - MECHANICAL ASSEMBLIES, PC BOARDS & SCHEMATICS

Contains component layout drawings for all mechanical assemblies, PC board assemblies, interconnect diagrams, circuit schematics, waveforms and other miscellaneous data needed to repair the A-7550 Spectrum Analyzer.

APPENDICES

Contains useful supplementary information for the care, maintenance and operation of the A-7550 Spectrum Analyzer, including Specifications, supplementary equipment requirements, charts, shipping instructions and a list of abbreviations used in the manual.

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TABLE OF CONTENTS

Paragraph	Title	Page
	Preface	i
	Table of Contents	iii
	List of Illustrations	vi
	List of Tables	ix
	SECTION 1 - INTRODUCTION	
1-1	General	1-1
1-2	Electrical Description	1-1
1-3	Mechanical Description	1-2
	SECTION 2 - THEORY OF OPERATION	
2-1	General	2-1
2-2	System Theory of Operation	2-3
2-3	Functional Theory of Operation	2-5
2-3-1	Receiver Section Operation	2-5
2-3-2	Video Processor Operation	2-6
2-3-3	Control Processor Operation	2-7
2-3-4	Frequency Synthesis Operation	2-8
2-3-5	Frequency Calculations	2-8
2-3-6	Generator Section Operation	2-11
2-4	Detailed Theory of Operation	2-12
2-4-1	Power Supply	2-12
2-4-2	Input (0 to 60 dB) Attenuator	2-15
2-4-3	Receive IF	2-16
2-4-4	Analyzer IF	2-18
2-4-5	Analyzer Log Amp	2-19
2-4-6	Quasi-peak	2-23
2-4-7	10.7 MHz Receiver	2-26
2-4-8	Sweep Digitizer	2-29
2-4-9	Video Processor	2-31
2-4-10	Control Processor	2-33
2-4-11	General Purpose Interface Bus (GPIB)	2-35
2-4-12	RS-232C Interface PC Board	2-36
2-4-13	Interface PC Board	2-36
2-4-14	Reference Oscillator	2-38
2-4-15	1st LO Sampling Loop	2-39
2-4-16	1350-2350 MHz VCO	2-42
2-4-17	Synthesizer #1	2-43
2-4-18	Synthesizer #2	2-45
2-4-19	2nd LO Summing Loop	2-47
2-4-20	Tracking Generator	2-48

Paragraph	Title	Page
	SECTION 3 - PERFORMANCE EVALUATION	
3-1	General	3-1
3-1-1	Test Equipment Requirements	3-2
3-1-2	Corrective Maintenance Procedures	3-2
3-2	Performance Evaluation Procedures	3-7
3-2-1	Initial Setup and Self-Test	3-7
3-2-2	Cal Out Performance Evaluation	3-8
3-2-3	Frequency Display Linearity and Readout Accuracy Performance Evaluation	3-11
3-2-4	Noise Sidebands Performance Evaluation	3-13
3-2-5	Amplitude Scale Linearity Performance Evaluation	3-15
3-2-6	Frequency Response Performance Evaluation	3-19
3-2-7	Resolution Bandwidth Accuracy Performance Evaluation	3-21
3-2-8	Variance Between Bandwidth Filters Performance Evaluation	3-23
3-2-9	IF Gain Performance Evaluation	3-25
3-2-1	RF Attenuator Performance Evaluation	3-28
3-2-11	10.7 MHz Receiver Performance Evaluation	3-31
3-2-12	Tracking Generator and Output Attenuator Performance Evaluation	3-34
	SECTION 4 - CALIBRATION	
4-1	General	4-1
4-1-1	Safety Precautions	4-1
4-1-2	Calibration Equipment Requirements	4-2
4-1-3	Disassembly Requirements	4-2
4-2	Power Supply Calibration	4-11
4-3	Display Calibration	4-15
4-4	CRT Calibration	4-17
4-5	Reference Oscillator Calibration	4-23
4-6	RF Control Calibration	4-25
4-7	Amplitude Calibration	4-29
4-8	10.7 MHz Receiver Calibration	4-38
4-9	Tracking Generator Calibration	4-41
4-10	Quasi-peak Filter Calibration	4-44
4-10-1	Headroom Measurement	4-44
4-10-2	Filter Check	4-46
4-10-3	Pulse Measurements	4-51
4-10-4	Filter Tests	4-62
4-10-5	Impulse Tests	4-64

Paragraph	Title	Page
SECTION 5 - ASSEMBLIES, PC BOARDS & SCHEMATICS		
5-1	General	5-1
5-2	How To Use Schematics	5-1
5-2-1	Coaxial Cables	5-1
5-2-2	Multiple Pin Connectors	5-1
5-3	Alphabetical Index of Technical Drawings	5-2
APPENDICES		
Appendix A	A-7550 Performance Specifications	A-1
Appendix B	Test Equipment Requirements	B-1
Appendix C	Preventive Maintenance Recommendations	C-1
Appendix D	Special Accessory Test Equipment	D-1
Appendix E	Abbreviations and Reference Designators	E-1
Appendix F	dBm to Microvolt Conversion Chart	F-1
Appendix G	A-7550 Spectrum Analyzer Accessory Items	G-1
Appendix H	Repacking For Shipment	H-1

LIST OF ILLUSTRATIONS

Figure No.	Title	Page
1-1	A-7550 Composite Assembly w/Module Identification ..	1-3
1-2	A-7550 Controls, Connectors & Indicators	1-5
2-1	A-7550 System Block Diagram	2-2
2-2	Receiver Group Block Diagram	2-5
2-3	Video Processor Funcational Block Diagram	2-6
2-4	Control Processor Functional Block Diagram	2-7
2-5	Frequency Synthesis Functional Block Diagram	2-8
2-6	Generator Functional Block Diagram	2-11
2-7	Power Supply Block Diagram	2-12
2-8	Receive IF Block Diagram	2-16
2-9	Analyzer IF Block Diagram	2-18
2-10	Log Amp Block Diagram	2-20
2-11	Quasi-peak Filter Block Diagram	2-23
2-12	Quasi-peak Detector Block Diagram	2-24
2-13	10.7 MHz Receiver Block Diagram	2-26
2-14	Sweep Digitizer Block Diagram	2-29
2-15	Video Processor Block Diagram	2-31
2-16	Control Processor Block Diagram	2-33
2-17	GPIB Block Diagram	2-35
2-18	RS-232C Interface Block Diagram	2-36
2-19	Interface PC Board Block	2-37
2-20	Reference Oscillator Block Diagram	2-38
2-21	1st LO Sampler Loop Block Diagram	2-40
2-22	1350-2350 MHz VCO Block Diagram	2-42
2-23	Synthesizer #1 Block Diagram	2-43
2-24	Synthesizer #2 Block Diagram	2-45
2-25	2nd LO Summing Loop Block Diagram	2-47
2-26	Tracking Generator Block Diagram	2-48
3-1	Cal Out Test Setup	3-8
3-2	Amplitude Scale Linearity Test Setup	3-15
3-3	Frequency Response Test Setup	3-19
3-4	IF Gain Test Setup	3-25
3-5	RF Attenuator Test Setup	3-28
3-6	Tracking Generator/Output Attenuator Test Setup	3-34

Figure No.	Title	Page
4-1	Power Supply Calibration Test Setup	4-11
4-2	CRT Calibration Test Setup	4-17
4-3	Overlay for CRT Calibration	4-18
4-4	Trapezoidal Adjustments	4-21
4-5	Partial View of CRT Neck/Deflection Yoke	4-21
4-6	Pincushion/Barrel Adjustments	4-22
4-7	Reference Oscillator Calibration test Setup	4-23
4-8	RF Control Calibration Test Setup	4-25
4-9	Amplitude Calibration Test Setup	4-29
4-10	10.7 MHz Receiver Calibration Test Setup	4-38
4-11	Tracking Generator Calibration Test Setup	4-41
4-12	Headroom Test Setup	4-45
4-13	Filter Test Setup	4-46
4-14	200 Hz Bandwidth Filter Shape	4-48
4-15	9 kHz Filter Limits (9 kHz from Mid-band)	4-49
4-16	120 kHz Filter Limits (120 kHz from Mid-band)	4-50
4-17	Quasi-peak Test Setup	4-52
4-18	Pulse Spectrum	4-54
4-19	δf_3 Zero Crossing	4-54
4-20	δf_2 Zero Crossing	4-57
4-21	δf_1 Zero Crossing	4-60
4-22	Impulse Test Setup	4-64
4-23	Composite and Adjustments	4-69
5-1	Interconnect w/Block Diagram and Coax Running List	5-4
5-2	A-7550 Power Supply Assembly	5-6
5-3	RF Motherboard with Wire Harness Assembly	5-8
5-4	Front Panel & Keyboard Assembly	5-10
5-5	Fan Assembly	5-12
5-6	0-60 dB Attenuator Assembly	5-13
5-7	Receive IF Assembly	5-14
5-8	Analyzer IF Assembly	5-16
5-9	Quasi-peak Assembly	5-18
5-10	10.7 MHz (FM/AM/SSB) Receiver Assembly	5-20
5-11	Analyzer Log Amp Assembly	5-22
5-12	Battery Assembly	5-24
5-13	Digital Motherboard PC Board Assembly	5-25
5-14	Sweep Digitizer PC Board Assembly	5-26
5-15	Video Processor PC Board Assembly	5-28
5-16	Processor PC Board Assembly	5-30
5-17	Interface PC Board Assembly	5-32
5-18	GPIB PC Board Assembly	5-34
5-19	RS-232C PC Board Assembly	5-35
5-20	Reference Oscillator Assembly	5-36
5-21	1380-2350 MHz VCO Filter PC Board Assembly	5-37

Figure No.	Title	Page
5-22	1st LO Sampling Loop Assembly	5-38
5-23	1350-2350 MHz VCO Assembly	5-40
5-24	+20 dB External Amplifier Assembly	5-41
5-25	Synthesizer #1 Assembly	5-42
5-26	Synthesizer #2 Assembly	5-44
5-27	2nd LO Sampling Loop Assembly	5-46
5-28	Tracking Generator Installation	5-48
5-29	CRT Display Assembly	5-54
D-1	Circuit Schematic and Diagram of Battery Load Simulator	D-1
D-2	TF-30 Tune Fixture Assembly	D-2
D-3	20 dB Test Point	D-5
D-4	Filter Enclosure	D-6
D-5	150 kHz Low-pass Filter	D-6
D-6	30 MHz Low-pass Filter	D-6
D-7	30 MHz High-pass Filter	D-6
G-1	75 Ohm Adapter (BNC-to-BNC)	G-1
G-2	75 Ohm Adapter (BNC-to-Female)	G-1
G-3	Maintenance Kit	G-2
G-4	Camera Mount	G-3
G-5	Soft Padded Carrying Case	G-4
H-1	Shippable A-7550 Spectrum Analyzer	H-2

LIST OF TABLES

Table No.	Title	Page
1-1	A-7550 Major Electrical Circuits	1-1
1-2	A-7550 Mechanical Groups	1-2
2-1	A-7550 Spectrum Analyzer Options	2-4
2-2	Synthesizer #2 Frequency Calibration	2-9
2-3	Summing Oscillator Frequency Calculation	2-10
2-4	A-7550 Frequency Calculations	2-10
2-5	Relationship of Bit Selection to Time Constant Variables	2-24
3-1	A-7550 Performance Evaluation Record	3-3
3-2	Parameters for Resolution Bandwidth Performance Evaluation	3-22
3-3	Scan Width Settings for Bandwidth Selections	3-24
3-4	Selectivity Settings	3-33
4-1	Module Replacement and Calibration Requirements	4-4
4-2	A-7550 Calibration Record	4-5
4-3	IF Gain Linearity	4-34
4-4	RF Attenuation Linearity	4-34
4-5	Quasi-peak Amplitude Pulse	4-51

SECTION 1 - INTRODUCTION

1-1 GENERAL

This section illustrates the internal electrical and mechanical configurations of the A-7550 Spectrum Analyzer for units with Firmware Versions 2.0 and Later (Serial Numbers 2400 and On). Exploded composite drawings (Figure 1-1) show the A-7550 Spectrum Analyzer in two views. The first view shows a standard unit (no options installed). The second view shows a unit with all allowable options installed. Figure 1-2 gives the location of the A-7550 controls, connectors and indicators on the front and back panels.

1-2 ELECTRICAL DESCRIPTION

The A-7550 Spectrum Analyzer is microprocessor controlled. It is digitally synthesized and is capable of displaying signals of interest from 100 kHz to approximately 1 GHz, at an input level up to +30 dBm. Table 1-1 lists A-7550 modules included with each major circuit.

Power Distribution	Receiver
Power Supply	0-60 dB Attenuator
	Receive IF
Video Processor	Analyzer IF
	Log Amp
Sweep Digitizer	Quasi-peak (option)
Video Processor	10.7 MHz (FM/AM/SSB)
	Receiver Option
Control Processor	Frequency Synthesis
Control Processor PC Board	Reference Oscillator
Interface PC Board	1st LO Sampling Loop
Keyboard	1350-2350 MHz VCO
CRT	Synthesizer #1
GPIB Interface PC Board (Option)	Synthesizer #2
	2nd LO Summing Loop
RS-232c Interface PC Board	
Generator (Option)	
Tracking Generator with 0 to 75 dB Output Attenuator (Option)	

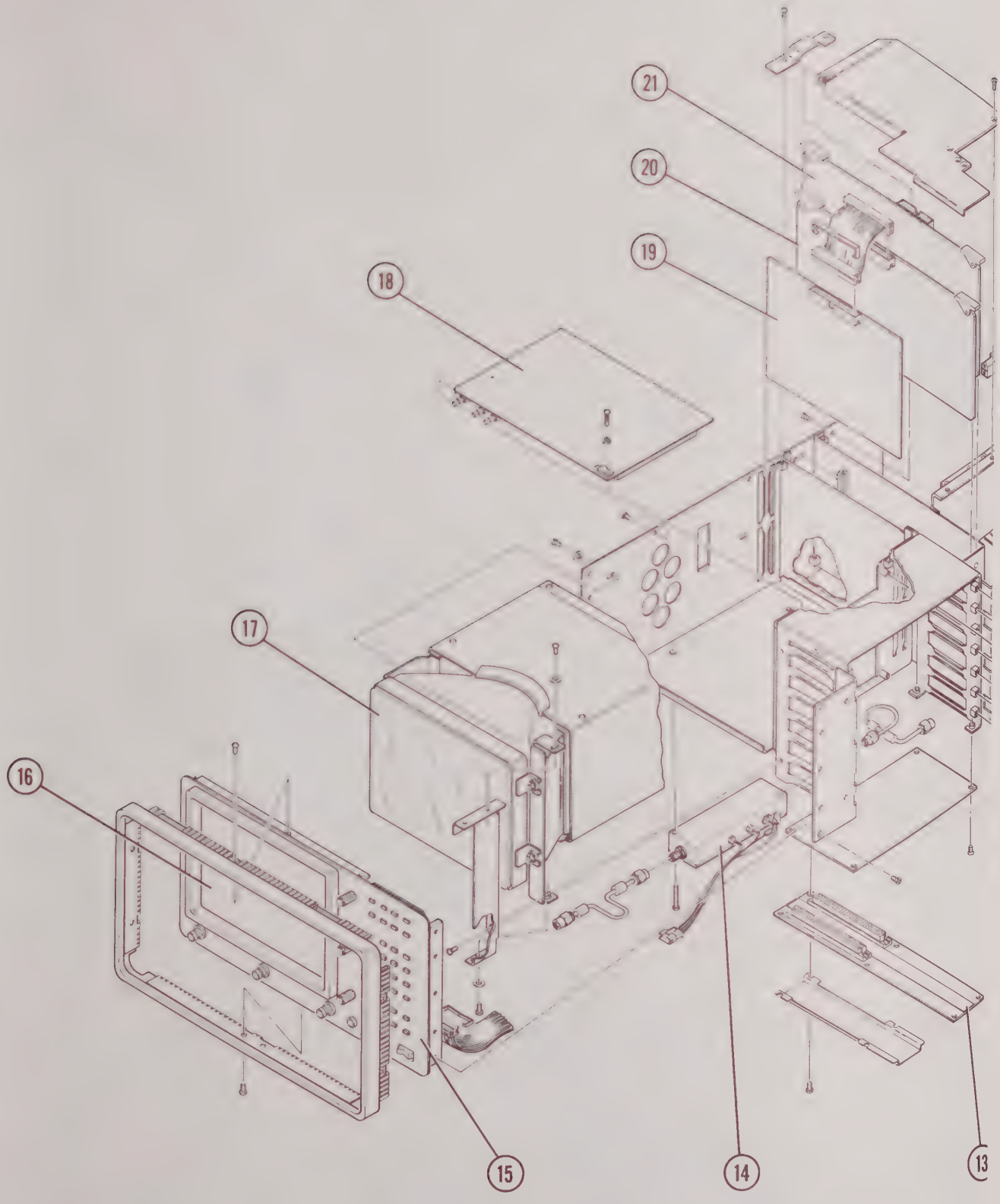
Table 1-1 A-7550 Major Electrical Circuits

1-3 MECHANICAL DESCRIPTION

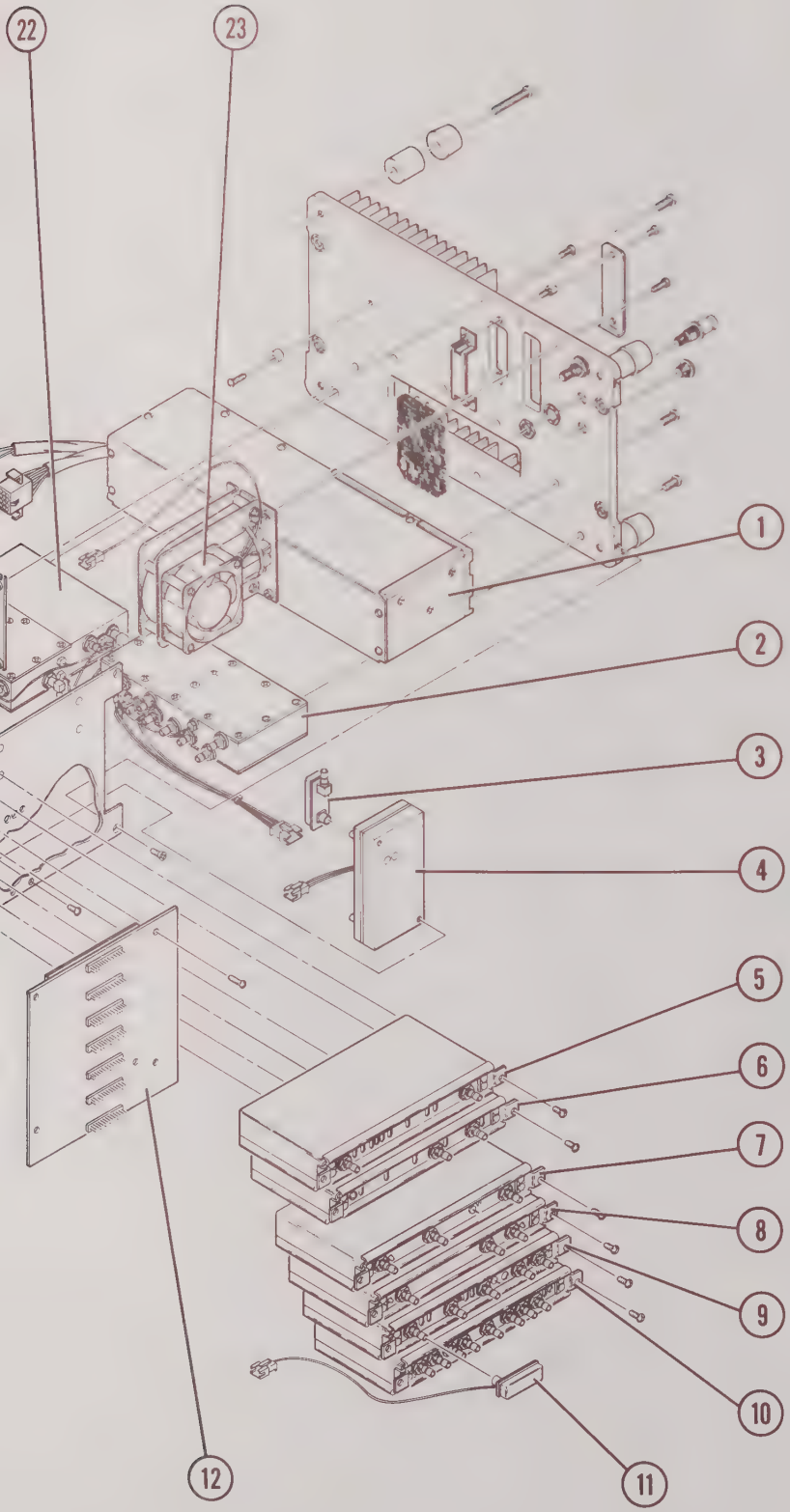
The location of each module is broken down for mechanical purposes in Table 1-2. Refer to the Composite drawings (Figure 1-1), as appropriate, to locate each A-7550 module.

Front	Rear
Front Panel	Power Supply
CRT	Rear Panel
Keyboard	
Top	**Bottom**
VCO Filter Module	Receive IF
Interface PC Board	2nd LO Summing Loop
Control Processor PC Board	1350-2350 MHz VCO
Video Processor PC Board	0-60 dB Input Attenuator
Sweep Digitizer PC Board	Digital Motherboard
Battery (Option)	Tracking Generator (Option)
Quasi-peak (Option)	0-75 dB Attenuator (Option)
GPIB PC Board (Option)	
RS-232c PC Board (Option)	
Right Side	
Log Amp	Analyzer IF
10.7 MHz (FM/AM/SSB) Receiver (Option)	
Synthesizer #1	Synthesizer #2
1st LO Sampling Loop	Reference Oscillator
RF Motherboard	

Table 1-2 A-7550 Mechanical Groups



A-7550 Composite with Module Identification



(Without Options)

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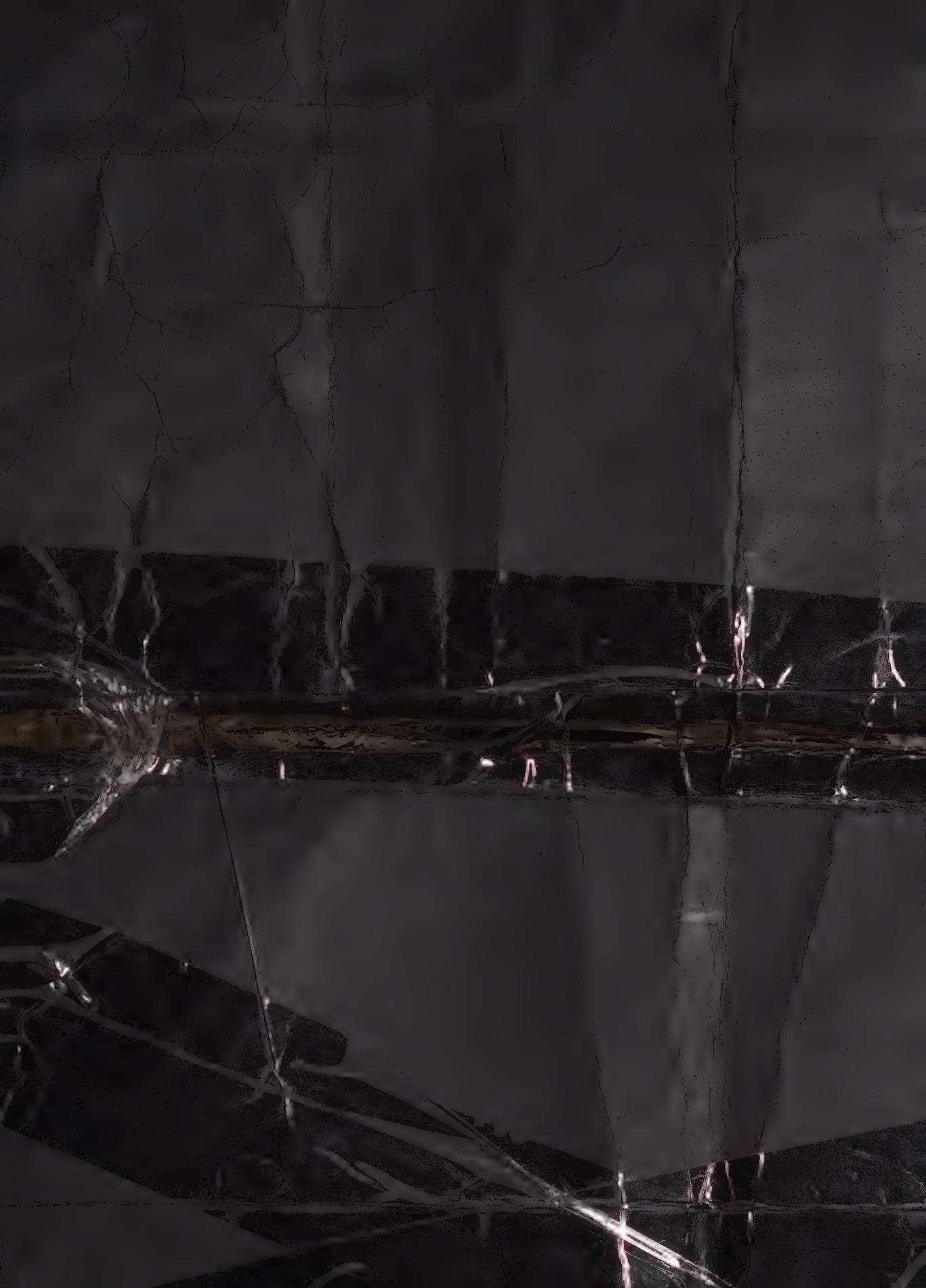
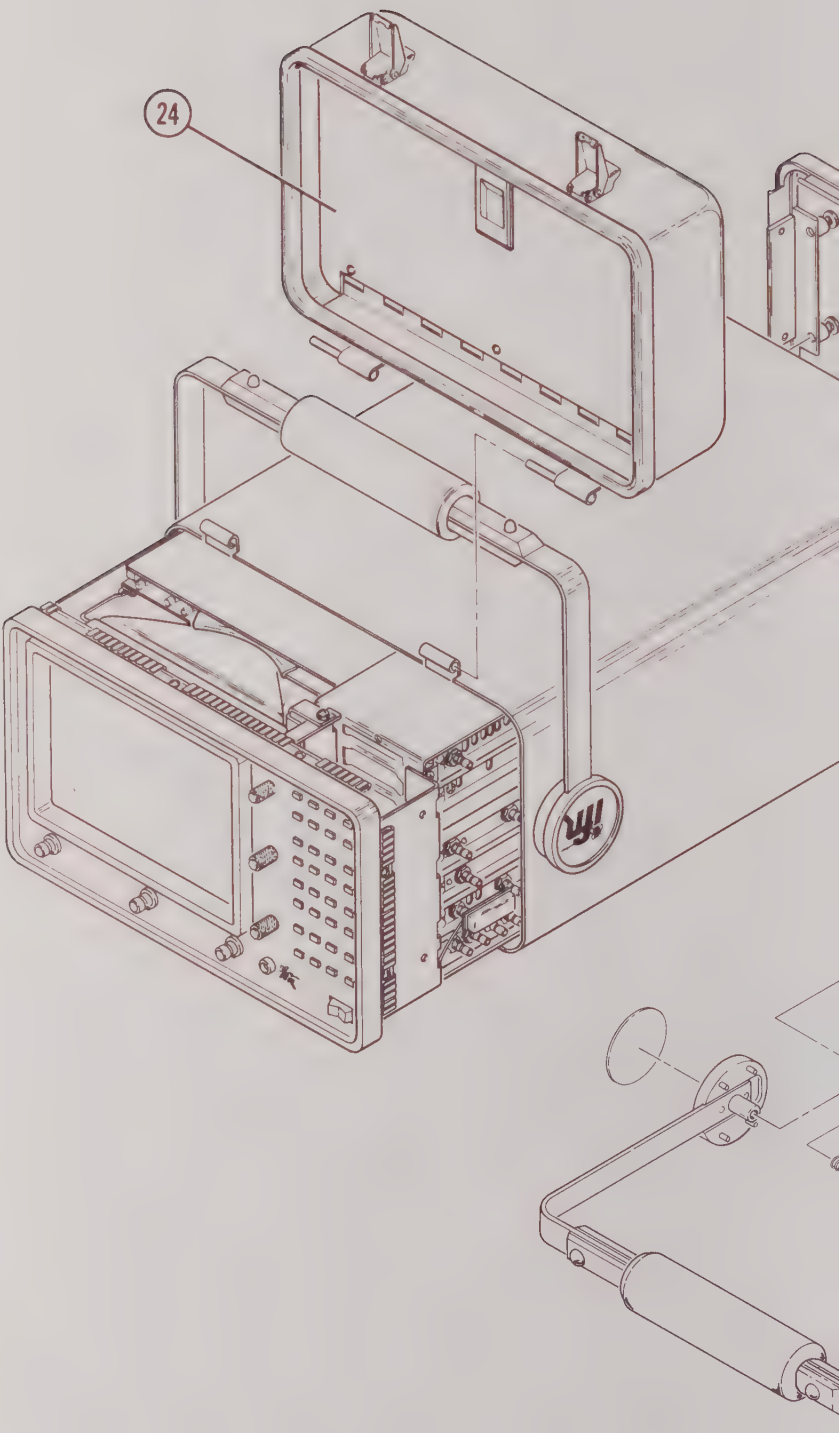


Power Supply Assembly
Receive IF Assembly
1380-2350 MHz VCO Filter Assembly
1350-2350 MHz VCO Assembly
Analyzer Log Amp Assembly
Analyzer IF Assembly
Synthesizer #1 Assembly
Synthesizer #2 Assembly
First LO Sampling Loop Assembly
Reference Oscillator Assembly
Buffer Amp PC Board Assembly
RF Motherboard PC Board Assembly
Digital Motherboard PC Board Assembly

14. 0/60 dB Attenuator Assem
15. Keyboard Assembly
16. Front Panel Assembly
17. CRT Display Assembly
18. Interface PC Board Assem
19. Sweep Digitizer PC Board Assembly
20. Video Processor PC Board Assembly
21. Processor PC Board Assem
22. Second LO Summing Loop Assembly
23. Fan Assembly
24. Lid Assembly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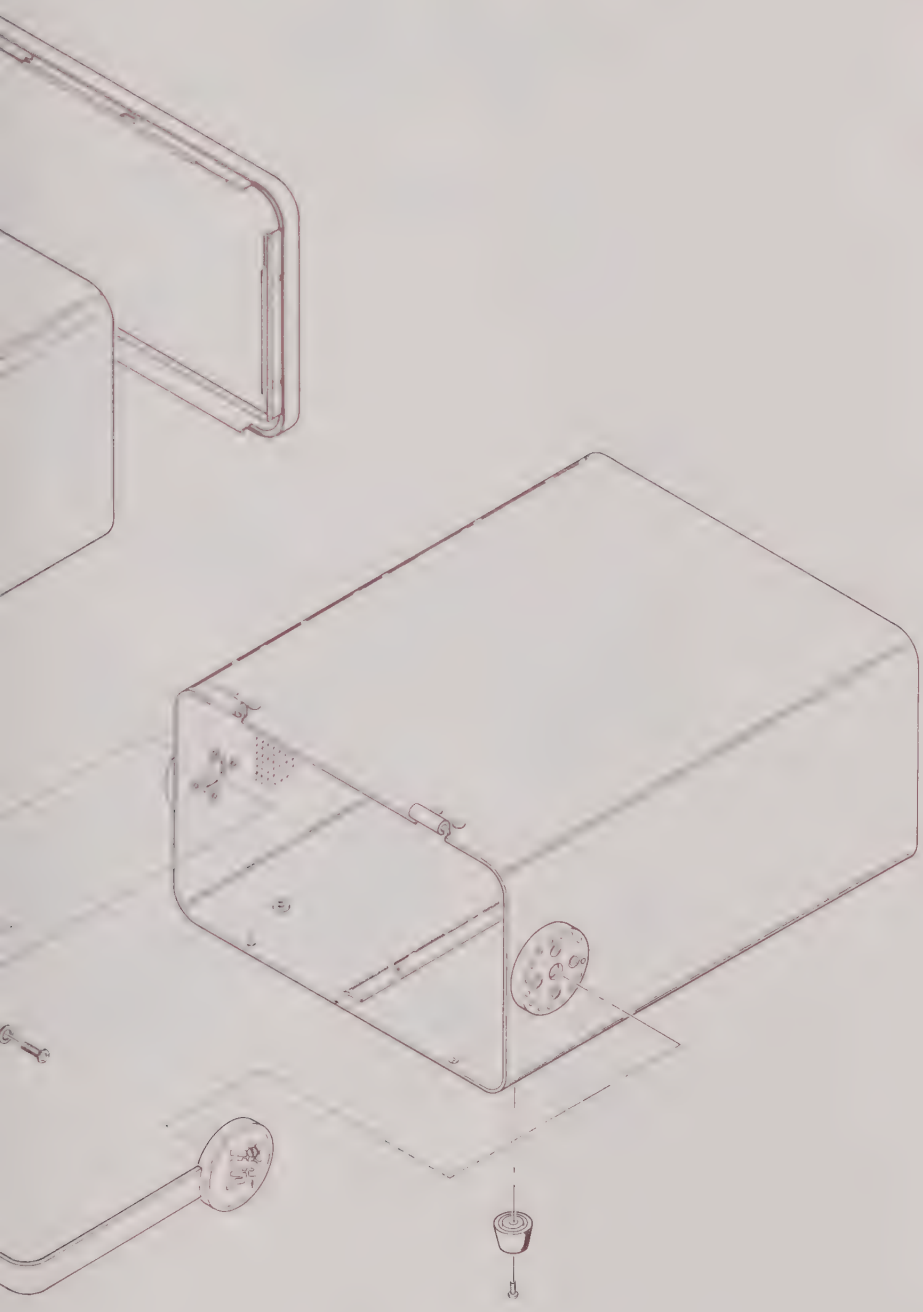
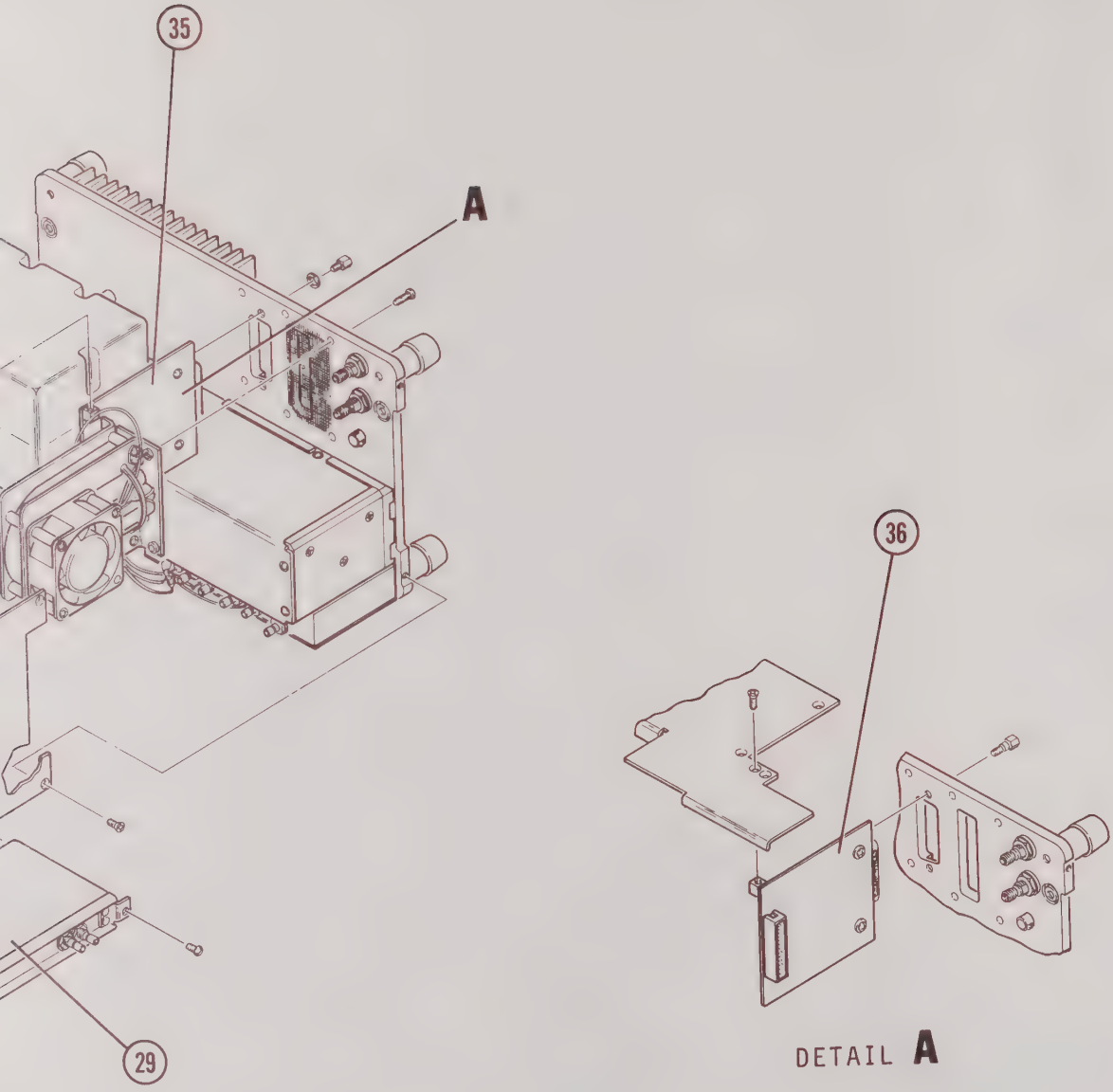
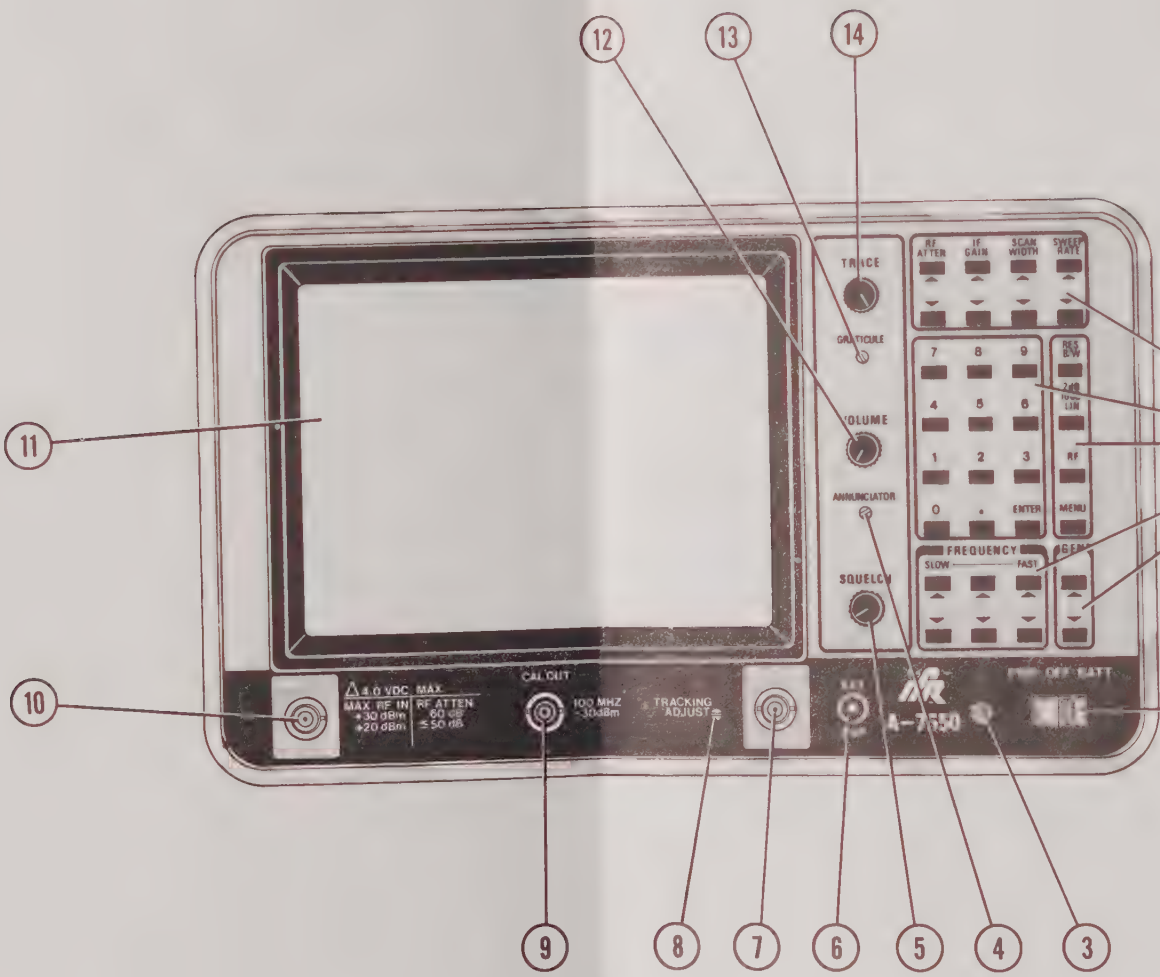


igure 1-1 A-7550 Spectrum Analyzer (Sheet 1 of 2)



Composite with Module Identification (Options & Accessories)

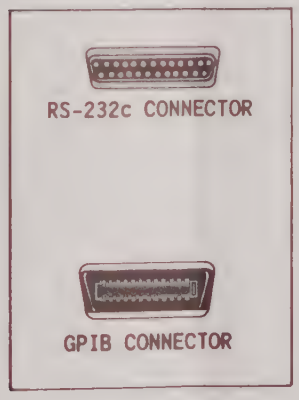
Figure 1-1 A-7550 Spectrum Analyzer (Sheet 2 of 2)



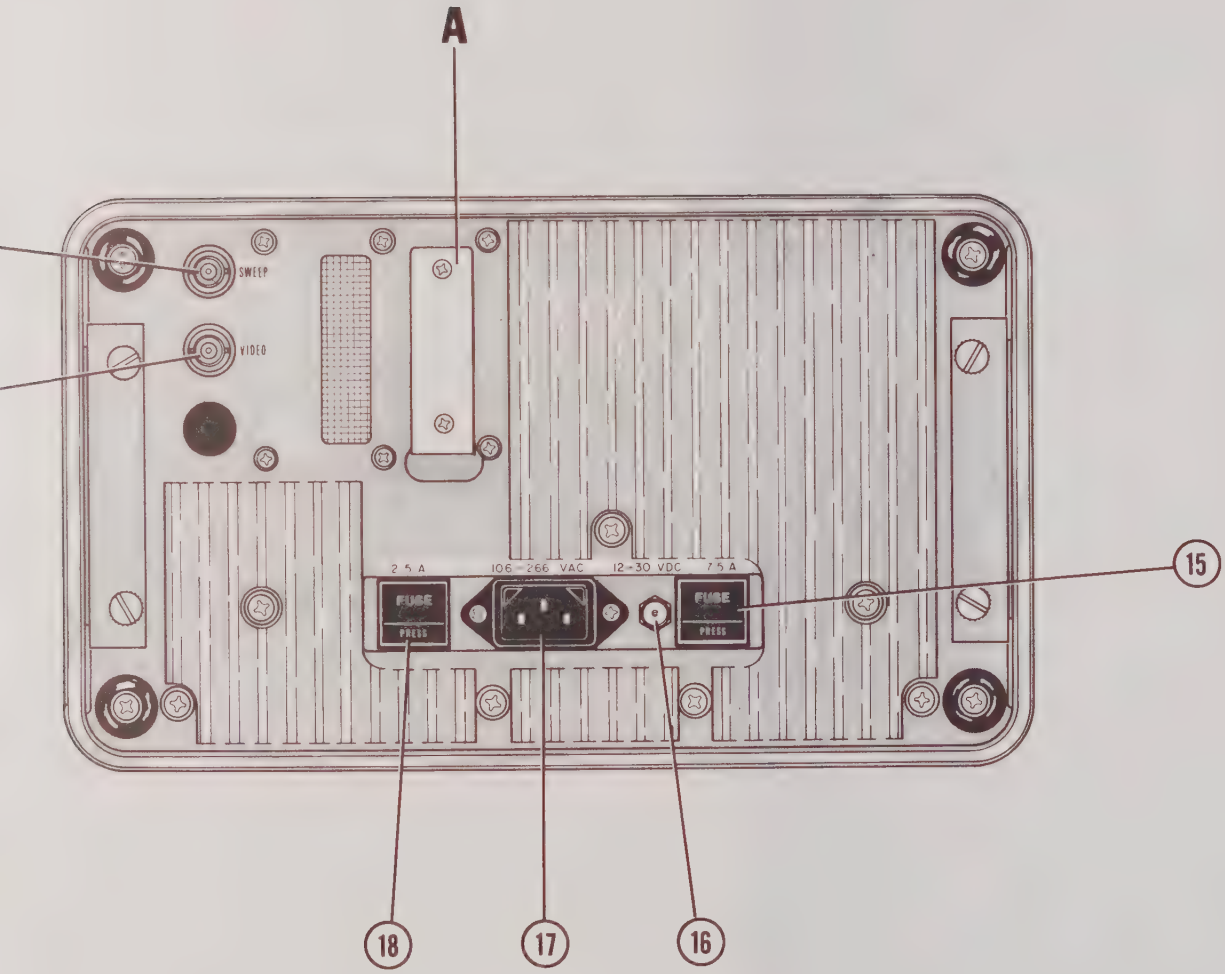
Front Panel Assembly

KEY:

1. Keyboard
2. PWR/OFF/BATT Switch
3. Power On Indicator
4. ANNUNCIATOR (Volume Adjust)
5. SQUELCH Control
6. EXTernal AMP Connector
7. GENERATE OUTPUT Connector
8. TRACKING ADJUST
9. CAL OUT Connector
10. ANALYZER INPUT Connector
11. CRT Display
12. VOLUME Control
13. GRATICULE Intensity Adjust
14. TRACE Intensity Adjust
15. DC Fuse
16. DC Power Input Connector
17. AC Power Input Connector
18. AC Line Fuse
19. ANALOG VIDEO Out Connector
20. SWEEP Out Connector



DETAIL **A**



Rear Panel Heat Sink

Figure 1-2 A-7550 Controls, Connectors & Indicators

SECTION 2 - THEORY OF OPERATION

2-1 GENERAL

This section contains three levels of Theory of Operation. It is organized as follows:

A. System Theory of Operation

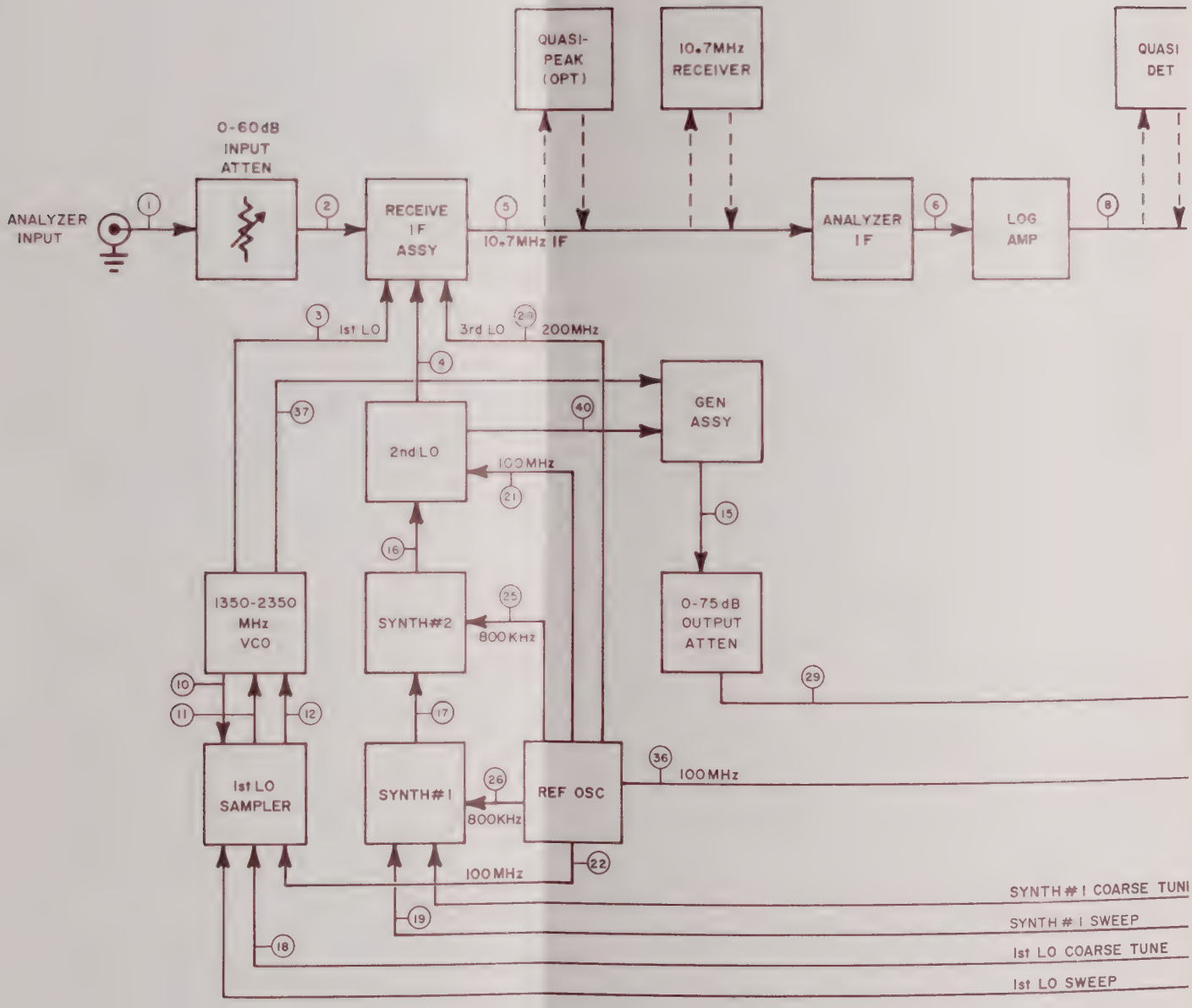
Paragraph 2-2 describes a simplified description of signal flow through the A-7550 Spectrum Analyzer. A system block diagram (Figure 2-1) illustrates the signal flow.

B. Functional Theory of Operation

Paragraph 2-3 describes the major functional groupings of the A-7550 Spectrum Analyzer. The descriptions correspond with block diagrams included for each functional group of modules.

C. Detailed Theory of Operation

Paragraph 2-4 describes the detailed theory of operation for each module and PC board in the A-7550 Spectrum Analyzer. The descriptions are accompanied by a block diagram and, in Section 5 of this manual, Mechanical and PC board assembly drawings and Schematic diagrams.


QUASI-
PEAK
(OPT)
10.7MHz
RECEIVER
QUASI
DET
0-60dB
INPUT
ATTEN
ANALYZER
INPUT
1
2
RECEIVE
IF
ASSY
5
10.7MHz IF
ANALYZER
IF
6
LOG
AMP
8
3
1st LO
3rd LO
200MHz
4
GEN
ASSY
37
40
2nd LO
100MHz
21
15
16
1350-2350
MHz
VCO
SYNTH#2
25
800KHz
0-75dB
OUTPUT
ATTEN
29
10
11
12
17
1st LO
SAMPLER
SYNTH#1
26
800KHz
REF OSC
36
100MHz
22
100MHz
SYNTH#1 COARSE TUNE
19
SYNTH#1 SWEEP
18
1st LO COARSE TUNE
1st LO SWEEP

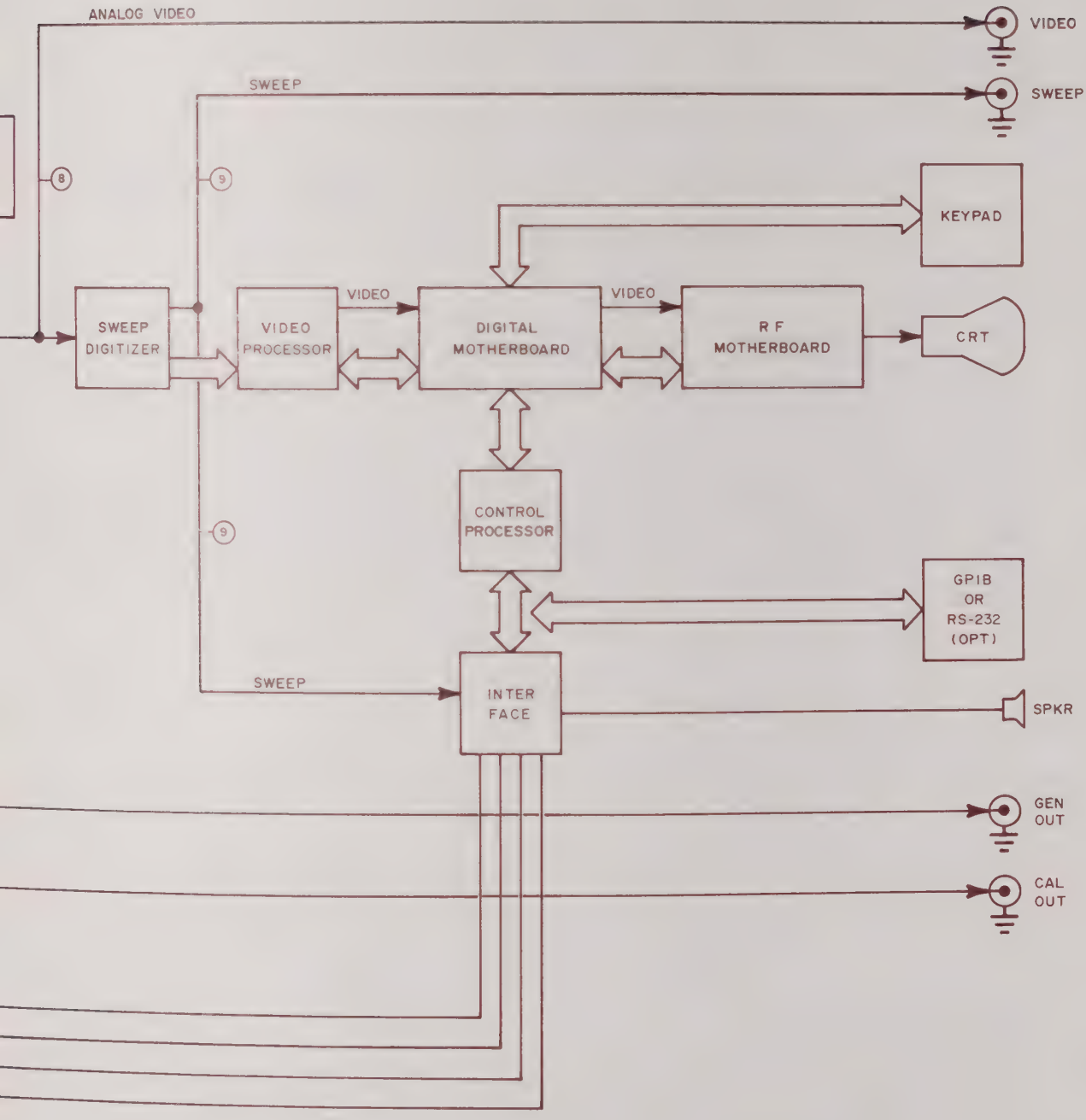


Figure 2-1 A-7550 System Block Diagram

2-2 SYSTEM THEORY OF OPERATION

The A-7550 is an RF Spectrum Analyzer that is microprocessor controlled. The control functions are selected on the keyboard, which includes an entire menu hierarchy. The operation and selection of the keyboard and menus are described in the A-7550 Operation Manual. The CRT display system operates with a Vertical Raster Scan (VRS™ is a registered trademark of IFR Systems, Inc.). The A-7550 can use external AC or DC power supply or, optionally, an internal battery power supply.

The microprocessor system can automatically select and optimize the scan width, sweep rate, display resolution, and step the frequency using the slew keys. Center Frequencies (CF's) from 100 kHz to 999.9999 MHz can be entered directly from the numeric portion of the keyboard. Amplitude can be read on 2 dB/Div, 10 dB/Div or Linear scales. The scales can be referenced in dBm, dBμV, dBV or dBμW units.

All menu selectable functions of the A-7550 Spectrum Analyzer are concurrently displayed with graticule and trace information. Signals can be displayed in six different modes to facilitate various functions of the Spectrum Analyzer, including "Live," "Average (AVE)," "Compare (COMP)," "Store," "Recall," and "Peak hold (PkHold)." The "STORE" mode is used to store a current trace, which can be later viewed using the "RECALL" mode or compared with the current display using "COMP" mode. "PkHold" is useful with a variety of applications including EMC measurements with the Quasi-peak option. Table 2-1 lists the expandable A-7550 options. A-7550 Spectrum Analyzer Accessories are listed in Appendix G.

The input signal is processed by the Receiver Group consisting of a 0 to 60 dB Attenuator, Receive IF module, Analyzer IF module and Log Amp module. Options available with this group include Quasi-peak and the 10.7 MHz (FM/AM/SSB) Receiver.

The Video Processor Group digitizes the signal and combines it with graticule and sweep information for display purposes. The Video Processor group consists of the Sweep Digitizer and the Video Processor.

The Control Processor Group is mainly responsible for routing information between modules and, with the use of the GPIB and RS-232C options, between other units as part of a computer system. The Control Processor group consists of Digital Motherboard, Control Processor, RF Motherboard, Interface PC board, CRT and Keyboard.

The Frequency Synthesis group provides the frequency steering and phase lock function for the Receiver and Generator groups. The Frequency Synthesis group includes the 1st LO Sampler, Synthesizer #1, Synthesizer #2, 2nd LO, Reference Oscillator (3rd LO) and, optionally, a Tracking Generator.

Option	Description
01	Internal Rechargeable Battery
02	Tracking Generator with 0 to 75 dB Attenuator, 1 dB Step Attenuator
04	10.7 MHz (FM/AM/SSB) Receiver
05*	GPIB (IEEE Standard 488-1978)
06*	RS-232C Interface
08	Quasi-peak

Table 2-1 A-7550 Spectrum Analyzer Options

* Options 05 and 06 cannot be used in one unit at the same time.

2-3 FUNCTIONAL THEORY OF OPERATION

2-3-1 RECEIVER SECTION OPERATION

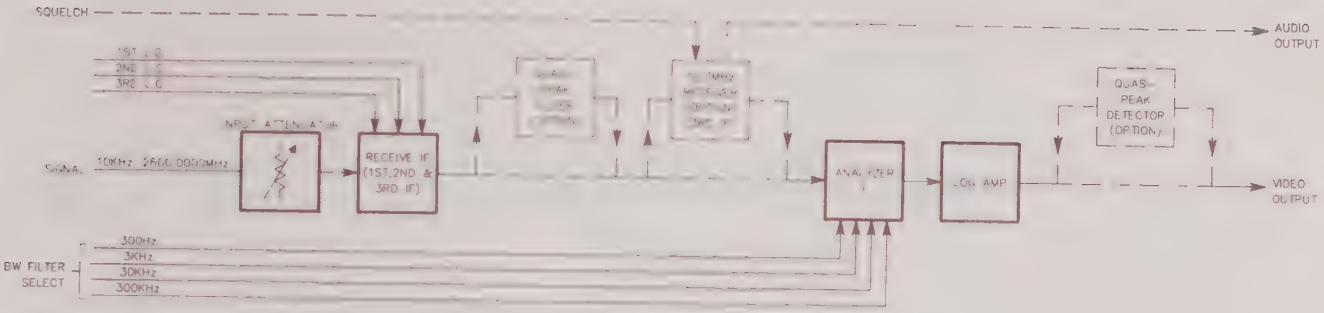


Figure 2-2 Receiver Group Block Diagram

The input signal is processed by the Receiver group. The Input Attenuator provides up to 60 dB attenuation in 10 dB steps. The Receive IF assembly receives the signal, triple converts it by mixing it with signals from the Frequency Synthesis group, and produces an IF of 10.7 MHz with MHz bandwidth. The Analyzer IF allows filtering for 300 kHz, 30 kHz, 3 kHz and 300 Hz bandwidths. The signal is then processed by the Log Amp module, where it is either logarithmically or linearly amplified. Up to 65 dB of IF Gain can be introduced in the Log Amp module in 1 dB steps. If the 10.7 MHz Receiver is installed, the IF signal is tapped for selective filtering and demodulation. If the Quasi-peak module is installed, selected bandwidths of 200 Hz, 9 kHz and 120 kHz are added for EMC testing.

2-3-2 VIDEO PROCESSOR OPERATION

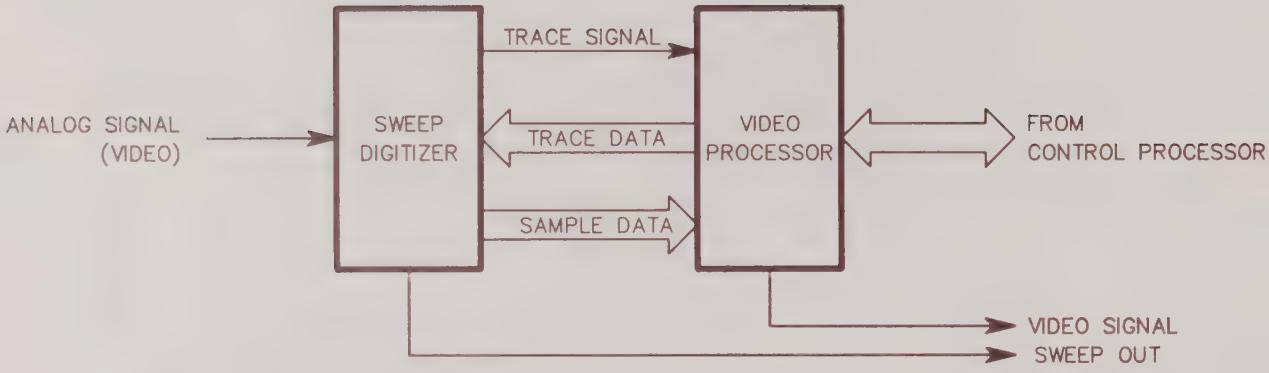


Figure 2-3 Video Processor Functional Block Diagram

The Video Processor group:

A. Digitizes the analog signal from the Receiver group;

B. Processes and stores data samples, as required;

C. Generates a video signal of alphanumeric (AN), graticule, and trace information, and passes it to the CRT for display; and

D. Provides sweep information for the Frequency Synthesis group.

2-3-3 CONTROL PROCESSOR OPERATION

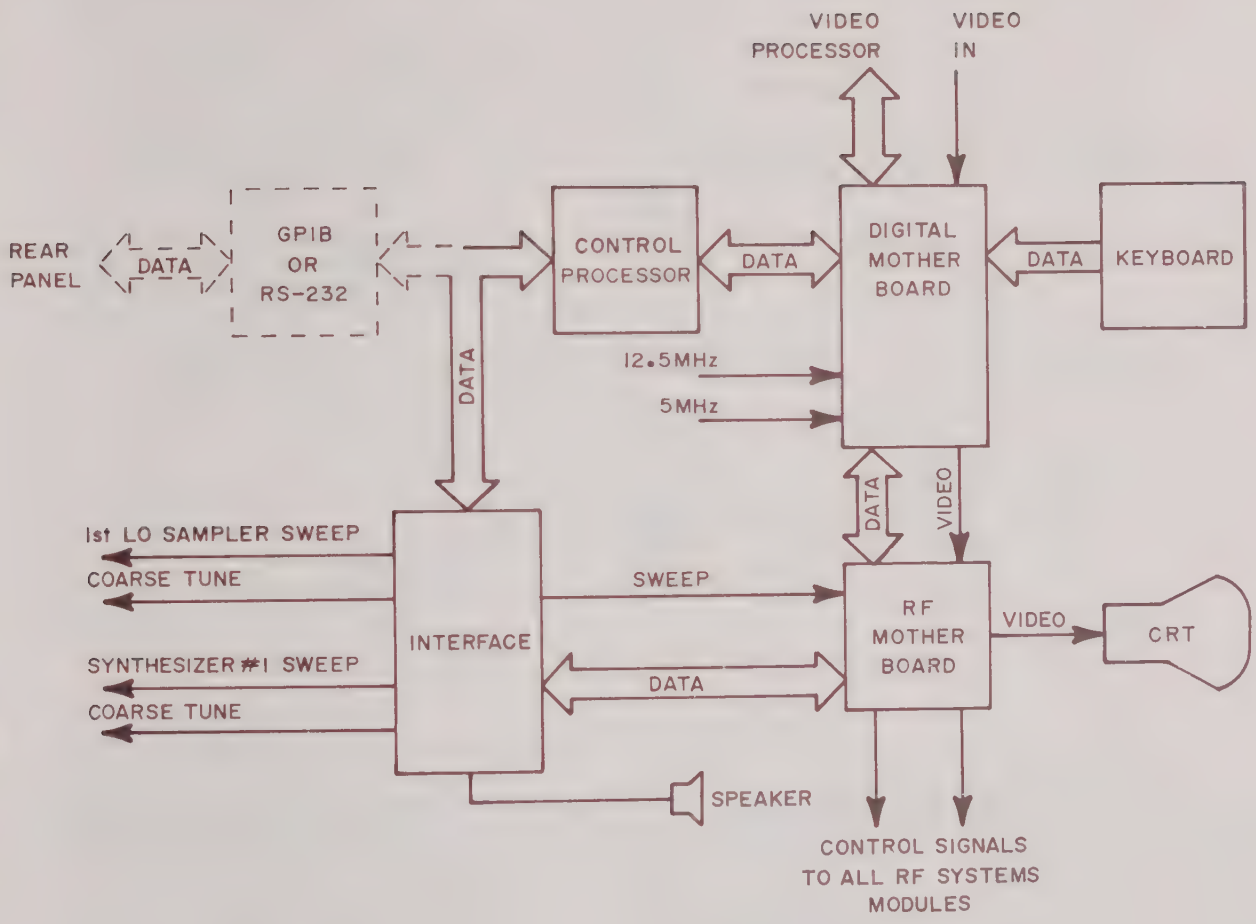


Figure 2-4 Control Processor Functional Block Diagram

The Control Processor is the "nerve center" of the A-7550 Spectrum Analyzer. Signals and data are accepted, controls and parameters are set and interfacing can be provided between the A-7550 Spectrum Analyzer and external units via GPIB and RS-232C interfacing. Digital information from the Keyboard, Video Processor and Control Processor are communicated through the Motherboards. The Interface board generates digital and analog signals to control operation of the RF system.

2-3-4 FREQUENCY SYNTHESIS OPERATION

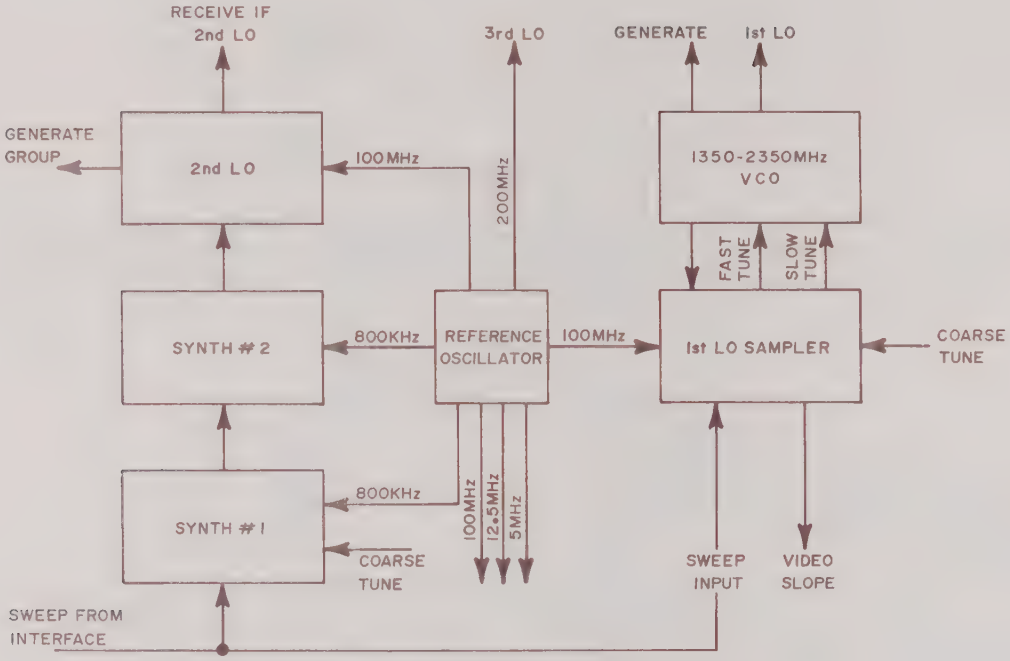


Figure 2-5 Frequency Synthesis Functional Block Diagram

The Frequency Synthesis functional block performs the frequency steering and phase lock functions for both the Receive IF and Generator modules. To do this, reference frequencies from the Reference Oscillator and control signals from the Interface PC board are used. The 1st LO Sampling Loop steers the 1350-2350 MHz VCO, which drives the 1st Mixer in the Receive IF module and the 2nd Mixer in the Generate module. Synthesizer #2 and the 2nd LO modules, together, drive the 2nd Mixer in the Receive IF module and the 1st Mixer in the Generate module.

The frequencies developed in the Frequency Synthesis section depend on the center frequency and the scanwidth selections entered by the operator. Paragraph 2-3-5 explains how the different A-7550 frequencies are developed.

2-3-5 FREQUENCY CALCULATIONS

All calculations are based on the lock frequency, which is the frequency at the left edge of the screen. First, center frequency (cf) is entered from the keyboard in the format:

abc.defg (MHz)

The cf is adjusted for scanwidth to give the lock frequency:

ABC.DEFG = abc.defg - (5 * scanwidth/division)

A. 1st LO Frequency

To determine the 1st LO frequency:

1. Compute n = ABC/50 (truncate the remainder)

2. 1st LO frequency = 1300 MHz + (50 * n) Synthesizer #1 Frequency

Compute the Synthesizer #1 frequency from the lock frequency and the sweep range (see note):

SWEEP RANGE	SYNTH #1 OUTPUT	ACTUAL FREQUENCY
I	0.2EFG MHz	output * 500
II	2.0EFO MHz	output * 50
III	2.00EO MHz	output * 50
IV	2.0000 MHz	output * 50

NOTE: See Table 2-4 for sweep ranges and a condensed calculation scheme of A-7550 frequencies.

B. Synthesizer #2

Synthesizer #2 has two oscillators: the Summing Oscillator and the Synthesizer #2 oscillator. Its frequency is determined by the lock frequency and the sweep range (see Table 2-2).

SWEEP RANGE	SYNTH #2 FREQ
I	160.9 - BC.D MHz
II	162.7 - BC.D MHz
III	180.7 - BC.D MHz

Table 2-2 Synthesizer #2 Frequency Calibration

C. Summing Oscillator Frequency

The Summing Oscillator frequency is Synthesizer #2 frequency - Synthesizer #1 frequency for sweep ranges I and II. For sweep range III, the ÷10/÷1 line controls a divider that alters the equation to Synthesizer #2 - (10 * Synthesizer #1) (see Table 2-4). Both oscillators have high and low ranges selected by the Control Processor.

SWEEP RANGE	SUMMING OSCILLATOR FREQUENCY
I	Synth #2 - Synth #1
II	Synth #2 - Synth #1
III	Synth #2 - (10 * Synth #1)

Table 2-3 Summing Oscillator Frequency Calculation

NOTE: This is the output of Synthesizer #2.

D. 2nd LO Frequency

To calculate the 2nd LO frequency:

2nd LO frequency = Synthesizer #2 frequency + 1000 MHz

SCAN RANGE	SCANWIDTH PER DIV	SYNTH #1 DIVIDE	SYNTH #2 MULTR	SWEPT BY	SWEEP RAMP	NOTE
I	0 kHz 1 kHz 2 kHz 5 kHz 10 kHz	÷500	X1	Synth #1 (÷100)	none 1 2 5 10	1
II	20 kHz 50 kHz 100 kHz	÷50	X1	Synth #1 (÷10)	2 5 10	
III	200 kHz 500 kHz 1 MHz	÷50	X10	Synth #1 (÷1)	2 5 10	
IV	2 MHz 5 MHz 10 MHz 20 MHz 50 MHz 100 MHz	÷50	X10	1st LO Sampler (÷10) (÷1)	2 5 10 2 5 10	

NOTE: The ÷10, ÷1 circuit in the difference frequency line of Synthesizer #2 effectively multiples the incoming Synthesizer #1 frequency by X10 or X1.

Table 2-4 A-7550 Frequency Calculations

2-3-6 GENERATOR SECTION OPERATION

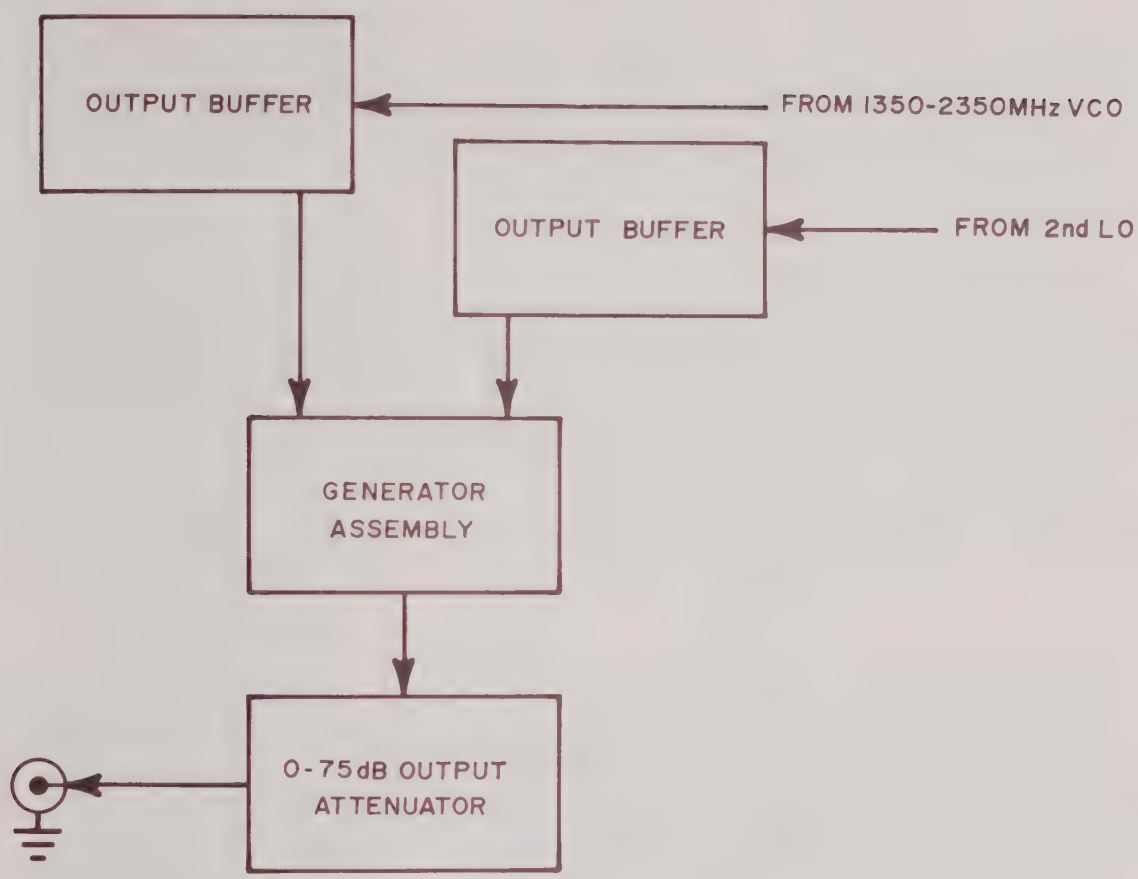


Figure 2-6 Generator Functional Block Diagram

The Generator group performs a tracking generator function. It uses selected outputs of the frequency synthesis group and an internal oscillator to create a tracking signal.

2-4 DETAILED THEORY OF OPERATION

The Theory of Operation in the remainder of this section gives supplementary information to the technician concerning the operation of each module in the A-7550 Spectrum Analyzer. A block diagram accompanies the theory of most modules to assist the technician in following the functional flow of the schematics supplied in Section 5.

2-4-1 POWER SUPPLY

The Power Supply can operate on AC or DC. The AC input can be 106 to 226 VAC and 50 to 400 Hz. The DC input is an external +12 to +30 VDC source or optional +12 VDC internal battery. When the PWR/OFF/BATT switch on the front panel is set to PWR or to BATT, voltages of +12, -12, +5 and +40 VDC are sent to the RF Motherboard where they are distributed throughout the set and +12 VDC is sent to the fan assembly.

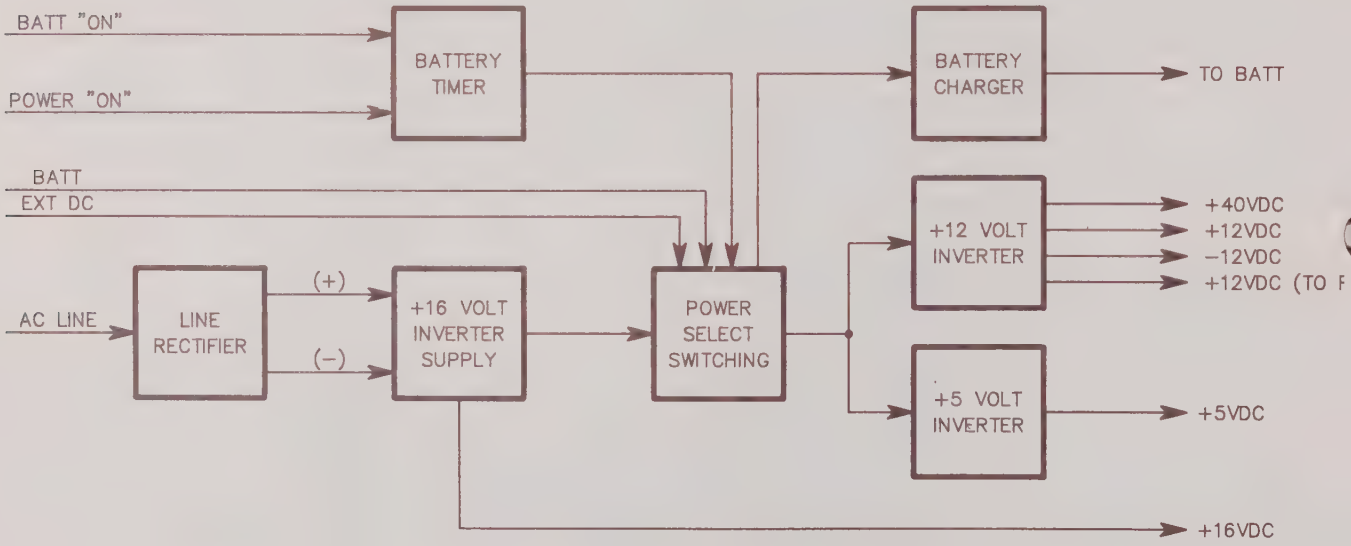


Figure 2-7 Power Supply Block Diagram

A. AC Line Voltage

WARNING: THE DIFFERENCE OF POTENTIAL BETWEEN THE FLOATING GROUND AND CIRCUIT OR CHASSIS GROUND CAN EXCEED 300 V. THIS POTENTIAL CAN CAUSE SERIOUS INJURY OR EVEN DEATH. ALWAYS USE AN ISOLATION TRANSFORMER AND TAKE EXTREME CARE WHEN WORKING WITH AC VOLTAGES INSIDE THE POWER SUPPLY MODULE.

The AC line voltage is filtered and rectified by T16001 and BR16001 on the Line Rectifier PC board. The output of the rectifier, several hundred volts DC, is filtered by C16001 and C16002. The negative output of the line rectifier is used as a floating ground.

The DC output of the rectifier is applied to the Power Supply PC board assembly, where it is sent to the step-down transformer (T17002) and the 15.8 V floating regulator, which also feeds the step-down transformer. Q17018, Q17019 and CR17027 form a sub-regulator that reduces the rectified DC voltage to approximately 15 V. The regulated DC is supplied to U17011, which produces a sawtooth waveform that is applied to the positive side of comparator (U17012). Opto-coupler (U17013) provides a controlled DC level, which is applied to the negative side of U17012 and produces a rectangular wave with the duty cycle controlled by the DC output of the opto-coupler (U17012).

This rectangular wave is applied to Q17020 and Q17021 to provide necessary drive current to give the FET switch (Q17022) fast turn-on/turn-off characteristics. Q17023, Q17024 and Q17025 act as current limiters. Q17022 essentially grounds one side of T17002 when the rectangular wave from pin 3 of U17012 is higher than pin 2. The output of T17022 is rectified by CR17024 and is fed back to the opto-coupler through U17010 to provide +16 V regulation. ADJUST trimpot (R17068) is used to tune the feedback controlling the +16 VDC level.

B. Battery Charger

The Battery Charger circuit operates on either +16 VDC derived from external AC or on external +15 to +30 VDC, depending on the source used. Q17001 supplies current through CR17006. Q17002 controls conduction of Q17001. Q17002 is controlled by voltage supplied by the comparator (U17001). BATT CHARGE trimpot (R17006) is used to adjust battery charge voltage to 14.4 V at Q17001 with 0.3 A minimum current. If the battery state is in low charge, the voltage output at Q17001 drops, which lowers the output voltage divider (R17004, R17005 and R17006) to pin 3 of U17001. Reducing U17001 output allows Q17002 to conduct, which increases conduction at Q17001. T17001 limits the maximum current which Q17001 can draw to approximately 1.5 A.

C. Battery Timer/Enable

The Battery Timer and Enable circuit includes flip-flop U17002B and related components. When the PWR/OFF/BATT switch is toggled to BATT, the resulting ground discharges C17003 through R17014, forcing pin 11 of U17002B into a low state.

As C17003 charges, the increasing voltage sets clock output, Q (pin 13, U17002B) high, which turns on Q17005 to enable the DC regulation circuits. Pressing the PWR/OFF/BATT switch a second time sets clock output low (pin 12, U17002B). If U17002B is not clocked a second time, the timer circuit will reset U17002B approximately ten minutes later.

Programmer timer (U17003) starts counting when it initially receives +12 V output. A terminal count is set at pins 9 through 12. The on-chip oscillator frequency is established by R17022, R17023 and C17006 to allow approximately ten minutes of battery operation, after which, U17003 provides a high output which resets U17002B (pin 12) to a low state and terminates battery operation.

A low-voltage battery cutoff circuit stops battery operation if battery voltage drops below approximately +11.4 VDC. Regulated +12 VDC is applied to emitter of Q17006 and battery voltage drops to approximately +11.4 VDC, Q17006 turns on and applies +12 VDC to the SET pin (pin 1) of U17003. This sets timer to terminal count and causes U17002B to go to a low state, which terminates battery operation.

External power operation is enabled by pressing the PWR/OFF/BATT switch to PWR. This applies a ground to the base of Q17004, turning it on, and causing Q17004 and Q17005 to turn on. Q17003 is provided for fast circuit shutdown if external power is lost.

D. +12 V Regulator

Q17005 provides a ground for the enable line if either battery or external power is selected. This turns on Q17007 and turns off Q17012. When Q17007 is on, Zener diode CR17013 sets a +10 VDC level which is applied to U17004, U17005, U17006, U17007, U17008 and U17009. When Q17012 is off, U17004 produces a sawtooth wave that is applied to the non-inverting input of integrator, U17005. Zener diode (CR17013) produces a sawtooth wave that is applied to the non-inverting input of U17005. +6.9 VDC is produced by Zener diode (CR17021) as a reference source for the +12 VDC and +5 VDC voltage regulator circuits. U17005 compares the oscillator output level (U17004 and related components) with the reference level from U17008 and produces a pulsed output with a duty cycle that decreases as the reference level increases. R17035 and R17037 set a minimum reference to allow a 50% maximum duty cycle.

The output of the square wave generator (U17005) drives the complementary pair (Q17008 and Q17009). The output of the complementary pair drives the parallel FET's (Q17010 and Q17011), which charge and discharge the primary coil of T17001 in proportion to the duty cycle of the square wave from U17005. The -12 VDC and +40 VDC track the +12 VDC output.

E. +5 V Regulator

+5 VDC is generated by FET's Q17016 and Q17017 pulsing current to the low-pass filter (L17008, L17009 and C17023). The duration of the pulsed current determines the level of voltage at the output of the low-pass filter. The FET's (Q17016 and Q17017) are placed in parallel for adequate current drive capability and lower resistance. CR17022 provides a discharge path for L17008, preventing inductive "kick" through the FET's.

The pulses are controlled by the generated rectangular wave from the comparator (U17007). The rectangular wave is buffered by Q17013 and the complementary amplifier formed by Q17014 and Q17015. This provides necessary on-off characteristics for optimum FET operation. The duty cycle of the rectangular wave is controlled by comparing a RAMP wave with a sample of the +5 VDC output. The RAMP wave is generated at U17006; the RAMP time constant is set by R17041, C17017 and R17043. The start of the RAMP is timed by U17006 to allow FET's Q17016 and Q17017 to draw current from the +16 V supply line, 180° out of phase with the +12 VDC supply FET's (Q17010 and Q7011). This reduces the ripple in the power supply. A proportionate sample of +5 VDC is compared with a Zener referenced voltage by U17009.

When the +5 V sample (R17060, R17061 and R17062) is higher than the divided output (R17057 and R17058) from the Zener diode (CR17021, approximately 4.45 VDC), the output of the comparator (U17009, pin 6) goes high. This causes the reference level to rise. Since the RAMP must increase to reach the reference level, the pulse width from U17007, pin 6 decreases and +5 VDC decreases. R17062 calibrates the +5 VDC.

2-4-2 INPUT (0 TO 60 dB) ATTENUATOR

100 kHz through 1000 MHz Analyzer Input is received through J34001. Up to 60 dB of Attenuation, in 10 dB steps, can be selected via keyboard selection. This allows the appropriate select lines (J34003) to be turned on.

Selecting 0 dB attenuation sets control lines to relays K35001 and K35002 to 0 V, bypassing the 10 dB and 20 dB attenuators. Pin 1 of J34003 supplies -12 V, which turns on diodes (CR35002 and CR35003) and bypasses the 30 dB attenuator.

Selecting 10 dB attenuation causes pin 3 of J34003 to go high (+12 V) and energizes relay K35001, which routes the signal through the 10 dB attenuator (R35001, R35002, R35003 and C35003) as the other control lines do not change. The signal is routed through the contacts of K35002 (bypassing the 20 dB attenuator) and bypasses the 30 dB attenuator. C35003 adjusts the frequency response of the 10 dB attenuator.

Selecting 20 dB attenuation allows pin 2 of J34003 to go high (+12 V) and energizes relay K35002, which routes the signal through the 20 dB attenuator (R35017, R35006, R35005 and C35007). The signal is routed through the contacts of K35001 (bypassing the 10 dB attenuator) and bypasses a 30 dB attenuator. C35007 adjusts frequency response of the 20 dB attenuator.

Selecting 30 dB attenuation causes pin 1 of J34003 to go high (+12 V), causing CR35001 and CR35004 to conduct. This routes the input signal through the 30 dB attenuator (R35008, R35009, R35011, C35008) and bypasses the 10 dB and 20 dB attenuators. C35008 adjusts the frequency response of 30 dB attenuator.

Selecting 40 dB attenuation routes the signal through the 10 dB and 30 dB attenuators. Selecting 50 dB attenuation routes the signal through the 20 dB and 30 dB attenuators. Selecting 60 dB attenuation routes the signal through the 10 dB, 20 dB and 30 dB attenuators.

2-4-3 RECEIVE IF

The Receive IF receives the attenuated RF input signal and, using LO's from the frequency synthesis modules, triple-converts it to produce a 10.7 MHz IF.

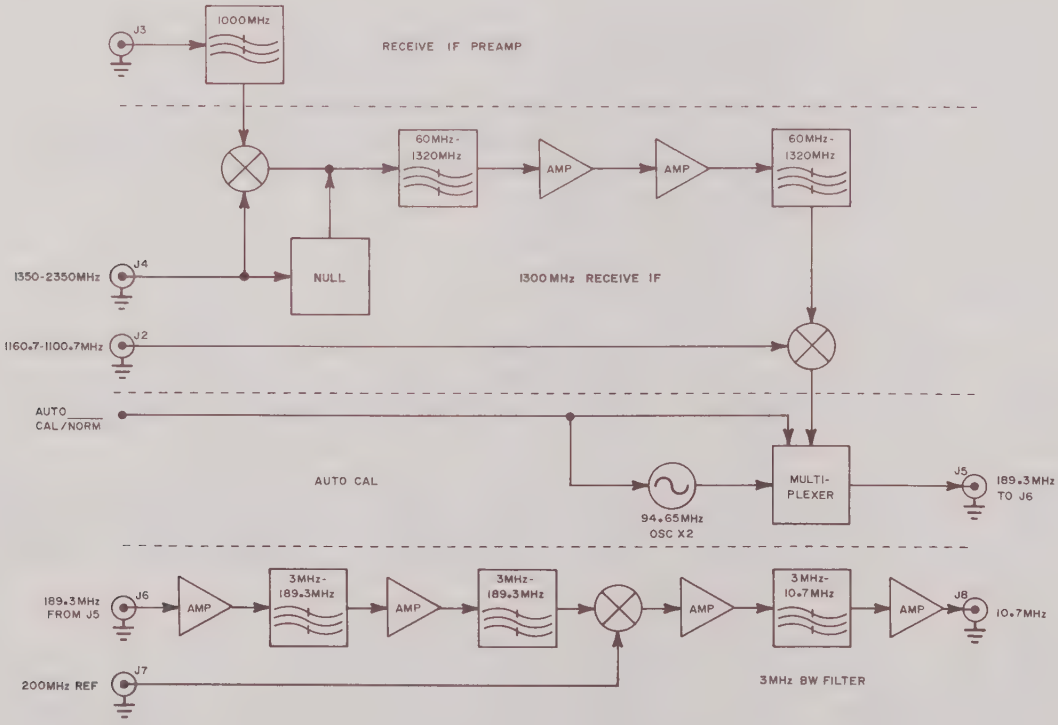


Figure 2-8 Receive IF Block Diagram

A. Input Low-pass Filter PC Board

The signal from the Input Attenuator passes through a stripline 1000 MHz Low-pass filter.

B. Buffer Amp

The 1st LO is filtered and amplified by Q73001 and related components which sends the 1350 to 2350 MHz LO to the first mixer.

C. 1300 MHz Receive IF

The 1st LO mixer (MXR41001) mixes the signal from the 1000 MHz Low-pass filter and the 1350 to 2350 MHz from the Buffer Amp, up-converting it to a 1290 to 1350 MHz IF. A null circuit (R45002, R45003 and related components) nulls the 1st LO frequency, the output of which, when in the passband (1290-1350 MHz), can overdrive the IF amplifiers, desensitizing the 0 to 10 MHz band. Q45001 and U45001 amplify the mixed signal after the resultant 1290 to 1350 MHz signal is bandpass filtered. L45001, L45002, C45010 and C45011 form a Low-pass filter. From U45001, the signal is again bandpass filtered for 1290 to 1350 MHz before it is input to the second LO mixer (MXR45002). MXR41002 down-converts the IF signal to 189.3 MHz by mixing the filtered signal with the 1100.71 to 1160.7 MHz input from the 2nd LO (J41002).

D. Automatic Calibration (Auto Cal)

The A-7550 Control Processor normally sets the AUTO CAL/$\overline{\text{NORM}}$ line to about -10 V. This forward biases CR43001 and CR43002, allowing the signal from the 1300 MHz Receive IF to pass to the 3 MHz Bandwidth filter PC board. Periodically, the Control Processor sets the AUTO CAL/$\overline{\text{NORM}}$ line high (about +10 V), which forward biases CR43003 to power up a 94.65 MHz calibrated oscillator circuit and shuts off the received signal. The oscillator then drives CR43007, resulting in a high level second harmonic (189.3 MHz). The 189.3 MHz harmonic is then used as a calibrated reference level.

The microprocessor uses the calibrated reference level of the oscillator (Q43001, Y42001 and associated components) to adjust the IF Gain and maintain the amplitude calibration of the A-7550 Spectrum Analyzer. The A-7550 performs an auto cal cycle every 600 sweeps.

L43006 is an adjustment for tuning the oscillator circuit. CR43005 is a level detector that biases Q43002 and Q43003 to maintain constant amplitude. CR43006 is used for temperature compensation. The RF output goes through CR43007, R43010 and R43011. The auto cal reference level is adjusted at trimpot R43010.

E. 3 MHz Bandwidth Filter

The 189.3 MHz IF is amplified (Q42001) before it is bandpass filtered for 189.3 MHz (C42005, C42006 and related components). The output of this filter is buffered and amplified again (Q42002) and bandpass filtered (L42005, L42006, L42007, L42008, C42011 and C42012) a second time before it is mixed (MXR42002) with 200 MHz third LO from the Reference module, producing 10.7 MHz IF.

The 10.7 MHz IF is twice filtered and amplified (Q42003, R42004 and related components). The resulting signal has a 3 MHz BW. The IF Gain is adjusted at trimpot R42029 to match the 10.7 MHz output level at J41008. The 10.7 MHz signal from J41008 is sent to the Analyzer IF module.

NOTE: If the Quasi-peak and/or the 10.7 MHz Receiver options are installed, the 10.7 MHz signal is routed through the optional modules (Quasi-peak, then 10.7 MHz Receiver) before it is passed to the Analyzer IF module.

2-4-4 ANALYZER IF

The Spectrum Analyzer IF selects the Resolution Bandwidth for the A-7550 Spectrum Analyzer display. Available bandwidths are 3 MHz, 300 kHz, 30 kHz, 3 kHz and 300 Hz.

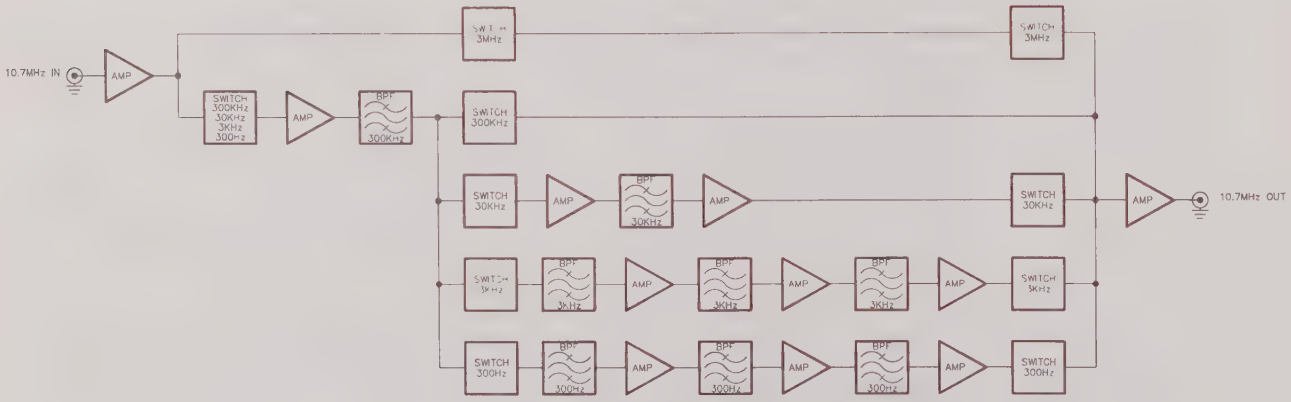


Figure 2-9 Analyzer IF Block Diagram

The 10.7 MHz IF is input from the Receive IF at J21003. Keyboard input selects the appropriate signal path for the bandwidth select line (P21001). Which select line goes high depends on the resolution bandwidth selected.

If 3 MHz bandwidth is selected, pin 2 of P21001 goes high, which bypasses any filtering in the module. All other bandwidth selections are first filtered through the 300 kHz bandwidth filter before any other selected bandwidth filter (i.e., 30 kHz, 3 kHz or 300 Hz filter). The selection process occurs through forward biasing select combinations of diodes.

Selecting 300 kHz bandwidth causes pin 4 of P21001 to go high, which forward biases CR22003, CR22002, CR22016 and CR22012. The bandwidth can be tuned at L22001 through L22008 and the level set with the 300 kHz LEVEL ADJUST trimpot (R22015).

Selecting 30 kHz bandwidth causes pin 1 of P21001 to go high, which forward biases CR22004, CR22002, CR22007 and CR22013. The bandwidth can be tuned at C22042 and C22043, and the level set with the 30 kHz LEVEL ADJUST trimpot (R22031).

Selecting 3 kHz bandwidth causes pin 3 of CR21001 to go high, which forward biases CR22005, CR22002, CR22008 and CR22014. The bandwidth can be tuned at C22052, C22053, C22056, C22058, C22062 and C22063 and the level adjusted with the 3 kHz LEVEL ADJUST trimpot (R22052).

Selecting 300 Hz bandwidth causes pin 5 of P21001 to go high, which forward biases CR22006, CR22002, CR22009 and CR22015. The bandwidth cannot be adjusted. The level is set with the 300 Hz LEVEL ADJUST trimpot (R22087).

Amplifier Q 22003 and associated parts bring the total gain across the Analyzer IF to +20 dBm. The IF Gain is adjusted with the IF LEVEL GAIN trimpot (R22020). The filtered 10.7 MHz IF analyzer output is then sent to the Analyzer Log Amp.

2-4-5 ANALYZER LOG AMP

The 10.7 MHz Analyzer IF is input to the Log Amp at J25003. The microprocessor in the Control Processor sets the control lines through keyboard operation to compensate for gain and temperature changes with Automatic Calibration (Auto Cal).

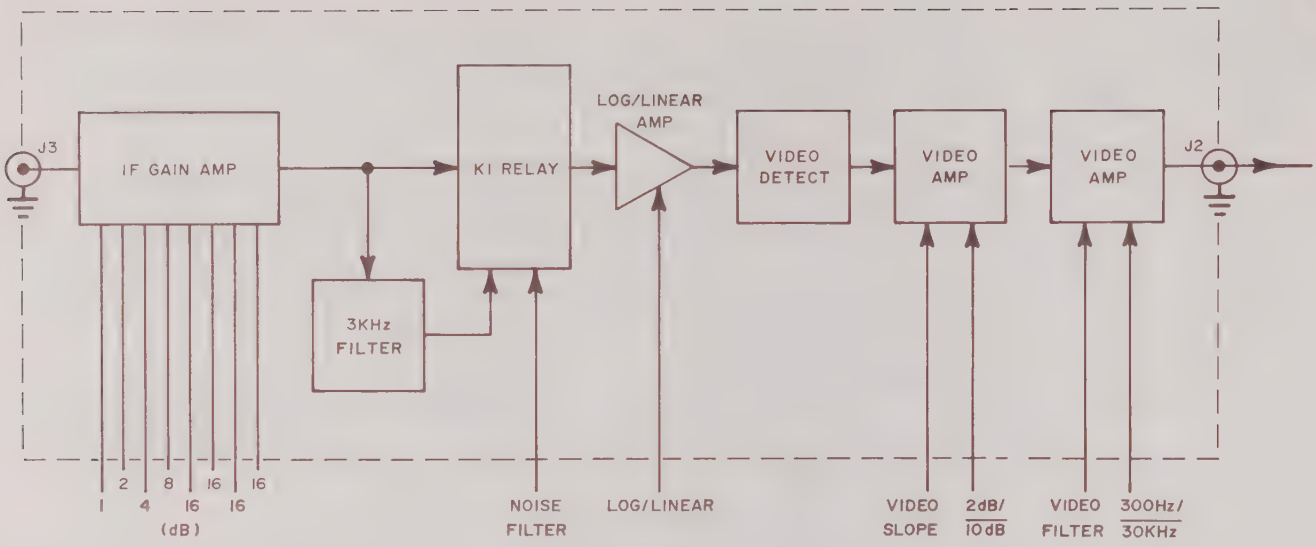


Figure 2-10 Log Amp Block Diagram

A. IF Gain

Pins 1 through 8 of P25001 receive the control signals for gain selection from the Control Processor via the Interface board. The eight gain stages include Q26001 through Q26017 and all related components. When a gain stage is selected, the pin for the selected gain (1 dB, 2 dB, 4 dB, 8 dB or one of the four independent 16 dB stages) goes high. This turns on the control transistor (even Q's), which switches a bias resistor in parallel with the emitter resistor of the gain transistors (even Q's). The resulting change in emitter feedback changes the gain of the stage from unity to the stated gain.

Pins 8, 7, 6 and 5 of P25001 set control lines of 1, 2, 4 and 8 dB, respectively, and turn on Q26002, Q26004, Q26006 and Q26008. Pins 4, 3, 2, and 1 of P25001 set control lines for each of the four 16 dB stages and turns on Q26010, Q26012, Q26014 and Q26016, respectively.

Q26017 and associated components form the output stage of the IF Gain section. Its bias is controlled by a Relay (K26001). K26001 is controlled by P25001, pin 19 for the noise filter. When P25001, pin 19 is low, the relay shorts L26011 and R256049 out of the collector of Q26017 and passes the emitter output to the LOG/LIN amplifier section. When the noise filter line (P25001, pin 19) goes high, the relay switches R26049 and L26011 into the collector of Q26017 and inserts a crystal filter, 10.7 MHz, 3 MHz BW (YFL26001) into the output of the Log Amplifer. This change from emitter follower to common emitter, with a tuned collector, increases gain to compensate for the insertion loss of the crystal filter. The crystal filter is selected in 3 kHz and 300 Hz resolution bandwidths.

B. LOG/LIN Amplifiers

The voltage applied to pin 21 of P25001 selects either logarithmic (LOG) or linear (LIN) mode, depending on keyboard input. When the applied voltage goes low, the Log Amplifier mode is selected. When applied voltage goes high, the LINEAR mode is selected.

When the voltage applied to pin 21 of P25001 goes low, +12 V is applied on pin 14 of U26005A and -5.1 V is applied at U26005B. The +12 VDC biases CR26003 through CR26020 in the logarithmic portion of their response curve, causing amplifier stages Q26018 through Q26029 to amplify the 10.7 MHz IF signal logarithmically. The -5.1 VDC reverse biases CR26013, CR26014, CR26017 and CR26018, which controls the Linear Gain circuit, keeping it blocked from the amplifier circuits during log operation. Typical operation of each of the six log amp stages is as described below, for the stage including Q26018 and Q26019.

Q26018 is biased as a common base amplifier to provide current gain for Q26019. Q26019 is DC biased to +4 VDC at its emitter. When LOG is selected, +12 V forward biases CR26003 and CR26004 at the diode "knee" region to conduct through R26062, R26063 and R26064. The Log circuit is coupled into the emitter of Q26019 where it is AC biased by C26032. When the 10.7 MHz signal on the base of Q26019 increases, the emitter current increases. The current increase is initially linear; but, becomes logarithmic as CR26003 and CR26004 bias the circuit.

As the current increases, the diodes reverse bias, which limits the current. The gain is limited to 15 dB. The diode bias is unbalanced by R26063, a 14.7 K resistor, and R26064, a 16.5 K resistor, to compensate for the emitter bias being on +4 volts. The imbalance allows more upswing, which allows a larger peak to peak amplitude than a symmetrical signal would allow. CR26005, CR26006, and associate components form a Reference Line Compressor, which is adjusted by the REF LIN COMPRESSOR trimpot (R26066).

The LOG LINEARITY HIGH trimpot (R26074) adjusts the higher level log gain. Higher level IF signals are logarithmically amplified by the first few stages. The later stages are driven into LOG limiting as the input signal decreases in amplitude. When this occurs, the first few stages are amplified logarithmically. The LOG LINEARITY LOW trimpot (R26097) adjusts log linearity for lower level IF signals.

When LOG/$\overline{\text{LIN}}$ line (P25001, pin 21) goes high, U26005A switches -5.1 V to the emitter diodes of the log stages. This cuts their gain to unity, which cuts current draw, and reverse biases CR26017, which blocks output from the Log stages to the detector. The linear amp (Q26033 and associated components) gets its input from the output of the relay (K26001). Trimpot R260123 controls gain from the linear amp. Switch U26053 passes the +12 VDC to forward bias diode switch CR26018. This passes the linear amp output to the video detector.

C. Video Detect

C26067 couples the 10.7 MHz signal into a discrete differential amplifier circuit, which includes Q26030, Q26031 and Q26032. C26072 couples the amplified signal fom the collector of Q26032 to the full-wave detector (CR26021 and CR26022). The signal is then filtered (C26076, C26077 and L26010) before it is sent to pin 2 of the video amplifier (U26003A).

D. Video Amplifier

U26003 is an inverting video amplifier. The 2 dB/$\overline{\text{10 dB}}$ line (pin 25 of P25001) selects the gain of the first half of the video amplifier (U26003A) from a controlling switch (U26001A). The 2 dB OFFSET (R26156) and 10 dB OFFSET (R26151) set respective bottom of scale levels. LINEAR OFFSET (R26195) sets the bottom of scale reference at the linear base line. This adjustment is switched on by pin 3 of U26005C when the linear scale is selected. The 2 dB GAIN (R26159) and 10 dB GAIN (R26161) set their respective levels for trace display at top of scale. A DC voltage is input from the frequency-to-voltage converter of the 1st LO Sampler module to pin 3 of U26003A to provide video slope that compensates for frequency dependent losses in the RF and IF System.

E. Video Slope

Video Slope is activated in LOG mode only. In LIN mode, switch U26005B connects +12 VDC to Q26034. When this transistor turns on, the resultant 11.3 volts disables the negative voltage video slope from P25001. When LOG is selected, U26005B switches -5.1 volts to Q26034, which reverses the current to enable the video slope input. L26014 and C26080 prevent transient displays from the switch (U26005). The negative-going slope signal is input to the reference at the video amp (U26003, pin 3), producing increased video gain as the RF of the set increases.

F. Video Filters

When no video filter is selected (P25001, pin 23), switch U26001C decouples the video filter capacitors (C26081 and C26082) from the op-amp feedback, which results in U26003B being a unity gain video amp. C26092 increases video bandwidth. Pin 23 of P25001 goes high to select video filtering and sets the video filter capacitors in parallel with the feedback resistor (R26164) to activate the video filter (U26003B). The 30 kHz/300 Hz control line (P25001, pin 20) selects the capacitors and the filter bandwidth (C26081 for 30 kHz, 26082 for 300 Hz). The video filter output is sent to the VIDEO OUTPUT Connector (J25002).

2-4-6 QUASI-PEAK

The optional Quasi-peak module contains a filter board and a detector board. The Quasi-peak filter selects either a 200 Hz, 9 kHz or 120 kHz bandwidth, if Quasi-peak operation is selected, or no filtering, if the Quasi-peak option is turned off. The Quasi-peak detector uses the pulsed video signal after it has been filtered, over a prescribed time, to conduct EMI measurements.

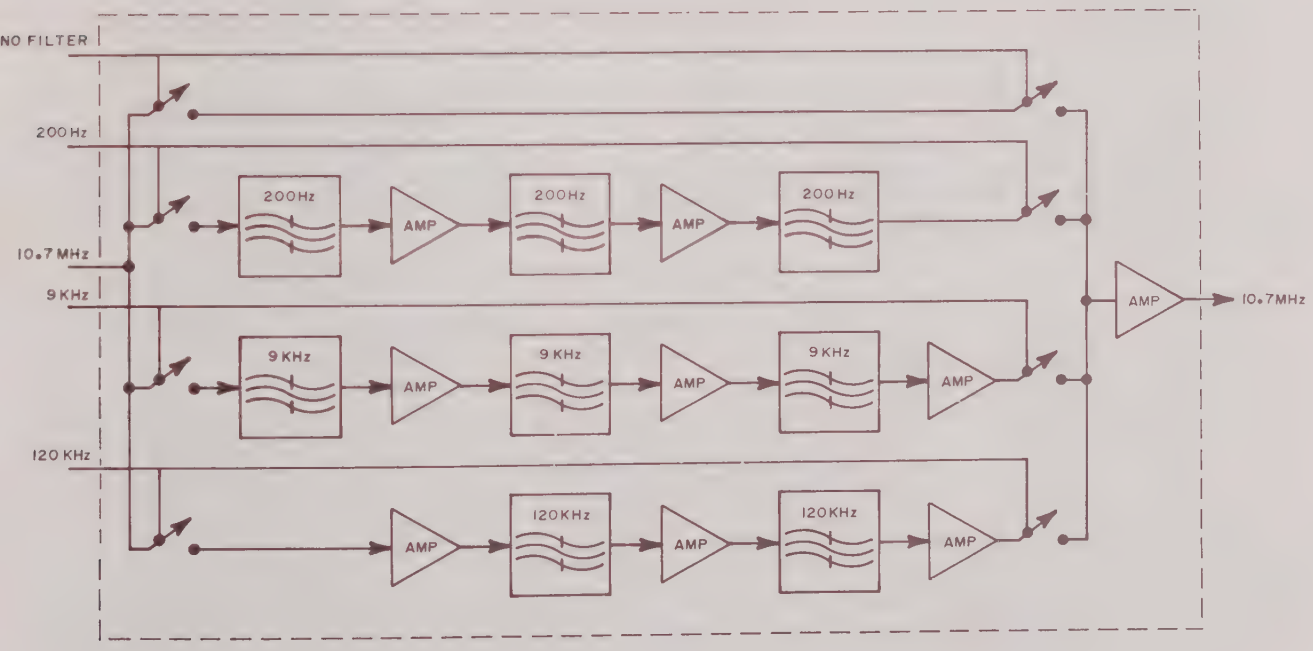


Figure 2-11 Quasi-peak Filter Block Diagram

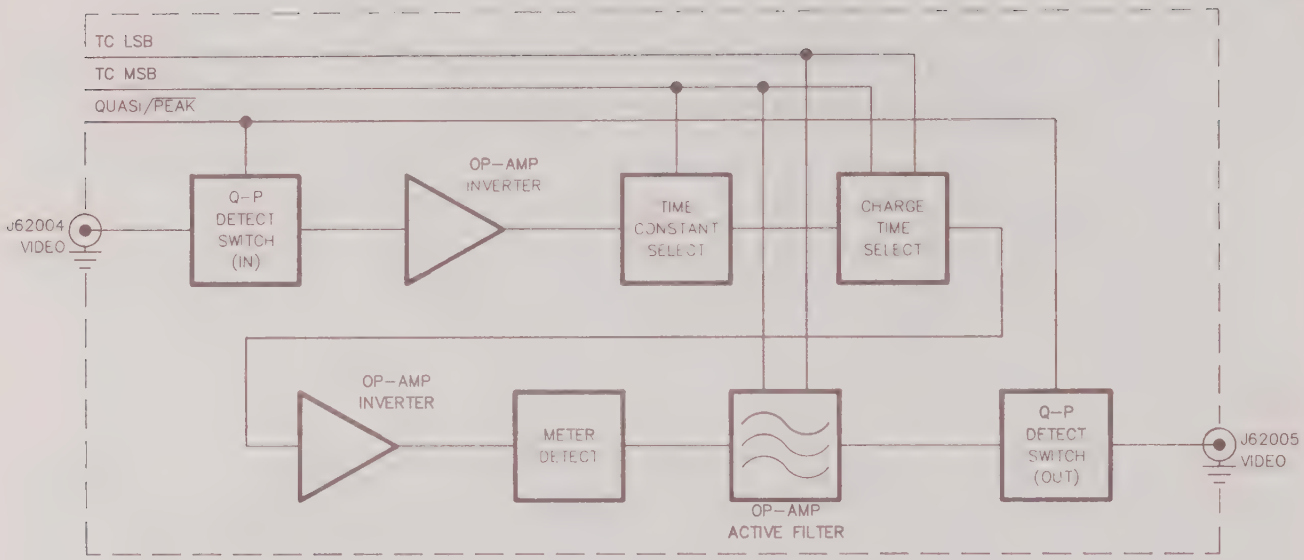


Figure 2-12 Quasi-peak Detector Block Diagram

A. Bandwidth Selection

Pin 4 of P62001 provides the least significant bit (LSB) of the Time Constant (TC1, TC2, TC3). Pin 5 of P62001 provides the most significant bit (MSB) of the Time Constant. The interaction of these two bits is shown in Table 2-5. The lines are controlled by the Control Processor and selected via menu operation.

P62001 Pin 5 (MSB)	P62001 Pin 4 (LSB)	Time Constant Selected	Bandwidth Filter (Hz)	Charge Time (ms)	Discharge Time (ms)
0	0	NONE	NONE	--	--
1	0	TC1	200	500	500
0	1	TC2	9K	1	160
1	1	TC3	120K	1	550

Table 2-5 Relationship of Bit Selection to Time Constant Variables

B. Quasi-Peak Filter

Q63009 through Q63012 are used to forward bias CR63001 through CR63008, depending on the selected bandwidth (see Table 2-5). The input signal is sent through the switch (U63001 A-B-C). Output from U63001B charges Q63012 which forward biases CR63007 and CR63008, which allows the signal to be filtered across a network of filters and amplifiers. L63011 through L63018 are adjustable inductors. R63056 is the 120 kHz ADJUST trimpot that tunes the output level. If the 9 kHz bandwidth is selected, pin 2 of U63001B charges Q63011, which forward biases CR63005 and CR63006, to allow filtering of the 9 kHz bandwidth.

C. Quasi-Peak Detector

Video enters the Quasi-peak detector at J62004, where the QUASI/PEAK signal (pin 6 of J62001) sends an inquiry to the Quasi-peak detector input (U64001C) and output (U64003C). If no Quasi-peak is detected, the signal bypasses the entire circuit (pin 5 U64001C is selected).

If Quasi-peak is detected, the signal is amplified and charged negatively (U64002A and CR64002) through R64002 and input to the Op-Amp switch (U64001B), which is controlled by TC MSB (pin 5 of U62001). If voltage is low, the signal is routed through R64004, which selects time constant 1 (TC1). If voltage is high, the signal is routed through R64003, which is used for both TC2 and TC3. C64002 applies the charge to the selected time constant and sends the charged pulse to the discharge phase. CR64002 prevents the pulse from being discharged through U64001A. The pulsed signal is controlled by TC LSB (pin 4 of J62002). If the voltage at pin 11 of U64001A is high, the signal is charged through to pin 12 of U64005A, which discharges TC1 and TC3. If the voltage at pin 11 of U64001A is low, the pulse is discharged at pin 12 of U64001A. The charge/discharge times are shown in Table 2-5. As it is discharged, the signal is sent through Op-Amp (U64002B), which allows further discharge and inverts the signal positively. The signal is filtered through the Zero Gain Active Filter (U64004A, U64003A-B and related components). If the voltage through pins 10 and 11 of U64003A-B is high, the signal is routed through pin 1 of U64003B and pin 13 of U64003A. This sets R64010 and R64013 parallel with R64011 and R64012, which reverses the charge on parallel capacitors (C64004 and C64005) and changes the discharge times of TC1 or TC3, as selected. The signal is output through U64003C to the Video Processor (via J62005) and the Rear Panel Connector.

2-4-7 10.7 MHz RECEIVER

The 10.7 MHz Receiver uses the 10.7 MHz signal from the Receive IF (optionally, via the Quasi-peak filter). The signal is filtered in the 10.7 MHz filter, demodulated, and the resultant audio routed to the speaker via the RCVR menu. The signal is controlled by the Control Processor, which selects the control lines.

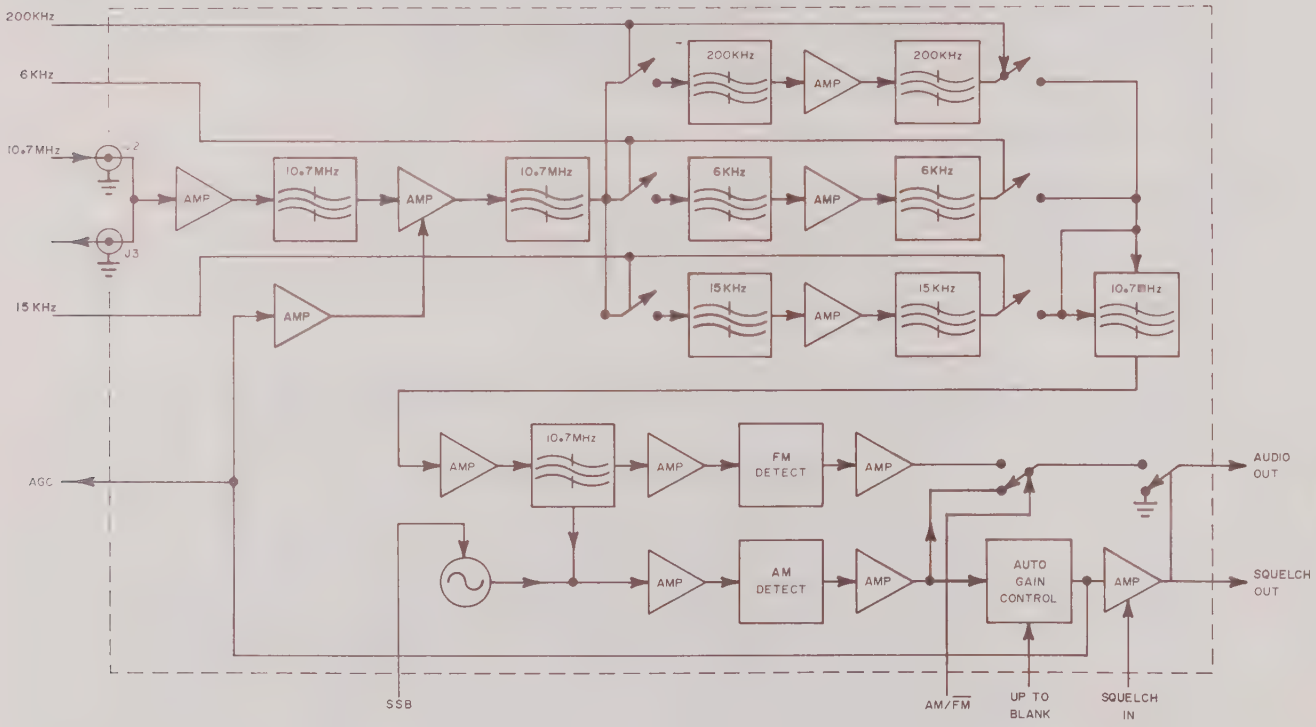


Figure 2-13 10.7 MHz Receiver Block Diagram

A. Bandpass Filter-Amplifer Circuit

The 10.7 MHz signal from the Receive IF is input (J57002) and amplified (Q58001), a gain of 20 dB, before it is routed to a coupling transformer (FL58001). FL58001 output (pin 3) is applied to gate 2 of a FET (Q58003). Pin 3 is controlled by Automatic Gain Control (AGC) signal from Q58007 and Q58008. The coupling transformer (FL58003) tunes the drain of Q58003 to 10.7 MHz. The signal is then split and filtered for 6 kHz, 15 kHz, or 200 kHz bandwidths, as selected during menu operation.

Each filter includes a switching diode, a crystal filter, an amplifier, a second crystal filter, and a second switching diode. To select any of the three filters, a +12 V bias is applied to the diodes and amplifier in the selected filter circuit.

In the 15 kHz and 6 kHz filters, the filter may be tuned by the variable capacitors, on either side of the crystal filter. FL58003 and FL58004 provide impedance matching between the filters and help suppress spurious modes of crystal operation. The band-limited signal is injected at gate 2 of the Dual-gate FET (Q58009). Gate 1 provides AGC control. The drain of the FET is tuned to 10.7 MHz and output signal is coupled by a Transformer (FL58005). The FM signal demodulating circuitry is tapped from the primary source of FL58005.

B. FM Operation

Q58010 amplifies the FM signal. CR58008 and CR58009 limit the amplitude of the IF to prevent AM signal from interfering with FM signal demodulation. The IF is coupled to a quadrature amplifier-detector (U58001), which is tuned with an adjustable inductor (L58019 and related components). The detected signal is amplified (U58002B) and low-pass filtered (R58012 and C58065). Limiting diode (CR58015) limits positive peaks to 5.3 V to prevent overloading the solid state switch (U58003C). Negative peaks can go to -12 V. When the control line for pin 11 of U58003C (which is FM/AM from pin 17 of P57001) is high, the FM detected signal is selected and passed to the output switch (U58003B). The output switch control lines are the Receiver Blanking and Squelch. If both of these are high, the detected signal passes to the Audio Out line (pin 23 of P57001).

C. AM Operation

Q58013 amplifies the 10.7 MHz signal from FL58005. The signal is coupled inductively by a coupling transformer (FL58006) in the collector of Q58013. C58076 bleeds the carrier signal to prevent overloading input to U58002A. Bias diode (CR58010) provides DC bias for the detector diode (CR58011) and, because it is the same type of diode, it changes to possess identical characteristics as the detector diode. This provides temperature compensation by keeping the detector diode properly biased under all conditions. U58002A amplifies and low-pass filters the detected audio signal. This signal is sent to U58003C, where it is passed as output when the FM/AM line is low.

D. SSB Operation

Selecting SSB (Single Sideband) operation causes pin 26 of P57001 to go high. This turns on Q58011 and switches R58075 to ground, which activates the 10.7 MHz Oscillator (Q58012, Y58001 and related components). The resulting 10.7 MHz (adjusted by trimpot R58077) is injected to the base of Q58013 with the SSB signal onto the AM path from FL58005. This provides a reference for the AM Demodulator, which allows SSB information detection.

E. Receiver Blanking

Q58015 is turned on when the REC BLANK line (pin 3 of P57001) is high. Q58015 puts the Automatic Gain Control (AGC) system into hold status by opening the circuit at U58003B and pulls low on the output enable switch (U58003B), disconnecting the output line. When the REC BLANK line is low, Q58015 is off and the +5 V through R58090 switches the detected signal into the AGC circuit through U58003A. This line also causes CR58014 to reverse its bias, which allows the squelch circuit to control the output enable switch (U58003B).

F. AGC Operation

R58088 and R58089 divide +12 VDC to provide 1.09 V reference to U58004A. When the detected signal level from U58002A is lower than 1.09 V, the Op-Amp (U58004A) integrates in a positive direction. U58006C, a switch controlled by the FM/AM line, controls the change rate. The integrator capacitor in FM is C58078. A larger capacitor (C58079) is selected for AM or SSB operation. This provides slower AGC operation. To adapt to SSB's lack of carrier, the SSB line also turns on Q58014. Otherwise, the AGC circuit would not include a carrier level for signal detection.

When Q58014 is on, the AGC attack time becomes faster than normal AM or FM operation. This signal passes through R58086 and CR58012. The decay becomes slower because CR58012 blocks the signal flow. During normal operation, the attack and delay times are one, going through R58008 only.

The output of U58004A and U58005A rise at the same time, causing the controlling diode (CR58013) output to be directed into pin 2 of U58004A. This realizes a voltage increase and causes U58004A output to drop, thus, producing feedback which prevents the AGC output from going above 0 V.

When the detected signal level at pin 2 of U58004A goes above 1.09 V, the op-amp integrates towards -12 V. When the AGC line goes negative, it pulls down on the emitter of Q58008. The collector of Q58008 is also pulled down as Q58008 and Q58007 are biased on by R58048, R58049 and CR58007. The negative pull of the emitter controls the amount of the collector drop. The collector of Q58008 is connected by R58051 to gate 1 of Q58009. Pulling gate 1 lower causes Q58009 output to decrease, decreasing the gain of the 10.7 MHz signal. As the collector of Q58008 pulls down on the emitter of Q58007, the Q58007 collector voltage drops, losing the bias on gate 1 of Q58003 and reducing the gain on Q58003. This arrangement allows the later stage of the Amplifier (Q58009) to become saturated, causing it to be reduced first. Increasing the input signal levels cause the earlier AGC controlled stage (Q58003) to reduce its gain as well.

G. Squelch Operation

Squelch control is set on the Front Panel. Squelch level is coupled to U58004B via R58094, R58095 and R58099. Increasing the squelch level above the level of the AGC voltage causes the comparator (pin 7 of U58004B) to go high and switches U58003B to pass the audio to the output connector. Dropping the input signal increases AGC voltage to a level greater than the squelch level. This causes comparator output (U58004B) to be low, opening the switch (U58003) and blocking audio output.

H. Time Share Reception

During Time Share Reception (TSR) operation, the receiver is blanked during sweep trace. This allows intermittent audio reception and sweep trace viewing.

2-4-8 SWEEP DIGITIZER

Sweep Digitizer functions include taking digital samples, generating the sweep waveforms for the RF System, and producing traces for the CRT display. Timing diagrams are included in Section Five.

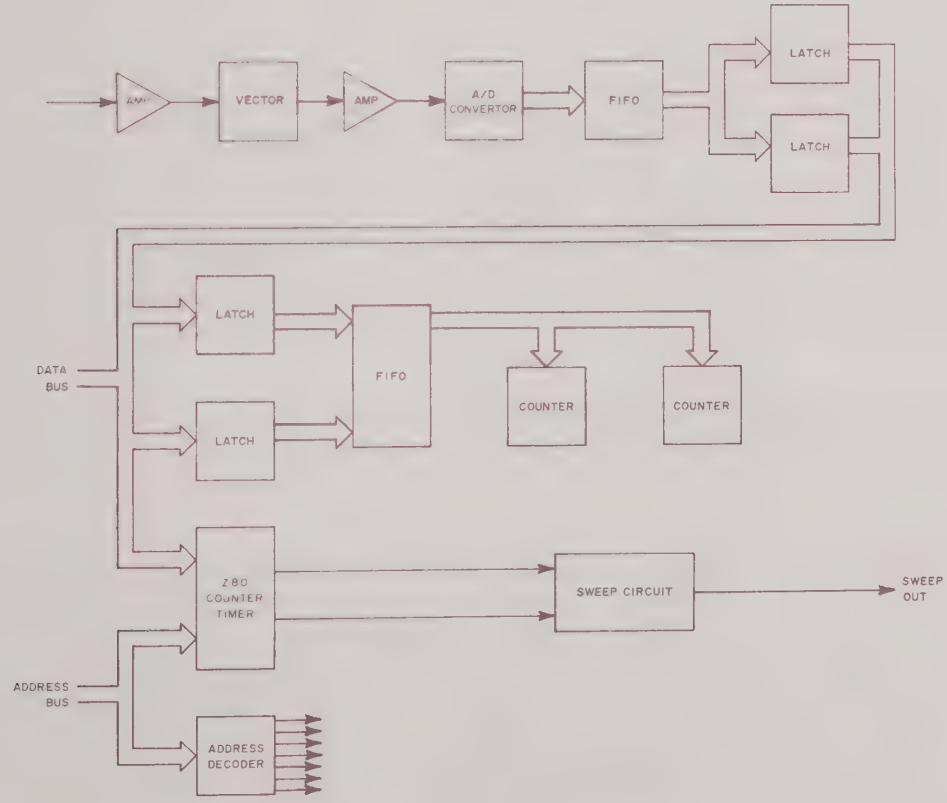


Figure 2-14 Sweep Digitizer Block Diagram

A. Sample Circuit

Video from the Log Amp enters the Sweep Digitizer at J32003, where it is low-pass filtered (R32005 and C32019). U32016A charges C32025 through CR32003 and R32003 to the positive signal peak occurring in each sample interval. This peak is sampled by the sample-and-hold chip (U32017). After sampling, Q32001, driven by a negative-going pulse on the base of Q32002, discharges C32025 into C32019 to about -0.7 VDC. This clears the sample circuit for the next sample. U32017 output is fed through U32028A to the ten-bit analog-to-digital converter (ADC), U35010. The data is fed into a 512-by-9 bit first-in/first-out (sample FIFO) memory (U32005). The "write" time of Sample FIFO memory is the same as the sample interval rate. The Control Processor reads the data as time allows. U32023 (A and B) operates as two monostable multi-vibrators to provide proper sequencing to the sampling and digi-tizing processes.

B. Sweep Circuit

When a sweep is required, the Video Processor sends a "start" com-mand to the Sweep Digitizer. U32006 decodes the command and sets the state of the flip-flop (U32018 C and D). U32018D releases the clear signal to the 12-bit counter (U32024, pin 11). The counter increases when the negative edges of the ramp clock pulses are detected (pin 9 of U32011). U32024 is incremented twice per sample interval, producing a digitized ramp. A ten-bit digital-to-analog converter (DAC - U32025) produces a ramp current that feeds the current-to-voltage converter (U32026A). The sweep ramp is Low-pass filtered (R32026, R32027, C32044 and C32045) and output via J35002 to the Interface board. THe Video Processor generates a "stop" command, which resets the nand-gate flip-flop. This results in U32024 being pulled high, which stops the counter. The clock rate (U32011, pin 9) is determined by the sweep rate selected on the front panel by U32011, a counter-timer controller IC.

NOTE: The "stop" command may be generated at any indefinite time after the last sample is taken.

C. Trace Circuit

Trace circuit display consists of a series of vertical line segments. Each segment is produced when an electron beam is turned on and off at particular intervals. The Video Processor batch loads 9-bit digital values into a 512-by-9 bit first-in/first-out (display FIFO) memory (U32008) in on-off-on-off sequence. The BCUR signal from the Video Processor generates an interrupt (TINT) in the Sweep Digitizer that is sent back to the Video Processor at the end of each displayed field. The Video Processor then loads all values for the next field to be displayed.

U32009A generates the $\overline{\text{TINT}}$ interrupt that is reset by $\overline{\text{3 CW}}$. U32009A tells the Video Processor which field to load. U32003 and U32004 convert 8-bit data into 9-bit words. U32014/U32015 and U32020/U32021 are configured as 9-bit down counters.

D. Counters

The first counter to reach zero stops counting and turns the trace on. When the other counter reaches zero, it stops counting and turns the trace off. U32012A and U32012B stop their respective counters; U32013 and U32027 provide timing signals for loading and enabling the counters. U32022 delays the U32014 and U32015 count by one clock pulse and delays the U32020 and U32021 count by five clock pulses. (The counters are loaded at different times.) U32018B and U32019C generate the trace from the signal produced by the counters and delay elements. The trace is a TTL-level signal sent to the Video Processor for gating and analog level adjustment.

2-4-9 VIDEO PROCESSOR

The Video Processor communicates with the Control Processor and Sweep Digitizer to develop displayed video signals.

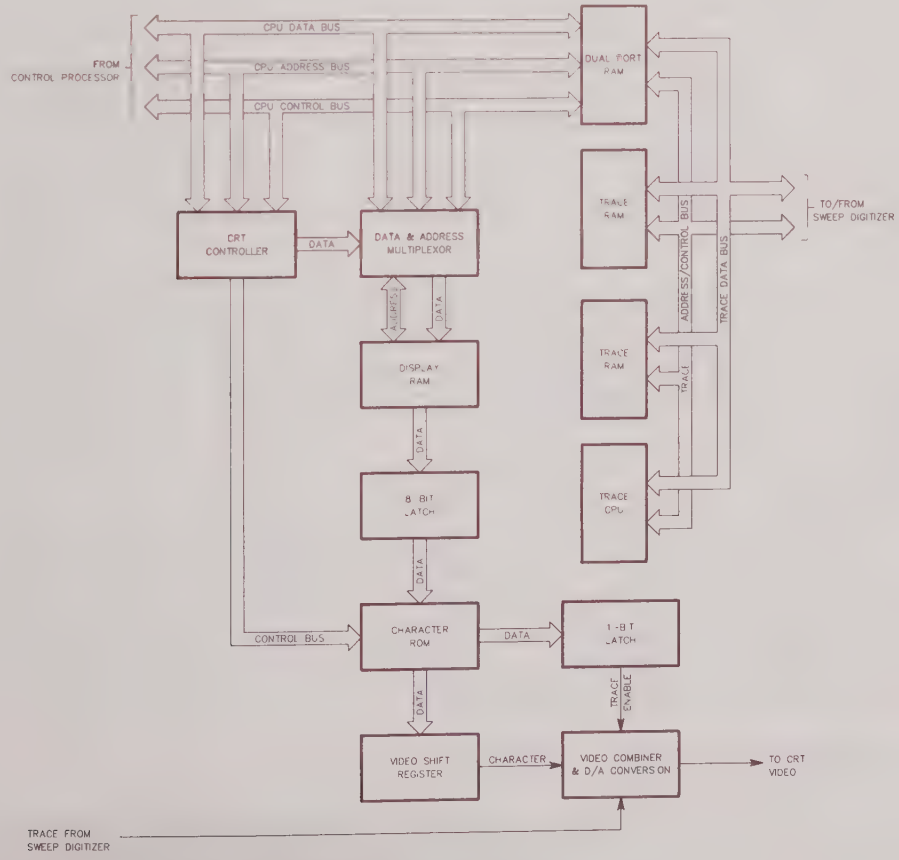


Figure 2-15 Video Processor Block Diagram

A. A-7550 Display

The A-7550 uses interlaced Vertical Raster Scan (VRS - VRS is a registered trademark of IFR Systems, Inc.) with a seven-inch electromagnetic-deflection monochrome CRT. The display operates in a manner similar to, but not compatible with, standard broadcast video. The deflection yoke in the CRT is rotated 90° counter-clockwise from standard video, and scanning frequencies are higher. In interlaced scan, alternate fields produce video, timed to position the lines of one display field midway between the lines of the other display field. Waveforms for the Video Processor are included in Section 5.

B. Character Display

The character display section of the Video Processor displays alphabetic and numeric characters. The graticules are special display characters. The CRT Controller (CRT-C - U31007) is the heart of the character display section. It provides address information during display RAM "reads", and synchronizes CRT and trace section signals.

When the Z80 microprocessor in the Control Processor (U20004) writes information into Video Processor Display RAM (U31009), it supplies memory addresses to the Display RAM through data selectors (U31001, U31002 and U31003) on the Video Processor. Memory addresses can be supplied from the CRT-C (U31007) when the Control Processor is not writing information. U31002 latches Display RAM output and selects the appropriate character from ROM (U31008). Character ROM output is seven bits. Six bits are input to video shift register (U31001O) and output to the video combiner (U31027). The other bit identifies a graticule character and is output to U21012B.

U31011, U31021C, U31021D and U31022B provide timing signals for Display RAM, latches and shift registers. The Display Enable (DE) signal from the CRT-C (U31007) is delayed in U31029 for use in the Sweep Digitizer. Characters are arranged as 6 x 13 pixels in U31008.

C. Trace Display

Most of the Trace Display section is on the Sweep Digitizer PC board. The trace uses its own microprocessor system (U31004, U31009 and U31017 through U31020). U31017 is also used as temporary storage for trace information. Dual-port RAM (U31019) buffers commands and information between the Trace microprocessor system and the Control Processor.

D. Video Combiner and Video Output Section

The graticule bit (pin 5A of U31002) must be set before traces can appear over characters on the video. This section is controlled by U31027, U31021A, U31021B and U31026E.

Q31001, Q31002 and associated components form a differential amplifier for graticule video. The GRATICULE Adjust pot (R11002) on the Front Panel adjusts current flow, which adjusts the gain of the graticule video amplifer. Q31003, Q31004 and associated components operate in a similar manner for the trace and non-graticule characters.

The collectors of Q31002 and Q31004 have a common load resistor (R31012), which combines the dual output. U31012A, U31022A and Q31005 are microprocessor controlled, and serve to shunt part of the video signal to ground. Otherwise, the display would be too bright to comfortably view in some display modes.

U31025 buffers the clock and synchronizing signals for the Sweep Digitizer, CRT and CRT Controller (U31007).

2-4-10 CONTROL PROCESSOR

The Control Processor serves as the master controller of the A-7550 Spectrum Analyzer. It controls communication between the Interface PC board and the Video Processor PC board, the keyboard and either the GPIB or the RS-232C option (if either option is installed).

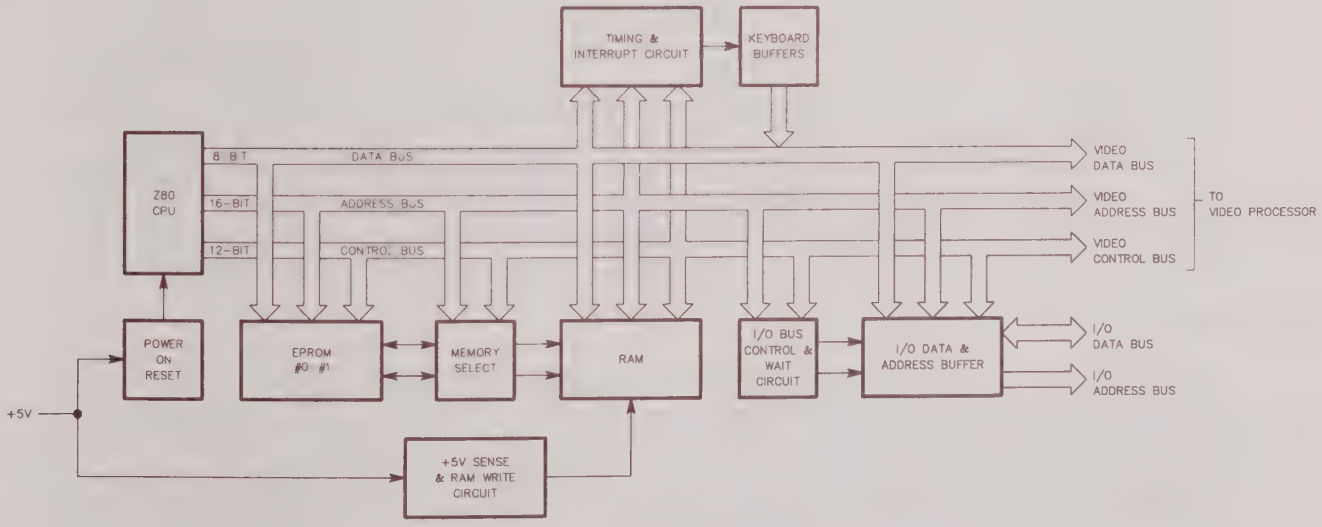


Figure 2-16 Control Processor Block Diagram

A. Central Processing Unit (CPU)

Communication to and from the Control Processor uses an 8-bit data bus, a 16-bit address bus and a 12-bit control bus. U20005 through U20008 are the bus buffers for the CPU (U20004). U20023C and U20023D control the direction of the data bus. A 5 MHz system clock is input at pin 27B of P20001. U20025C and U20025B buffer the clock, which is then referred to as Φ_1. Φ_1 is further buffered through U20008 to become Φ_2. Φ_2 is used to clock the CPU and CTC (U20017).

B. Memory

PROMs (U20009 and U20011) are the processor's memory. RAM (U20012) holds data in memory after the A-7550 Spectrum Analyzer is turned off, to make it available at power-up. The lithium battery (BT20001) provides approximately +3 V, which is sufficient to hold the contents of the RAM valid, even though +3 V is insufficient for reading and writing.

C. +5 V Sense and RAM Write Circuit

Differential Amplifier (Q20002 and Q20003) detects a power off condition by monitoring the +5 V line. When the ouput of Q20002 goes below approximately +4.7 V, Q20004 and Q20005 turn off. This prevents the active low signal from pin 12 of U20010 from reaching U20012, which prevents any data in the RAM from being accidentally changed. When the +5 V line drops below approximately +3 V, CR20002 is reverse biased and CR20003 is forward biased to allow the lithium battery to power RAM ("standby" or "power off" mode). The +5 V line is also monitored by U20025B and U20025E for power on reset. When the set is first powered up, the gates change states to activate the RESET line. When the set is first powered up, the gates change states to activate the RESET line. When the set is powered down, or when C20001 is fully charged, the RESET line is inactive (high). The RESET line resets the CPU and CTC.

D. Memory Select

When MREQ is active and RFSH are inactive, the memory select IC (U20010) selects one of the memory devices according to address lines A13, A14 and A15.

E. Timing and Interrupt Circuit

The timing and interrupt circuit includes CTC (U20017), decoder (U20014) and interrupt lines. U20014 decodes six address lines, and the M1 and IORQ control lines. The decoded output can enable U20015, U20016, U20017 or the Interface Bus Control Circuit. When U20015 is enabled, data corresponding to the eight horizontal rows on the keyboard are read onto the data bus. When U20016 is enabled, data corresponding to the four vertical columns on the keyboard are read onto the data bus. The interrupt signals sent to the CTC tell which device has been interrupted.

F. Interface Bus Control and Wait Circuit

The interface address lines are buffered (U20021 and U20022) for output to interface devices. Bi-directional buffers (U20019 and U20020) control the data flow to or from the interface devices. A wait circuit is provided because devices on the buffered buses require longer setup times than devices tied directly to the Z-80 bus. U20013, U20024C, U20024D and U20026 (A, B and C) form the wait circuit, which has a 3 μS time-out period. After the wait circuit times out, the Z-80 CPU finishes the current machine cycle and tristates U20014. On the next rising edge of the clock signal, U20018B is set, which tristates the interface data bus. The interface address bus is tristated when U20014 is not selected.

2-4-11 GENERAL PURPOSE INTERFACE BUS (GPIB)

GPIB (IEEE Standard 488-1978) is the means for communication between an external GPIB controller and the A-7550 Spectrum Analyzer.

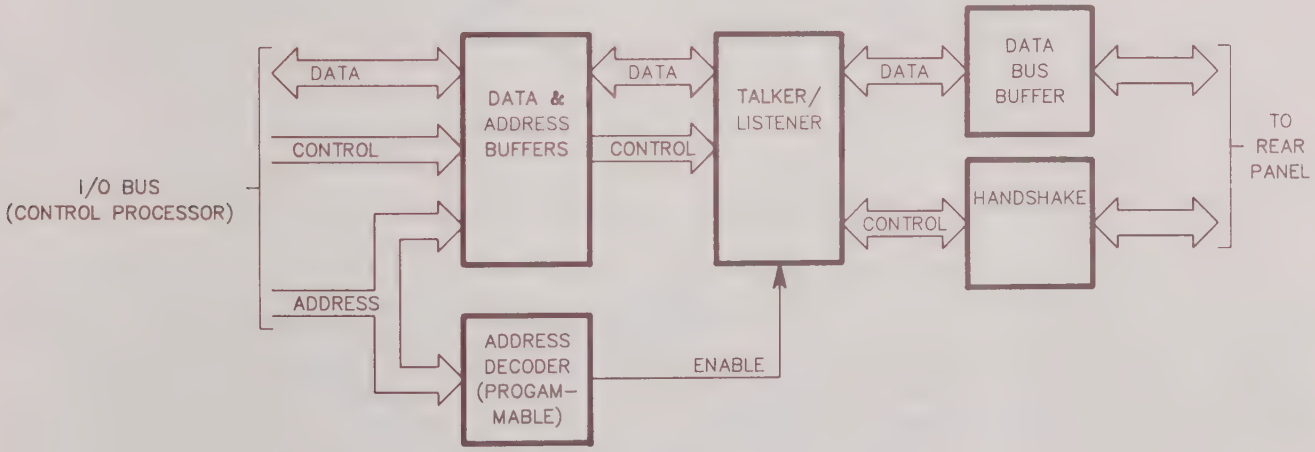


Figure 2-17 GPIB Block Diagram

U56001 is a bi-directional buffer for data sent to and from the Control Processor. U56002 is an input buffer for address and control lines from the Control Processor. U56003 is a decoder used to control data transmission and is the enable line of U56006. U56006 performs the "housekeeping" operations for the GPIB. U56007 through U56010 are bi-directional buffers.

2-4-12 RS-232C INTERFACE PC BOARD

The RS-232C interface is the means for communication between an external RS-232C controller and the A-7550 Spectrum Analyzer.

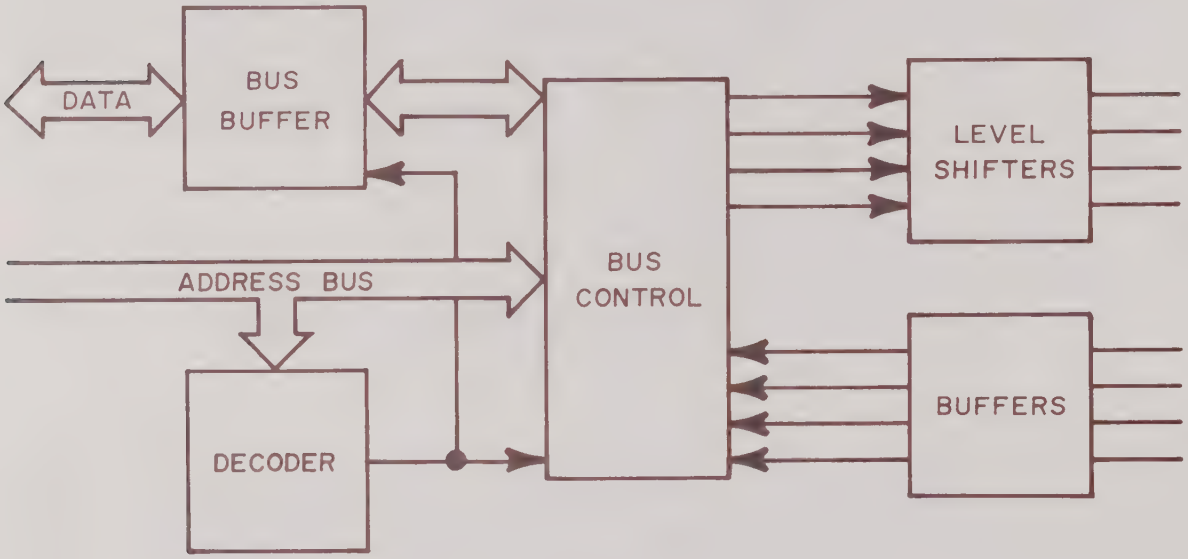


Figure 2-18 RS-232C Interface Block Diagram

U55001 is a bi-directional buffer for data sent to and from the Control Processor. U55002 is a decoder used to control data transmission. U55004 is an asynchronous interface adapter used to convert data from parallel format to a serial format in transmittal mode, and converts data from serial to parallel format in receiving mode. U55004 and U55007 perform level shifting. U55006 is a bi-directional data buffer.

2-4-13 INTERFACE PC BOARD

The Interface distributes analog and digital information throughout the unit. Discrete lines which control the RF section are routed to the RF Motherboard. Sweep adjustments and discrete digital input to the Control Processor are also located on this board.

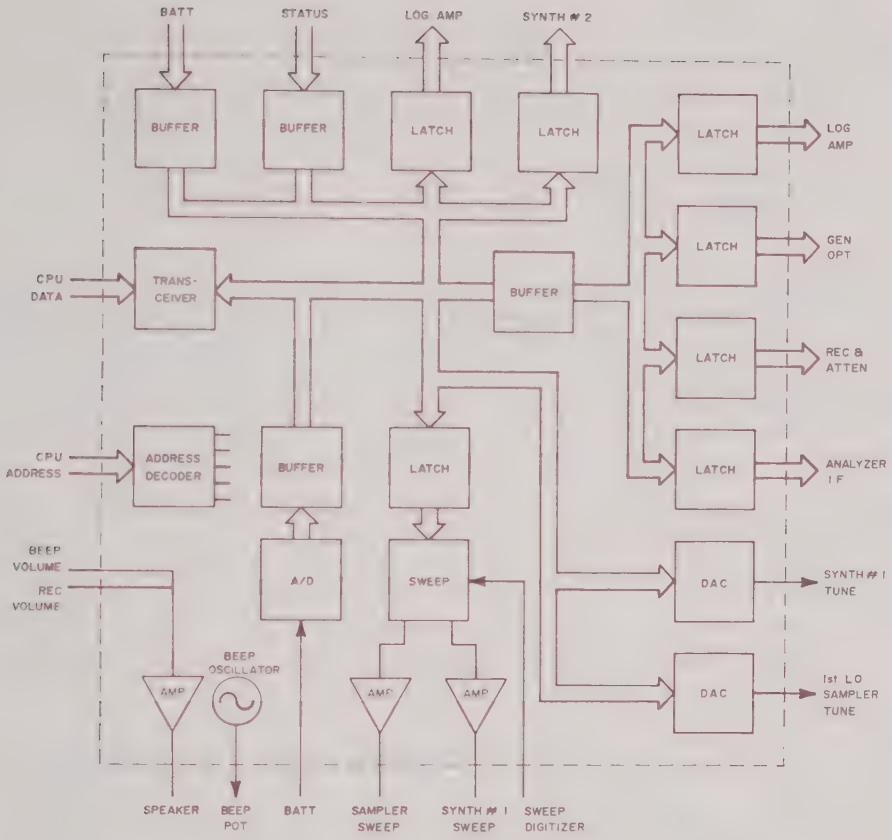


Figure 2-19 Interface PC Bd Block Diagram

U19011 and U19012 are TTL PROMs which use look-up tables to translate address lines from the Control Processor into Read/Write Enable lines for the Interface board. U19013 is a tristate transceiver that reads from or writes to the processor bus. U19001 and U19008 are read buffers for U19013. U19007 is an analog-to-digital converter (ADC) with adjustment points for +5 V BATTERY REFERENCE (R19029) and +7.5 V BATTERY CALIBRATION (R19030).

U19002 and U19003 are Digital-to-Analog Converters (DAC's), which develop the coarse tune voltages sent to the first LO Sampling Loop and to Synthesizer #1, respectively. SAMPLER GAIN adjustment (R19005) sets the high end sampler course tune voltage. SAMPLER OFFSET adjustment (R19009) sets the low end sampler course tune voltage. The SYNTH #1 GAIN adjustment (R19007) adjusts the high end coarse tune voltage. The SYNTH #1 OFFSET adjustment (R19013) adjusts the low end Synthesizer #1 coarse tune voltage.

Sweep input from J19005 is divided by the resistor network (R19016 through R19020) and U19004. When the Scan Range is selected between 1 kHz/Div and 1 MHz/Div, SYNTH #1 SWEEP (pin 31C of P19002) is enabled by U19005B. When the Scan Range is selected for 2 MHz/Div and above, SAMPLER SWEEP (pin 31B of P19002) is enabled by U19005A. The SAMPLER SWEEP GAIN adjustment (R19024) and SYNTH #1 SWEEP GAIN adjustment (R19021) provide sweep ramp amplitude adjustment for their respective sweep ramps.

U19018 and U19019 form a tone oscillator that is driven whenever an entry from the keyboard is accepted. This prompts the annunciator tone. U19023 is the audio amplifier which is driven by the annunciator of the demod audio from the 10.7 MHz receiver. A jumper block (JTB19001) is provided to disable Autocal when calibrating the A-7550 Spectrum Analyzer. The remaining components are control line latches to the various modules throughout the A-7550 Spectrum Analyzer.

2-4-14 REFERENCE OSCILLATOR

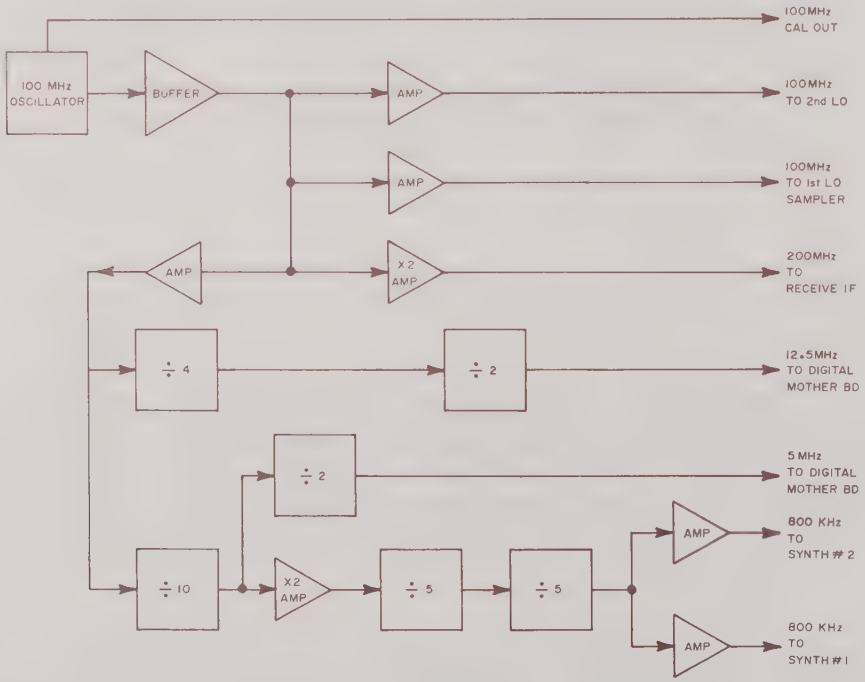


Figure 2-20 Reference Oscillator Block Diagram

Q47001, Y47001 and associated components form the 100 MHz Oscillator for the 100 MHz time base. Coil L47002 sets the frequency of the 100 MHz time base. CR47001 and C47002 form a peak detector for differential amp (Q47002, Q47003 and R47005), which is a level controller for the oscillator. CR47002 is needed for temperature compensation for CR47001.

If the detected peak voltage on Q47002 is less than the bias voltage of 1.3 VDC on Q47003, then Q47002 is turned off, increasing the bias voltage which increases AC Gain of Q47001. When the detected peak voltage is greater than the bias voltage of 1.3 V at Q47003, then Q47002 is turned on, reducing the AC Gain of Q47001.

Q47004 isolates the 100 MHz oscillator from the output buffers. Q47005 provides further isolation in the 1st and 2nd LO references. Q47014 buffers the 100 MHz output to the 2nd LO block (J46002). Q47006 buffers the 100 MHz output to the 1st LO SAMPLER (J46004). The collector of Q47007 is tuned by adjustment inductor (L46005 and associated components) to 200 MHz for the 3rd Mixer in the RECEIVE IF (J46003). C47014 through C47025 and L47006 through L47012 form two filter networks for the 200 MHz (3rd) LO. The first section is a bandpass filter and the last section is a low-pass filter. Q47008, Q47009 and Q47013 buffer the 100 MHz to the reference divider circuits.

Trimpot R47025 adjusts the 100 MHz CAL OUTPUT level to the front panel. R47026 and R47027 set the output impedance at REF CAL OUT (J46009). U47001 is a dual flip-flop circuit which divides the 100 MHz by four. The resulting 25 MHz is converted to TTL with R47034, R47035, R47036 and C47043. U47003 divides the frequency by two, which results in the 12.5 MHz clock supplied to the Video Processor (J46008).

U47002, U47004 and related components form a Divide circuit which produces several references used for various A-7550 functions. The 100 MHz signal is divided by five in U47002, which results in 20 MHz. An on-board circuit converts the signal to TTL levels. U47004 divides the 20 MHz TTL by four to produce the 5 MHz clock to the Video and Control Processors (J46007). U47004 doubles as a divide-by-25 circuit (two divide-by-five stages) to produce the 800 kHz reference. The 800 kHz is split and sent to Q47010 to drive Synthesizer #2 (J46005) and sent to Q47011 to drive Synthesizer #1 (J46006).

2-4-15 1ST LO SAMPLER LOOP

The 1st LO Sampler Loop module uses frequency-to-voltage conversion, coarse tune sweep and phase lock voltages to develop a slow tune voltage used to steer the 1350 to 2350 MHz VCO frequency. It also uses the VCO frequency with a reference frequency to develop a fast tune voltage, used for VCO phase correction.

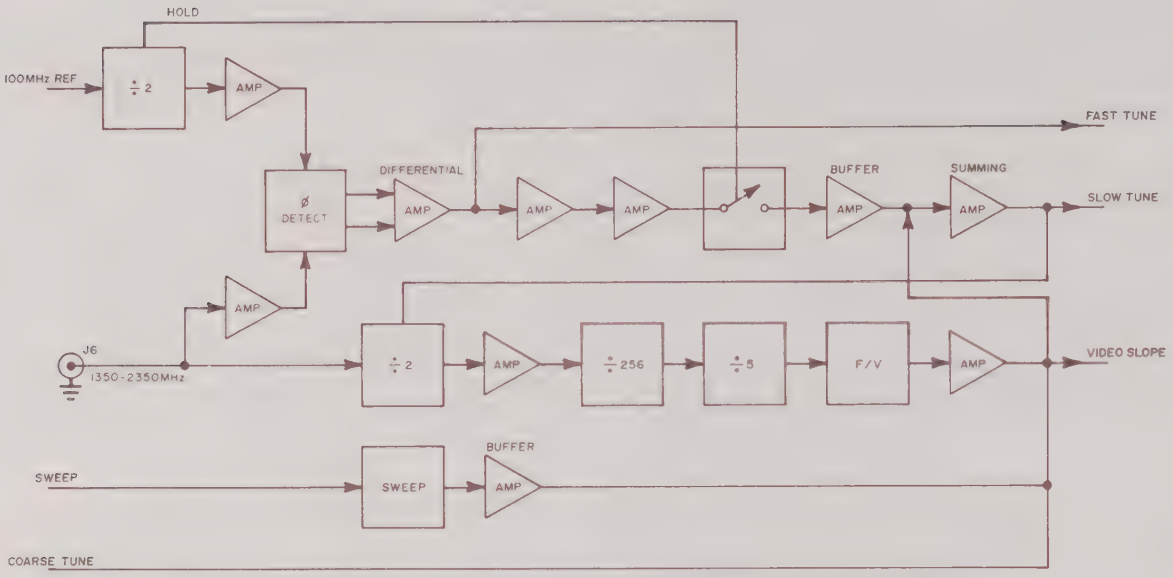


Figure 2-21 1st LO Sampler Loop Block Diagram

A. Fast Tune Voltage

The frequency from the VCO that enters the 1st LO Sampling Loop at J29006 is used for high speed sampling to create the Fast Tune Voltage. The 100 MHz reference frequency is input at J29003 and passed to U30011, which divides the frequency by two. If the HOLD line (pin 1 of P29001) is low, output at U30011 is disabled. Otherwise, Q30020 amplifies the 50 MHz reference from U30011 to drive CR30012, a step recovery diode, which produces 50 MHz harmonics. Q29019, CR29013, CR29014 and associated components form a level controller for Q29020. Harmonics are mixed through diodes (CR30010 and CR30011) to sample the VCO phase. The Differential Amplifier (Q30015 through Q30018) amplifies the sampled DC phase lock voltages. The SAMPLER OFFSET trimpot (R30070) adjusts the low end phase lock voltage. The collector of Q30017 drives U30012A and the fast tune output which cleans the VCO signal. R30081 adjusts the SAMPLER GAIN before the signal goes to the VCO (J29005). C29074 and L29016 form an adjustable 50 kHz trap.

B. Slow Tune Voltage

The fast tune voltage is integrated (U30013B) and switched (U30008A). During sweep mode, the HOLD line is low to open the switch (U30008A) and the slow tune phase lock voltage is held by C30072. If the VCO signal is not locked on a multiple of 50 MHz, U30012A output oscillates at about 100 Hz before it is buffered through U30012B. This oscillation causes the VCO voltage to vary 20 MHz so the sampler can lock into the proper 50 MHz harmonic.

The voltage summation point for the slow tune line is pin 2 of U30010A. U30012B output, the frequency-to-voltage converter (Q30004, Q30005 and related components), the coarse tune input (J29002) and sweep signals (pins 3 and 5 of J29002) are summed to create the slow tune voltage.

Sweep input enters at pin 3 of P29001 and is divided by ten if the scanwidth is 1 MHz/Div or less. The microprocessor controls the sweep to ensure its presence only after the synthesizers have been locked at the left-lock frequency and the scanwidth is 2 MHz/Div or greater.

The digital-to-analog conversion performed by the Interface PC board determines the coarse tune voltage entered at J29002. The VCO frequency enters at J29007, where it is divided by a regenerative divide-by-two circuit. This circuit contains a mixer (MXR30001), series resonant circuit (CR30001, L30001, and C30005) and an amplifier (U30001). The series resonant circuit produces a 90° phase shift signal which is fed into the Mixer IF port at one-half the input frequency. A varactor (CR30001) and the slow tune circuit form a tracking filter that steers the mixed frequency output to one-half the input frequency. Next, the VCO signal is divided by 1280 across a series of divider chips (U30002 and U30003). Q30006 and Q30008 transform the signal into a sharply defined square wave. C30029 and R30022 transform the square wave into pulses. The negative-going pulse is limited by Zener diode (CR30004). The positive-going pulse turns on Q30009, causing a current through R30024. R30110, R30111, C30033, C30079 and C30034 form a low-pass filter to average the voltage developed across R30024. The frequency-to-voltage converter output is also sent to the Log Amp (P29001, pin 25), where it supplies compensation to the Video Amp.

The resultant tune voltage from U30010A is integrated (U30009B), which pulls down on the emitter (Q30013) and conducts to vary the slow tune line output from 0 to +30 V. Q30010 operates as a current limiter on the +40 V tune supply. The HIGH LIMIT (R30045) and LOW LIMIT (R30049) trimpots set the maximum and minimum slow tune voltages for the VCO. The summed tune voltage is fed back through U03009A, where it is adjusted by the DIVIDER TUNE OFFSET (R30032) and the DIVIDER TUNE GAIN (R30033) trimpots. These set the amplifier level for tuning the regenerative mixer-divider circuit. The adjusted slow tune voltage is output to the VCO Filter (J29004).

2-4-16 1350-2350 MHz VCO

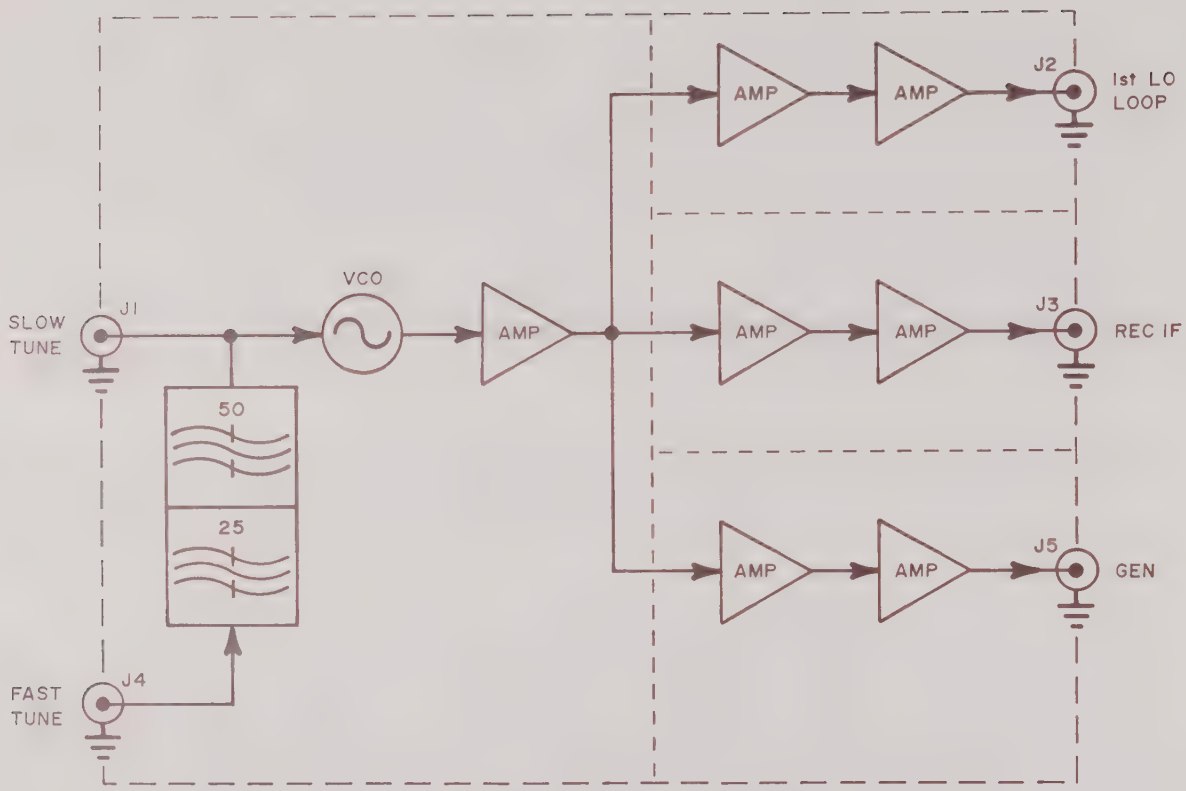


Figure 2-22 1350-2350 MHz VCO Block Diagram

The 1350-2350 MHz VCO develops the RF signal source for the 1st LO mixers and 1st LO Sampler Loop module. J39001 and J39004 are, respectively, the slow tune and the fast tune voltages developed in the 1st LO Sampler Loop. The fast tune voltage is filtered by 25 MHz and 50 MHz notch filters (L40010, L40002, L40003 and related components), to suppress modulation of the VCO. A varactor-tuned oscillator (G40001) is used to combine the tune voltages into a 1300 to 2350 MHz frequency. The oscillator frequency is amplified and sent to three output stages for further amplification. The output at J39002 is sent to the 1st LO Sampler Loop. Output at J39003 is sent to the Receive IF module. Output at J39005 is sent to the optionally installed Generator module.

2-4-17 SYNTHESIZER #1

Synthesizer #1 uses coarse tune and sweep voltages from the Interface PC board and an 800 kHz reference to develop a phase-locked VCO frequency.

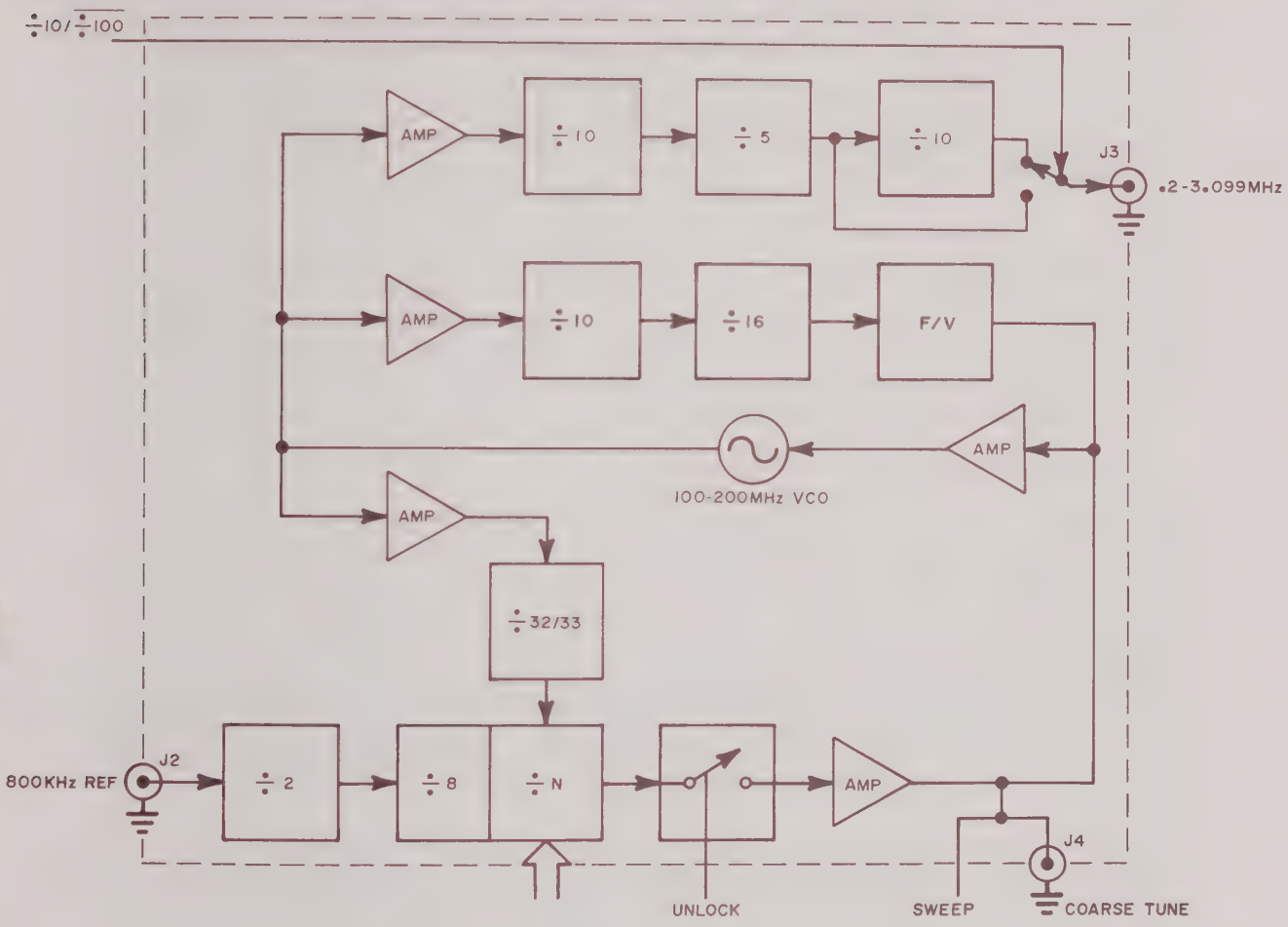


Figure 2-23 Synthesizer #1 Block Diagram

A. 50 kHz Loop

The 800 kHz reference from the Reference Oscillator is input at J23002 and divided by two (U24008B). This phase locks the 100 MHz to 200 MHz on-board VCO with a 50 kHz reference using serial data from the Control Processor. U24010 divides the 400 kHz signal by eight to produce the 50 kHz reference.

A dual modular prescaler (U24009) receives a 100 to 200 MHz signal from the VCO (CR24003, Q24001, Q24002, L24001 and related components) that is amplified by Q24005. The state of the modulus control (MC - pin 1 of U24009) is a divide-by-32/divide-by-33 circuit. This is controlled by U24010. Pins 3 and 4 of U24010 are the phase detector outputs. They charge or discharge C24042 through C24010 and C24011, depending on the signal phase difference.

The resulting error voltage goes to switch U24012A, where it is passed when the signal locks. This voltage is blocked as Synthesizer #1 sweeps. These actions are controlled by an unlock signal from the Control Processor (pin 20 of P23001). When the unlock signal is low, U24012B is open, which allows +5 VDC to pull U24012A on. This passes the error voltage, which closes the phase lock loop and puts it into lock condition. When a Synthesizer #1 sweep is required, the Control Processor pulls the "unlock" line high. This switches on U24012B and places its control low to open it during the Synthesizer #1 sweep, preventing the phase lock loop from pulling the currently sweeping frequency back to a locked condition.

When the phase lock loop locks, pin 9 of U24010 goes high and turns off Q24010. This sends a "locked" signal to the processor via pin 22 of P240001. When the loop unlocks, pin 9 of U24010 goes low, which turns on Q24010 and illuminates the LED (DS23001). This indicates an unlock condition and sets the Synthesizer #1 lock (pin 22 of P23001) low.

B. Frequency-to-Voltage Converter

The VCO frequency is divided by 10 (U24004) and by 16 (U24005) before the signal is transformed into a sharply defined square wave (Q24006, Q24007 and related components). The square wave is transformed into pulsed signals (C24022 and R24028). The negative-going pulse is limited by Q24008, the positive-going pulse turns on Q24009, producing a current through R24033. A low-pass filter (R24061, R24035, C24025, C24026 and C24014) averages the voltage developed across R24033. The frequency-to-voltage (f/v) converter output from U24007B is then summed with the other control voltages at pin 2 of U24007A.

Coarse tune voltage and sweep voltage, both from the Interface PC board, are also summed with the frequency-to-voltage correction and phase lock error voltage at U24007A. The Control Processor sends sweep input and "unlock" signals to Synthesizer #1 only after the synthesizers have been locked at the left-lock frequency and the scan range is between 1 kHz/Div and 1 MHz/Div, inclusively.

The VCO output is divided by ten (U24001) and by five (U24002). If ÷10/÷100 (pin 7 of P23001) is high, the second divide-by-ten circuit (U24006) is bypassed; otherwise, if ÷10/÷100 is low, the frequency is again divided by ten. The resultant 0.2 MHz is a 3.099 MHz TTL signal which is sent to Synthesizer #2 (J23003).

2-4-18 SYNTHESIZER #2

Synthesizer #2 uses Synthesizer #1 output and an 800 kHz reference to develop a phase-locked VCO frequency output as part of the 2nd LO source.

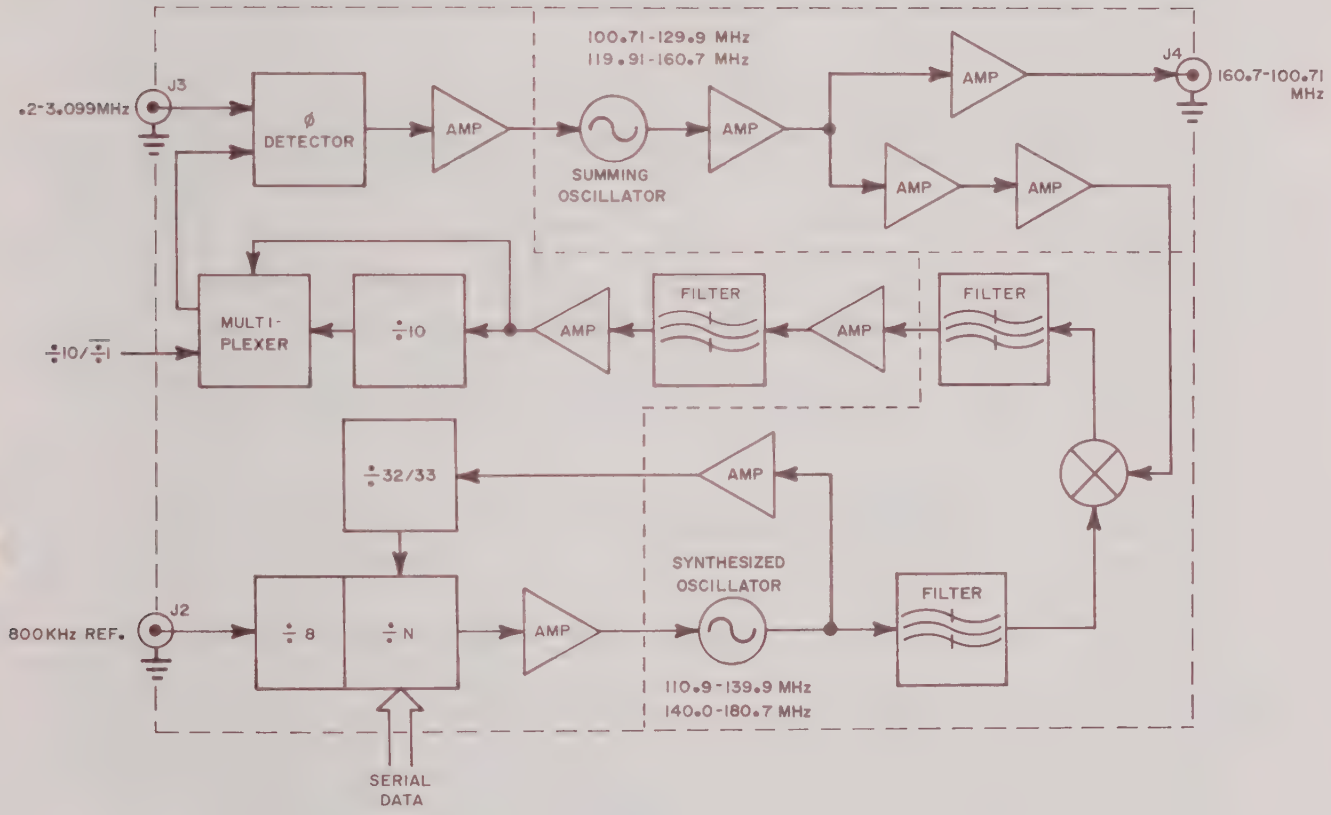


Figure 2-24 Synthesizer #2 Block Diagram

A. Synthesizer Oscillator

A phase-lock loop IC (U28007) is used to lock the synthesizer oscillator with a 100 kHz reference signal using serial data from the Control Processor. The 800 kHz reference from the Reference Oscillator is divided by eight (U28007). Phase detector output (pins 3 and 4 of U28007) charges and discharges C28064 through CR28015 and CR28016, depending on the phase difference between the divided reference and the divided VCO frequency. If the loop is unlocked, pin 9 of U28007 goes low, which activates Q28016 and causes DS28002 to illuminate. The "UNLOK" message then appears on the CRT display. The phase lock tune voltage on C28064 is integrated (U28010), which produces the control for the synthesized VCO frequency.

The synthesized VCO circuit (Q28022 and associated components) is switched between low and high ranges by data bit 19 of U28007 to control Q28017. High range results from Q28017 pulling current through CR28018 and putting L28018 and L28019 in parallel with L28012. VCO output buffer (Q28019 and Q28021) drives the mixer (MXR28001) and Q28020. Q28020 drives the dual modular prescaler (U28009), which is controlled by U28007. The prescaler divides the VCO frequency by 32 or 33, depending on its control input.

B. Summing Oscillator

The summing oscillator circuit generates the output frequency for Synthesizer #2. The difference signal from mixer 1 and input signal from Synthesizer #1 phase lock the summing oscillator frequency. The 100.71 MHz to 160.7 MHz summing VCO circuit (Q28023 and associated components) is switched between low and high ranges by data bit 18 of U28007 to control Q28006. High range occurs when Q28006 pulls current through CR28009, putting L28003 and L28020 in parallel with L28004. The VCO output is buffered (Q28008) to drive Q28009 and Q28010. The output signal produced (Q28009) is from 100.71 to 160.7 MHz to J27004. The summing VCO signal is amplified (Q28010 and Q28011) to drive the mixer (MXR28001).

The frequency difference between the summing oscillator and synthesizer oscillator (from MXR28001) is run through a series of Low-pass filters and amplifiers. The resultant phase lock error frequency for the summing VCO circuit is either a 0.2 and 3.099 MHz signal or a 20 to 30.99 MHz signal, depending on the selected scanwidth. When the scanwidth selected is from 200 kHz to 100 MHz, pin 7 of P27001 goes high. WHen P27001 goes high, U28006A selects the divide-by-ten difference signal from U28005. This causes the error frequency to be 20 to 30.99 MHz, which when divided by ten, is reduced to a signal between 2 and 3.099 MHz and compared to the Synthesizer #1 output. This effectively multiplies the Synthesizer #1 frequency by ten.

JK flip-flop (U28003) operates with U28002 as a charge pump phase comparator between the error frequency (Q28014 and Q28015) and the Synthesizer #1 input signal (J27003). If the signals are not in phase, the charge on C28011 increases or decreases accordingly, in proportion to the phase difference. C28011 voltage is integrated (U28004) to produce the control for the 100.71 to 160.7 MHz summing VCO signal. U28001A operates when phase lock is lost and the charge on C28011 is too high. The integrator direction is reversed to send the summing VCO to its lowest frequency before the VCO scans for phase lock again. Pin 6 of U28002B pulls high when an unlock condition is sensed, forcing Q28001 to conduct and illuminates DS28001.

2-4-19 2ND LO SUMMING LOOP

The 2nd LO Summing Loop uses a 100 MHz reference and the VCO input from Synthesizer #2 to phase lock an internal VCO.

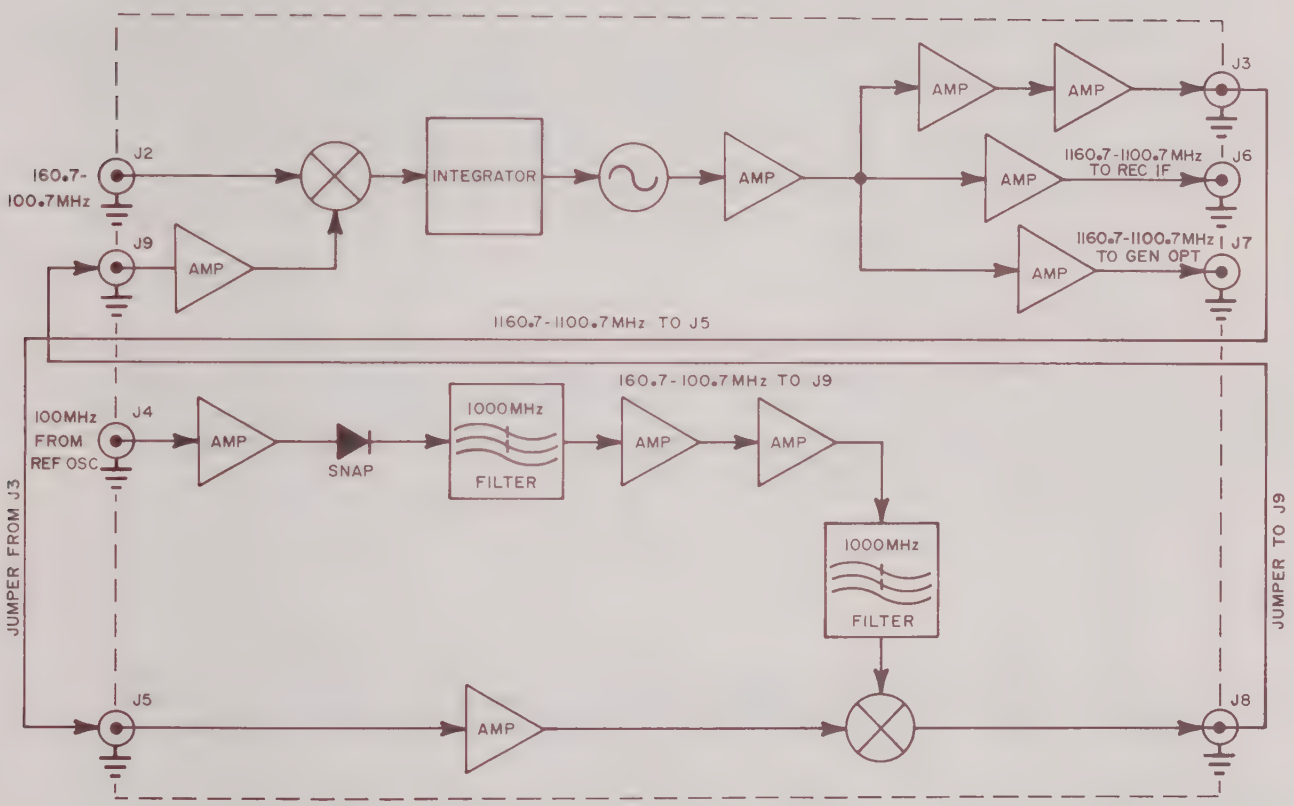


Figure 2-25 2nd LO Summing Loop Block Diagram

A. 1000 MHz Multiplier

A 100 MHz reference signal is input (J36004) and amplified (Q37002). Q37002 drives snap diode (CR37002) to produce 100 MHz harmonics. The 1000 MHz harmonic is bandpass filtered before it is amplified (Q37003 and Q37004), to drive the 2nd LO Mixer circuit.

B. 2nd LO Mixer

The 1000 MHz signal is input to MXR18001 through a 1000 MHz bandpass filter. MXR18001 mixes this signal with an 1160.7 to 1100.71 MHz VCO signal to produce 160.7 to 100.71 MHz signal for the 1160 MHz VCO board.

C. 1160 MHz VCO

160.7 to 100.71 MHz signal from the 2nd LO Mixer board is mixed with the 160.7 to 100.71 MHz signal from Synthesizer #2 at MXR38001 to obtain a desired zero pulse. If the input signals are out of phase, U38001 produces a DC output which is the tune voltage for the 1160.7 to 1100.71 MHz VCO (Q38001, CR38001, L38005, L38006 and associated components). If the CD voltage from the mixer remains out of range, the feedback network of U38001A forces the tune voltage to sweep. This drives the VCO to sweep frequency, which brings the VCO within the capture range of the phase lock loop. The output is buffered (Q38002 through Q38005) and sent to the Receive IF (J36006), the 2nd LO Mixer (J36003 and input at J36005), and to the optionally installed Generator via an output buffer (J36007).

2-4-20 TRACKING GENERATOR

The Tracking Generator option uses the 1160.7 to 1100.71 MHz output of the 2nd LO Module and the 1350 to 2350 MHz VCO Module to mix with a 189.3 MHz source and develop a tracking signal. The Tracking Generator option also includes a 0 to 75 dB Attenuator.

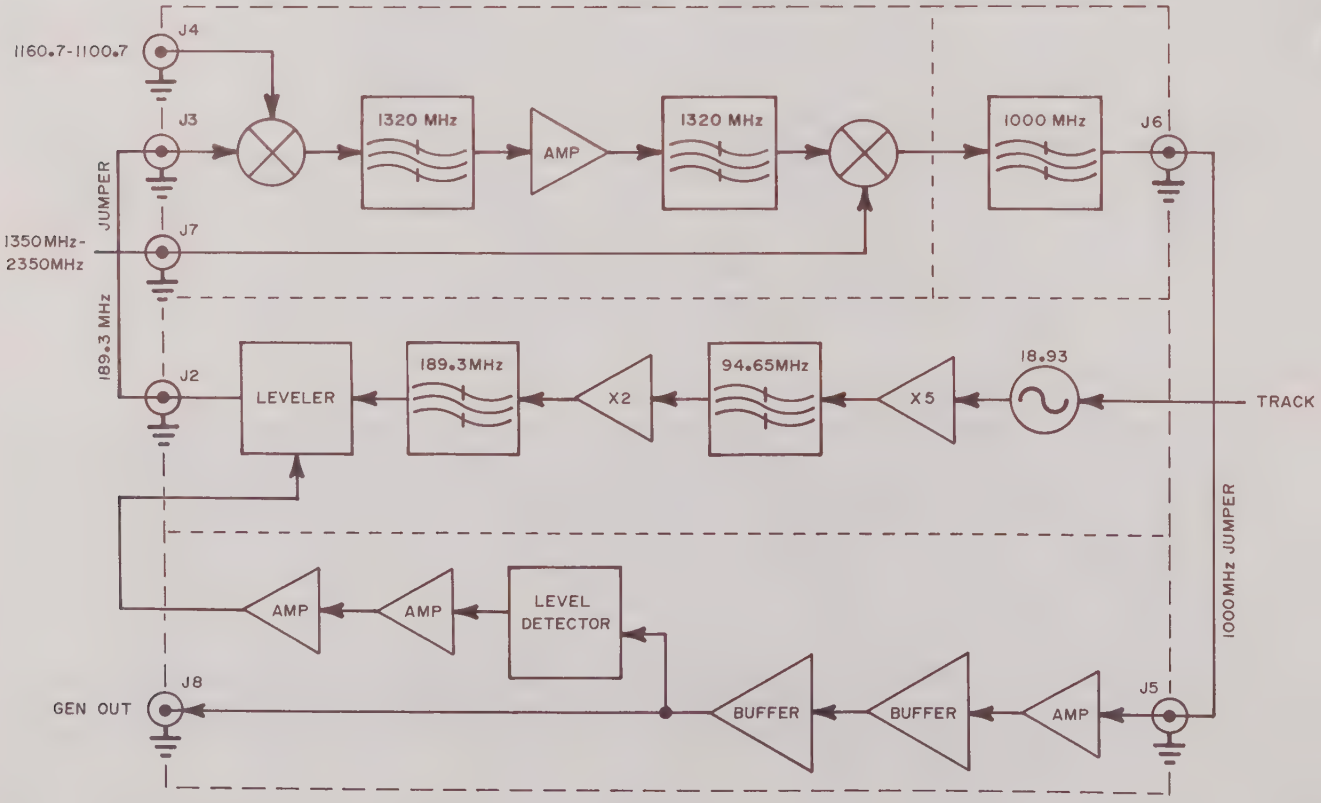


Figure 2-26 Tracking Generator Block Diagram

A. Generator Source

When the Tracking Generator is selected in the SETUP menu, pins 4 and 5 of J50001 go high to enable the module. The 18.93 MHz oscillator consists of Y51001, Q51001 and associated components. Q41002 and its filtered tank circuit is used as a multiplier (5X) which increases the frequency to 94.65 MHz. Q51003, Q51004 and the associated tank circuit (L51002 through L51004, C51018 through C51024, and related components) multiply the frequency by two to 189.3 MHz. The TRACKING ADJUST Control on the front panel is used to slew the oscillator frequency on each side of the 189.3 MHz. A positive leveler input voltage forward biases CR51002 and CR51003 to allow the 189.3 MHz source signal level to be controlled at J50002.

B. 1300 MHz Generate IF

The 189.3 MHz input at J50003 and the 2nd LO input at J50004 are mixed in MXR53001 to produce a 1290 to 1350 MHz IF which is filtered in a 1290 to 1350 MHz bandpass filter. U53001 and U53002 amplify the IF signal before it passes through another 1290 and 1350 MHz bandpass filter. MXR53002 mixes the IF signal with the 1st LO (J50007) to produce a 0 to 1000 MHz signal that is passed through a 1000 MHz Low-pass Filter and output at J50006 to the Generator Amp.

C. Generator Amp

U54001 and Q54001 amplify the 0 to 1000 MHz tracking signal input (J50005) to drive amplifier Q54002. Q54002 produces the output, a 50Ω load at J54008, and the signal to the leveler circuit. Q54003 controls the current to Q54002 for operating over a wide frequency range. The leveler circuit detector diodes (CR54002 and CR54003) detect the RF output level at J50008. The DC signal is filtered and integrated (U54002B) to control the 189.3 MHz output signal generated at J50002. The OUTPUT LEVEL ADJ trimpot (R54022) sets the generated output RF level at the GENERATE OUTPUT Connector on the front panel by adjusting the leveler circuit to the correct set point.

D. 0 to 75 dB Output Attenuator

The 0 to 75 dB output attenuator contains two interactive segments: a 0 to 60 dB attenuator, which operates in 10 dB intervals, and a 0 to 15 dB attenuator, which operates in 1 dB steps. The actual attenuation is selected from the keyboard on the Front Panel and set by the Control Processor. The Control Processor activates the control lines of the output attenuator (FL48001 through FL48007) via the Interface PC board.

1. 0 to 60 dB Output Attenuator

FL48001, FL48002 and FL48003 are the control lines that select 10 dB, 20 dB and 30 dB attenuation, respectively. This circuit is identical to the 0 to 60 dB input attenuator described in Paragraph 2-4-2.

2. 0 to 15 dB Output Attenuator

Relays K49001 through K49004 are activated by control lines FL48004 through FL48007. These operate in combination with the 0 to 60 dB Attenuator to provide the full attenuation range specified for the A-7550 Spectrum Analyzer Tracking Generator (0 to 75 dB).

When one of the control lines goes high, the corresponding relay activates a series of resistors, which increases the attenuation as selected on the front panel. For example, if 19 dB of attenuation is selected, FL48002 (10 dB), FL48004 (1 dB) and FL48007 (8 dB) all go high, which turns on relays K35002B, in the 0 to 60 dB Attenuator, and K49001 and K49004, in the 1 to 15 dB Attenuator. If 70 dB is selected, FL48001 through FL48003 go high, activating K35001B through K35003B in the 0 to 60 dB attenuator, and FL48005 and FL48007, which activates K49002 and K49004 in the 0 to 15 dB Attenuator.

SECTION 3 - PERFORMANCE EVALUATION

3-1 GENERAL

This section contains step-by-step test procedures for assessing performance of the A-7550 Spectrum Analyzer. Appendix A contains performance specifications. These procedures should be performed as the first step in the troubleshooting and maintenance process. Allow ten minutes to warm up the A-7550 to ensure its stable operation. All procedures in this section are performed using the Front and Rear Panels only. They do not require removing the case from the unit.

The Performance Evaluation tests listed below are included in this section. A performance evaluation record sheet is provided to record data from each test.

PARAGRAPH	TEST	PAGE
3-2-1	Initial Setup and Self-Test	3-7
3-2-2	Cal Out Performance Evaluation	3-8
3-2-3	Frequency Display Linearity and Readout Accuracy Performance Evaluation	3-11
3-2-4	Noise Sidebands Performance Evaluation	3-13
3-2-5	Amplitude Scale Linearity Performance Evaluation	3-15
3-2-6	Frequency Response Performance Evaluation	3-19
3-2-7	Resolution Bandwidth Accuracy Performance Evaluation	3-21
3-2-8	Variance Between Bandwidth Filters Performance Evaluation	3-23
3-2-9	IF Gain Performance Evaluation	3-25
3-2-10	RF Attenuator Performance Evaluation	3-28
3-2-11	10.7 MHz Receiver Performance Evaluation	3-31
3-2-12	Tracking Generator And Output Attenuator Performance Evaluation	3-34

NOTE: Numbers in parentheses following an A-7550 control, connector or indicator refer to item numbers shown in Figure 1-2.

3-1-1 TEST EQUIPMENT REQUIREMENTS

Appendix B contains a comprehensive list of test equipment suitable for performing the procedures in this section. Equipment not listed which meets or exceeds the stated specifications listed may be substituted for the recommended equipment.

3-1-2 CORRECTIVE MAINTENANCE PROCEDURES

The performance tests in this section are aids to operators and technicians when determining whether or not the A-7550 functions properly. A failure condition is normally reflected as either a calibration error or as a malfunction. A calibration error is defined as a measurement or reading (relating to the unit being tested) that is not within prescribed tolerances. In this condition, the set may ordinarily appear to be functioning properly. A malfunction denotes a defective condition where a signal may be totally absent, grossly out of tolerance, or that the unit, or any part thereof, is not working properly.

If a failure condition is confirmed, the technician should take appropriate corrective action to return the set to its prescribed operating condition.

Table 3-1: A-7550 PERFORMANCE EVALUATION RECORD

Technician: _____ Ser. No. _____

Date: _____

Paragraph	Test	Min Reading	Max Reading	Actual Reading
3-2-1	Self-Test	N/A	N/A	P/F
3-2-2	Cal Out			
	a. Frequency	99.9975 MHz	100.0025 MHz	_____
	b. Amplitude	-31 dBm	-29 dBm	_____
3-2-4	Noise Sidebands			
	a. Level below signal peak			_____
3-2-5	Amplitude Scale Linearity			
	a. 10 dB/Div			
	Top of Scale	N/A	N/A	_____
	-10 dB	-1.5 dB/10 dB	1.5 dB/10 dB	_____
	-20 dB	-1.5 dB/10 dB	1.5 dB/10 dB	_____
	-30 dB	-1.5 dB/10 dB	1.5 dB/10 dB	_____
	-40 dB	-1.5 dB/10 dB	1.5 dB/10 dB	_____
	-50 dB	-1.5 dB/10 dB	1.5 dB/10 dB	_____
	-60 dB	-1.5 dB/10 dB	1.5 dB/10 dB	_____
	Total (Top of Scale - 70dB):	±2.5 dB/70 dB		_____
	b. 2 dB/Div			
	Top of Scale	N/A	N/A	_____
	-2 dB	-0.4 dB/2 dB	0.4 dB/2 dB	_____
	-4 dB	-0.4 dB/2 dB	0.4 dB/2 dB	_____
	-6 dB	-0.4 dB/2 dB	0.4 dB/2 dB	_____
	-8 dB	-0.4 dB/2 dB	0.4 dB/2 dB	_____
	-10 dB	-0.4 dB/2 dB	0.4 dB/2 dB	_____
	-12 dB	-0.4 dB/2 dB	0.4 dB/2 dB	_____
	-14 dB	-0.4 dB/2 dB	0.4 dB/2 dB	_____
	Total (Top of Scale - 14dB):	±1.5 dB/14 dB		_____
	c. Linear		±2%	_____
3-2-6	Frequency Response		4 dB Variance	_____

Table 3-1 (Continued): A-7550 PERFORMANCE EVALUATION RECORD

Technician: _____ Ser. No. _____

Date: _____

Paragraph	Test	Min Reading	Max Reading	Actual Reading
3-2-7	Resolution Bandwidth Accuracy			
	a. 300 Hz	210 Hz	390 Hz	_____
	b. 3 kHz	2.1 kHz	3.9 kHz	_____
	c. 30 kHz	21.0 kHz	39.0 kHz	_____
	d. 300 kHz	210 kHz	390 kHz	_____
	e. 3 MHz	2.1 MHz	3.9 MHz	_____
3-2-8	Resolution Bandwidth Variance			
	a. 3 MHz through 3 kHz		2 dB Variance	_____
	b. 3 MHz through 300 Hz		4 dB Variance	_____
3-2-9	IF Gain (0 to 20 dB)		±2 dB	_____
3-2-10	RF Attenuator			
	a. 0 dB	Reference		_____
	b. 10 dB	-0.5 dB/10 dB	0.5 dB/10 dB	_____
	c. 30 dB	-0.5 dB/10 dB	0.5 dB/10 dB	_____
	d. 40 dB	-0.5 dB/10 dB	0.5 dB/10 dB	_____
	e. 50 dB	-0.5 dB/10 dB	0.5 dB/10 dB	_____
	f. 60 dB	-0.5 dB/10 dB	0.5 dB/10 dB	_____
3-2-11	10.7 MHz Receiver			
	a. Sensitivity (2 μV)			_____
	b. Adjacent Channel Reject			
	1. 15 kHz Filter (FM1)	<40 dB @ ±27 kHz		_____
	2. 200 kHz Filter (FM2)	<40 dB @ ±300 kHz		_____
	3. 6 kHz Filter (AM1)	<40 dB @ ±12 kHz		_____
	c. Selectivity (3 dB)			
	1. FM2		200 kHz	P/F
	2. FM1		15 kHz	P/F
	3. AM1		6 kHz	P/F

Table 3-1 (Continued): A-7550 PERFORMANCE EVALUATION RECORD

Technician: _____ Ser. No. _____

Date: _____

Paragraph	Test	Min Reading	Max Reading	Actual Reading
3-2-12	Tracking Generator (Option)			
	a. Frequency Response	100 kHz to 990 MHz (±2 dB)		_____
	b. Residual FM	100 Hz (RMS Peak)		_____
	c. Spurious			
	1. Harmonics		<20 dBc	_____
	2. Non-harmonics		<40 dBc	_____
	d. Output Attenuation		±2 dB	_____
3-2-13	Quasi-Peak (Option)			
	a. RF Level @ 4 dBm		at least 3 dBm	_____
	b. RF Level @ -17 dBm		+2 dBm @ 10.7 MHz	_____

3-2 PERFORMANCE EVALUATION PROCEDURES

NOTE: These procedures assume familiarity with A-7550 keyboard and menu operation. These are detailed in sections 3 and 4 of the A-7550 Operation Manual.

3-2-1 INITIAL SETUP AND SELF-TEST

NOTE: Values in parentheses after "MENU" and "SETTING" correspond with the key to press on the keypad when selecting the specified variable. At the end of any procedure, reset menu entries to their initial values.

STEP PROCEDURE

1. Set the following values in the menu displays:

MENU	SETTING
DISP (1)	LINE (1)
MODE (2)	LIVE (5)
RCVR (3) (if applicable)	FM1 (1)
	TSR 0 (6)
FILTERS (4)	NONE (1)
SETUP (5)	50 Ohm (1)
	dBm (2)
(if applicable)	Gen 0 (6)
SETUP (5) MANUAL (4)	Bw=A (1)
	Swp=A (2)
	Acal=1 (3)

2. Set the following A-7550 Controls:

CONTROL	SETTING
FREQUENCY (RF, ENTER)	500 MHz
SCALE (2db/LIN/10dB)	10 dB/Div

3. When all controls and menu functions are set, perform a self-test of the A-7550 Spectrum Analyzer using the "TEST" menu function (Press: MENU 5 5).

NOTE: All functions should pass the self-test. On occasion, the RAM F3 function may fail. If this occurs, retest this function (press "1" in the Test menu). The test should not fail when it is repeated.

3-2-2 CAL OUT PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF SIGNAL GENERATOR

1 MICROWATT METER

1 FREQUENCY COUNTER

PURPOSE OF TEST: Test frequency and amplitude accuracy of A-7550 Spectrum Analyzer 100 MHz calibration signal.

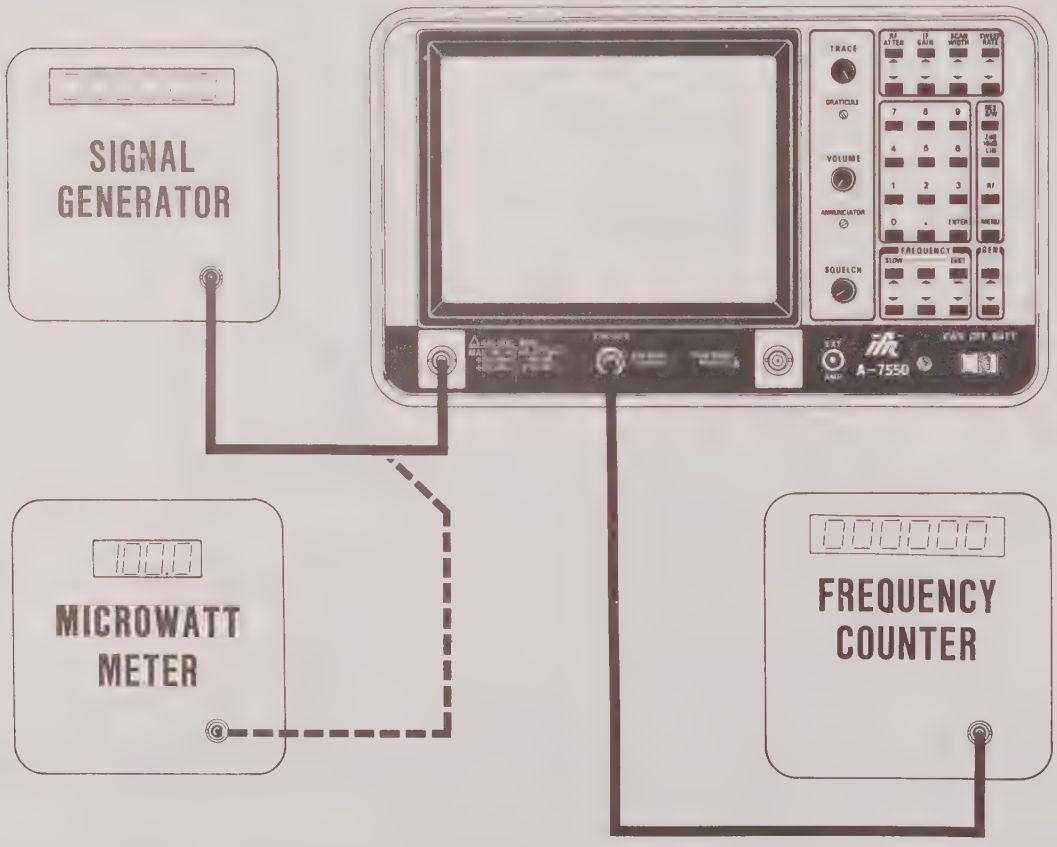


Figure 3-1 Cal Out Test Setup

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	100 MHz
RF ATTEN	10 dB
IF GAIN	0 dB
SCAN WIDTH	5 kHz/Div
RES B/W	3 kHz
SCALE (2dB/LIN/10dB)	2 dB/DIV

2. Set A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
MODE (2)	LIVE (5)
FILTERS (4)	NONE (1)
SETUP (5) MANUAL (4)	Bw=A (1)
	Acal=0 (OFF) (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	100 MHz
AMPLITUDE	-30 dBm
MODULATION	NONE (OFF)

4. Set the Frequency Counter controls to the indicated settings.

CONTROL	SETTING
MODE	CHANNEL A
FILTER	OFF
X20 ATTENUATOR	OFF
TRIGGER	MIN
REFERENCE	EXT. 10 MHz
DISPLAY DIGITS	1 Hz Resolution

Measure Frequency Accuracy

5. Connect 100 MHz CAL OUT (9) of A-7550 to Channel A input of Frequency Counter. Record the frequency error from 100 MHz in Hz on Performance Evaluation Record item 3-2-2a (Tolerance: ±2500 Hz).

6. Connect coax from CAL OUT (9) to ANALYZER INPUT (10) Connector. If signal peak is not visible, adjust RF ATTEN or IF GAIN until peak of signal is displayed at top graticule.

STEP	PROCEDURE

7. Store the signal and set the A-7550 to COMPARE Mode (Press: Menu 2 3 2).

8. Move coax from CAL OUT (9) to RF OUTPUT connector of Signal Generator. Adjust frequency and signal level to match exactly the A-7550 Spectrum Analyzer display.

9. Disconnect coax at ANALYZER INPUT (10) and measure RF output power of the Signal Generator at the open end of the coax with a power meter. Record the error in dB from -30 dBm on the Performance Evaluation Record (item 3-2-2b).

3-2-3 FREQUENCY DISPLAY LINEARITY AND READOUT ACCURACY PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 RF SIGNAL GENERATOR

PURPOSE OF TEST: Ensure display linearity within 5% of indicated frequency separation across 8 major divisions.

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	500 MHz
RF ATTEN	0 dB
IF GAIN	0 dB
SCAN WIDTH	1 kHz/Div
SCALE (2dB/LIN/10dB)	10 dB/Div

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
MODE (2)	LIVE (5)
SETUP (5) MANUAL (4)	Bw=A (1) Acal=0 (OFF) (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	500 MHz
AMPLITUDE	-40 dBm
MODULATION	NONE (OFF)

Frequency Display Linearity

4. Connect a coax from the RF Output Connector of the Signal Generator to the ANALYZER INPUT (10) Connector of the A-7550 Spectrum Analyzer.

5. Decrease the frequency of the Signal Generator to exactly four major divisions left of center frequency (i.e., CF - (4 X SCAN WIDTH). This will be the reference frequency.

STEP	PROCEDURE

6. From this reference, increase the frequency by eight times the Scan Width setting of the A-7550 Spectrum Analyzer. The signal should be shifted to within two minor divisions of the ninth major graticule (i.e., four graticules right of the center graticule, ±2 minor divisions).

7. Repeat Steps 5 and 6 for each Scan Width setting of the A-7550 Spectrum Analyzer.

Readout Accuracy

8. Disconnect the coax cable from the Signal Generator and connect it to the CAL OUT (9) Connector of the A-7550 Spectrum Analyzer.

9. Decrease the Scan Width and observe the center of the signal. It should remain centered within 1.5 minor divisions of the vertical center graticule.

10. Repeat Step 9 for all Scan Width settings to 1 kHz/Div. Harmonic response should remain within 1.5 minor divisions at each setting.

3-2-4 NOISE SIDEBANDS PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 RF SIGNAL GENERATOR

PURPOSE OF TEST: To ensure the noise floor skirt is at least -65 dBc at 5 times the Resolution Bandwidth setting.

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	225.015 MHz
RF ATTEN	30 dB
IF GAIN	0 dB
SCAN WIDTH	5 kHz/Div
RES B/W	3 kHz
SCALE (2dB/LIN/10dB)	10 dB/Div

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
MODE (2)	AVERAGE (1)
FILTERS (4)	300 Hz (3)
SETUP (5) MANUAL (4)	Bw=A (1)
	Acal=0 [OFF] (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	225.0 MHz
AMPLITUDE	0 dBm
MODULATION	NONE (OFF)
REFERENCE	INTERNAL

Measure Noise Floor Skirt

4. Connect coax cable from RF Connector of Signal Generator to ANALYZER INPUT (10) Connector of A-7550 Spectrum Analyzer.

5. Adjust the frequency from the Signal Generator to offset it 15 kHz from the Center Frequency of the A-7550 Spectrum Analyzer.

STEP	PROCEDURE
6.	Adjust the signal level from the Signal Generator until it just touches the top graticule of the A-7550 Spectrum Analyzer.
7.	Record the noise level at the vertical center graticule (in dBc) on the Performance Evaluation Record (item 3-2-4).

3-2-5 AMPLITUDE SCALE LINEARITY PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF SIGNAL GENERATOR

1 PRECISION 1 dB STEP ATTENUATOR

1 PRECISION 10 dB STEP ATTENUATOR

PURPOSE OF TEST: To measure the linearity of the amplitude scales. The 10 dB amplitude scale should be accurate within 2.5 dB across a range of 70 dB and within 1.5 dB at each 10 dB step. The 2 dB amplitude scale should be accurate within 1.5 dB across a range of 14 dB and within 0.4 dB at each 2 dB step.

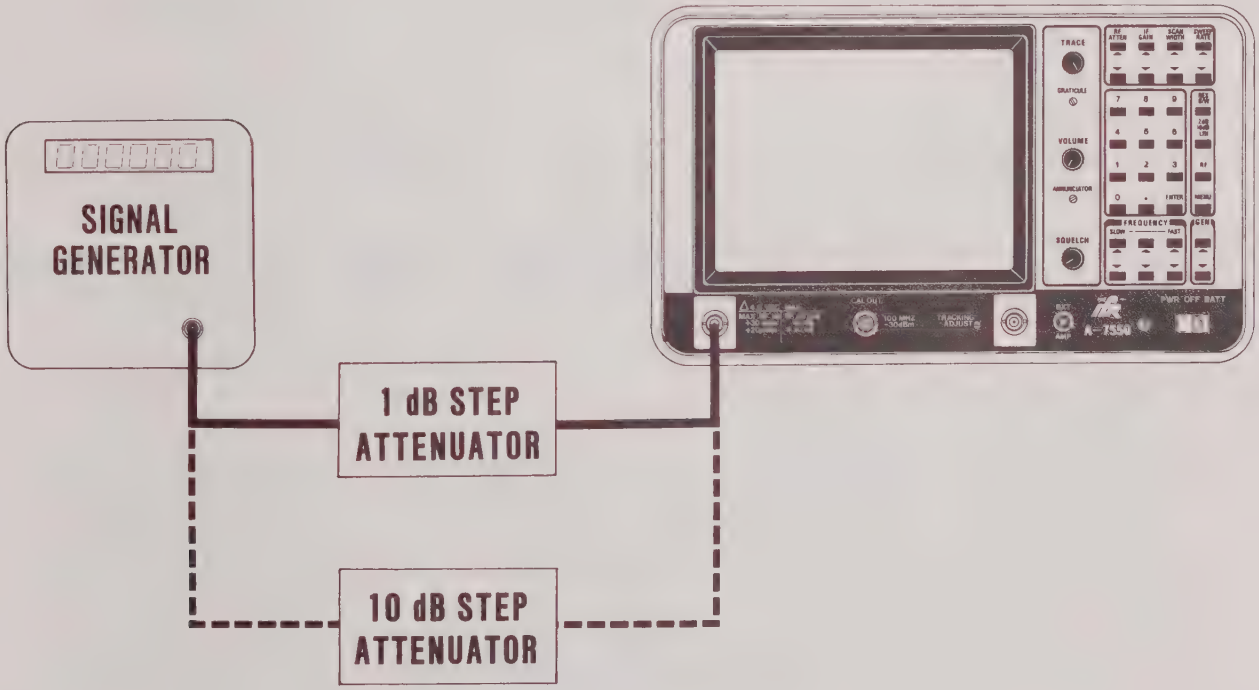


Figure 3-2 Amplitude Scale Linearity Test Setup

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	10 MHz
SCAN WIDTH	5 kHz/Div
RES B/W	3 kHz
RF ATTEN	0 db
SCALE (2dB/LIN/10dB)	10 dB

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
MODE (2)	AVERAGE (1)
FILTERS (4)	300 Hz (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	10.0 MHz
AMPLITUDE	-30 dBm
MODULATION	NONE (OFF)

4. Connect a coax from the Signal Generator Output Connector through the 10 dB Step Attenuator to the ANALYZER INPUT Connector (10) on the A-7550 Spectrum Analyzer.

10 dB Amplitude Scale Linearity

5. Use the Step Attenuator to step down signal in 10 dB steps from Top of Scale. At each 10 dB step, the deviation from the previous reference should not be greater than 1.5 dB. Total deviation, when the signal is stepped down 70 dB, should not exceed 2.5 dB across the full range.

   NOTE: Record actual levels (marked with *) in Steps 5 and 7 on Performance Evaluation Record (items 3-2-5a and 3-2-5b).

REFERENCE	LEVEL (ACTUAL)*		STEP DEVIATION	TOTAL DEVIATION*
Top of Scale	_____			_____
		--	_____	
-10 dB	_____			
		--	_____	
-20 dB	_____			
		--	_____	
-30 dB	_____			
		--	_____	
-40 dB	_____			
		--	_____	
-50 dB	_____			
		--	_____	
-60 dB	_____			
		--	_____	
-70 dB	_____			_____

2 dB Amplitude Scale Linearity

6. Disconnect the 10 dB Step Attenuator and connect the 1 dB Step Attenuator.

7. Set the Scale on the A-7550 Spectrum Analyzer to 2 dB/Div. Use the Step Attenuator to step down the signal in 2 dB steps from Top of Scale. At each 2 dB step, the deviation should not be greater than .4 dB from the previous step. Total deviation, when the signal is stepped down 14 dB, should not exceed 1.5 dB across the full range.

REFERENCE	LEVEL (ACTUAL)*		STEP DEVIATION	TOTAL DEVIATION*
Top of Scale	_____			_____
		--	_____	
-2 dB	_____			
		--	_____	
-4 dB	_____			
		--	_____	
-6 dB	_____			
		--	_____	
-8 dB	_____			
		--	_____	
-10 dB	_____			
		--	_____	
-12 dB	_____			
		--	_____	
-14 dB	_____			_____

STEP	PROCEDURE

LINEAR Scale Linearity

8. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
SCALE (2dB/LIN/10dB)	LINEAR
IF GAIN	0 dB
RF ATTEN	0 dB

9. Adjust signal to top display graticule, if needed.

10. Use the 1 dB Step Attenuator to decrease Signal Generator output 6 dBm. Verify signal is at horizontal center graticule within 0.4 major divisions (±2 minor divisions). Record on Performance Evaluation Record item 3-2-5c.

3-2-6 FREQUENCY RESPONSE PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF SIGNAL GENERATOR (may be STEP PROGRAMMABLE)

1 POWER METER w/THERMISTOR MOUNT

PURPOSE OF TEST: To measure overall flatness of signal across full frequency range of A-7550 Spectrum Analyzer within 4 dB.

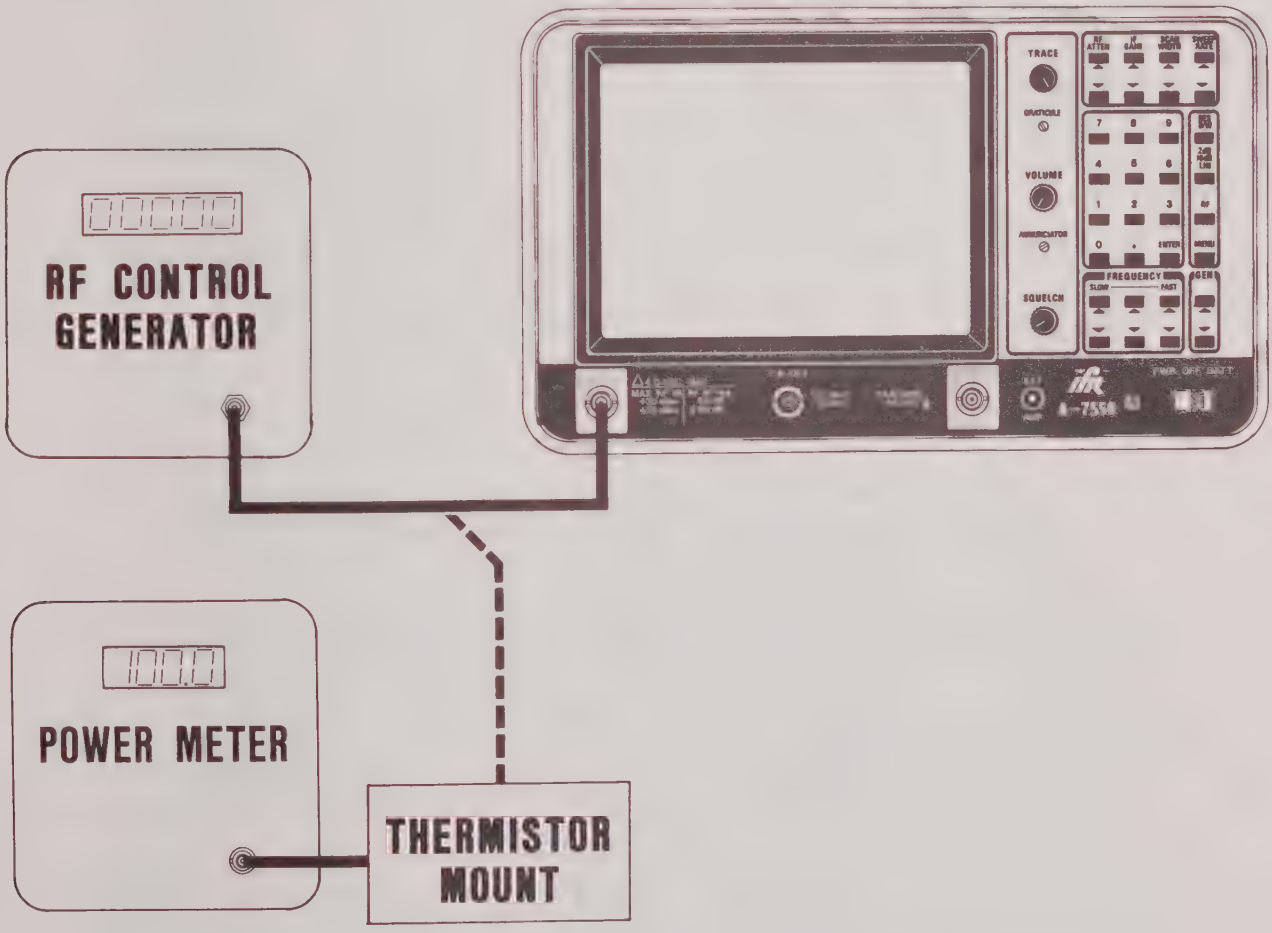


Figure 3-3 Frequency Response Test Setup

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	500 MHz
SCAN WIDTH	100 MHz/Div
RF ATTEN	0 dB
IF GAIN	0 dB
SCALE (2dB/LIN/10dB)	2 dB

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated value.

MENU	SETTING
MODE (2)	PkHold (6)
FILTERS (4)	NONE (1)
SETUP (5) MANUAL (4)	Bw=M (1)
	Acal=0 (OFF) (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	10.0 MHz
AMPLITUDE	-34 dBm
MODULATION	NONE (OFF)

NOTE: Measure amplitude with Power Meter at end of coax before proceeding. Adjust signal amplitude to -34 dBm indication, as required.

4. Connect coax cable from RF Signal Generator Output Connector to ANALYZER INPUT (10) Connector of A-7550 Spectrum Analyzer.

5. Disconnect coax cable from ANALYZER INPUT (10) Connector and connect it to the Power Meter.

6. Increase Signal Generator frequency 10 MHz and adjust signal level at signal source for -34 dBm, as needed.

7. Repeat Steps 4 through 6 to 1000 MHz.

8. Verify the excursions on the A-7550 Spectrum Analyzer display do not exceed 4 dB between maximum and minimum amplitude levels of the display.

3-2-7 RESOLUTION BANDWIDTH ACCURACY PERFORMANCE EVALUATION

SPECIAL ACCESSORY
EQUIPMENT REQ'D: 1 RF SIGNAL GENERATOR

PURPOSE OF TEST: To ensure 3 dB Bandwidth Filter shape within 30% of selected settings.

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	225.0 MHz
SCAN WIDTH	1 kHz/Div
RF ATTEN	10 dB
IF GAIN	0 dB
SCALE (2dB/LIN/10dB)	2 dB
RES B/W	300 Hz

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
MODE (2)	LIVE (5)
FILTERS (4)	NONE (1)
SETUP (5) MANUAL (4)	Bw=M (1)
	Acal=0 [OFF] (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	225.0 MHz
AMPLITUDE	-28.0 dBm
MODULATION	NONE (OFF)

Measure Bandwidths

4. Connect coax cable from RF output connector of the Signal Generator to ANALYZER INPUT (10) Connector of A-7550 Spectrum Analyzer.

5. Adjust signal from Signal Generator so top of signal is on the center graticule (horizontal) of the A-7550 Spectrum Analyzer display.

6. Increase the signal from the Signal Generator 3 dB.

7. Measure the bandwidth at the center graticule to be between 210 Hz and 390 Hz (at 300 Hz Resolution). Record the bandwidth in the Performance Evaluation Record on the appropriate line of item 3-2-6.

8. Repeat Steps 5 through 7 for each bandwidth using the constraints of Table 3-2. Record each step on the appropriate line of item 3-2-6 of the Performance Evaluation Record.

BANDWIDTH SELECTION	SCAN WIDTH SELECTION	MINIMUM BANDWIDTH	MAXIMUM BANDWIDTH
3 kHz	1 kHz/Div	2.1 kHz	3.9 kHz
30 kHz	10 kHz/Div	21.0 kHz	39.0 kHz
300 kHz	100 kHz/Div	210 kHz	390 kHz
3 MHz	1 MHz/Div	2.1 MHz	3.9 MHz

Table 3-2 Parameters for Resolution Bandwidth Performance Evaluation

3-2-8 VARIANCE BETWEEN BANDWIDTH FILTERS PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 RF SIGNAL GENERATOR

PURPOSE OF TEST: To measure the difference between Resolution Bandwidth filters of the A-7550 Spectrum Analyzer.

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	225.0 MHz
SCAN WIDTH	1 kHz/Div
RF ATTEN	10 dB
IF GAIN	0 dB
SCALE (2dB/LIN/10dB)	2 dB
RES B/W	300 Hz

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
MODE (2)	LIVE (5)
FILTERS (4)	NONE (1)
SETUP (5) MANUAL (4)	Bw=M (1)
	Acal=0 (OFF) (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	225.0 MHz
AMPLITUDE	-28.0 dBm
MODULATION	NONE (OFF)

Measure Variance

4. Connect a coax from RF Output Connector of Signal Generator to ANALYZER INPUT (10) Connector of A-7550 Spectrum Analyzer.

5. Adjust Signal Generator output level to display exactly -28 dBm on A-7550 Spectrum Analyzer. Measure for -28 dBm output of Signal Generator at the end of the coax with a microwatt meter. Record the output level of the Signal Generator in Table 3-3.

6. Repeat Step 5 for each Resolution Bandwidth setting of the A-7550 Spectrum Analyzer. Use the Scan Width settings as shown in Table 3-3.

BANDWIDTH SETTING	SCAN WIDTH SETTING	LEVEL
300 Hz	1 kHz/Div	_____
3 kHz	1 kHz/Div	_____
30 kHz	10 kHz/Div	_____
300 kHz	100 kHz/Div	_____
3 MHz	1 MHz/Div	_____

Table 3-3 Scan Width Settings for Bandwidth Selections

7. Calculate bandwidth switching error of 3 MHz, 300 kHz, 30 kHz and 3 kHz bandwidths by subtracting the smallest signal amplitude reading from the largest reading. The variance should not be greater than 2 dB. Record difference on item 3-2-8a of Performance Evaluation Record.

8. Repeat Step 7 for 300 Hz bandwidth. The variance should not be greater than 4 dB. Record difference on item 3-2-8b of Performance Evaluation Record.

3-2-9 IF GAIN PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
1 RF SIGNAL GENERATOR
1 10 dB STEP ATTENUATOR

PURPOSE OF TEST: Ensure each IF GAIN step is operable.

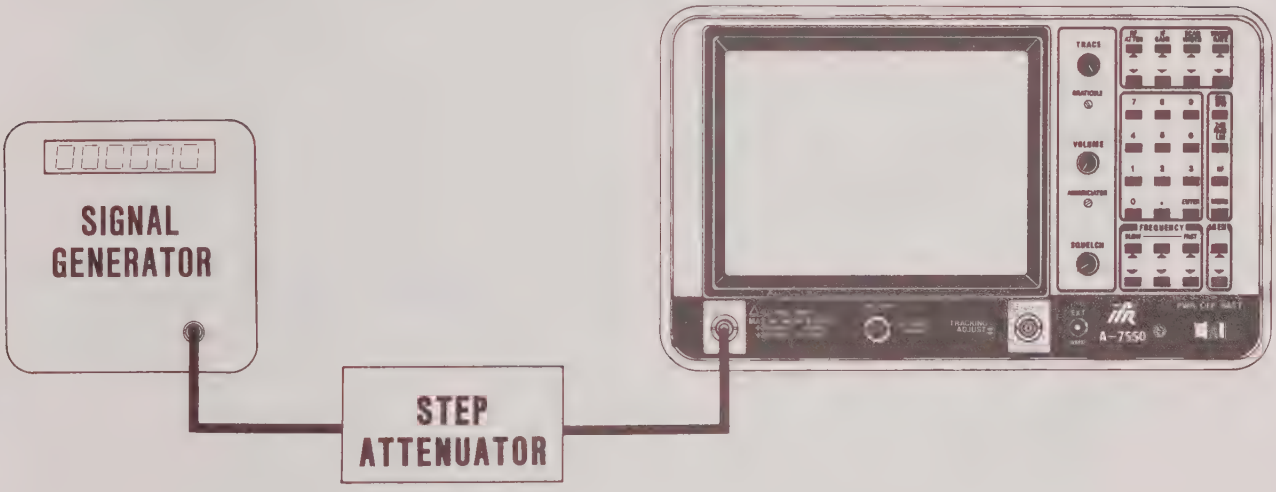


Figure 3-4 IF Gain Test Setup

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	225.0 MHz
RF ATTEN	30 dB
IF GAIN	0 dB
SCAN WIDTH	5 kHz/Div
SCALE (2dB/LIN/10dB)	2 dB/Div

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
MODE (2)	LIVE (5)
FILTERS (4)	300 Hz
SETUP (5) MANUAL (4)	Bw=A (1) Acal=0 (OFF) (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	225.0 MHz
AMPLITUDE	-8 dBm
MODULATION	NONE (OFF)

4. Connect a coax cable from the RF Output of the Signal Generator to the Step Attenuator. Connect the Step Attenuator to to the ANALYZER INPUT (10) Connector of the A-7550 Spectrum Analyzer.

Measure 20 dB of IF GAIN

5. Adjust output level of the Signal Generator to indicate -8 dBm on A-7550 Spectrum Analyzer display.

6. Enter the MODE Menu and store the signal. When the signal is stored, select COMPARE Mode (Press: MENU 2 3 2).

7. Use the 10 dB Step Attenuator to decrease the input level from the Signal Generator exactly 20 dB. Increase IF GAIN on the A-7550 Spectrum Analyzer 20 dB (i.e., Top of Scale = -20 dBm).

8. Record the algebraic difference between the stored signal level and the signal level after 20 dB of IF GAIN is applied on the Performance Evaluation Record (item 3-2-9a).

STEP PROCEDURE

9. Disconnect the Step Attenuator and connect the Signal Generator to the Analyzer Input (10) Connector of the A-7550 Spectrum Analyzer.

Check Functional Operation

10. Reset the A-7550 Controls to the following settings.

CONTROL	SETTING
RF ATTEN	60 dB
IF GAIN	65 dB
SCALE	10 dB/Div

11. Reset the A-7550 MODE Menu to LIVE (Press: MENU 2 5).

12. Set the Amplitude readout of the Signal Generator to -40 dBm.

13. Decrease the IF GAIN to 0 dB, observing the display at each 1 dB step. The level should drop approximately 1 dB per step.

3-2-10 RF ATTENUATOR PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:
- 1 RF SIGNAL GENERATOR
- 1 10 dB STEP ATTENUATOR

PURPOSE OF TEST: Ensure all steps of the input attenuator are operational within 0.5 dB at each step.

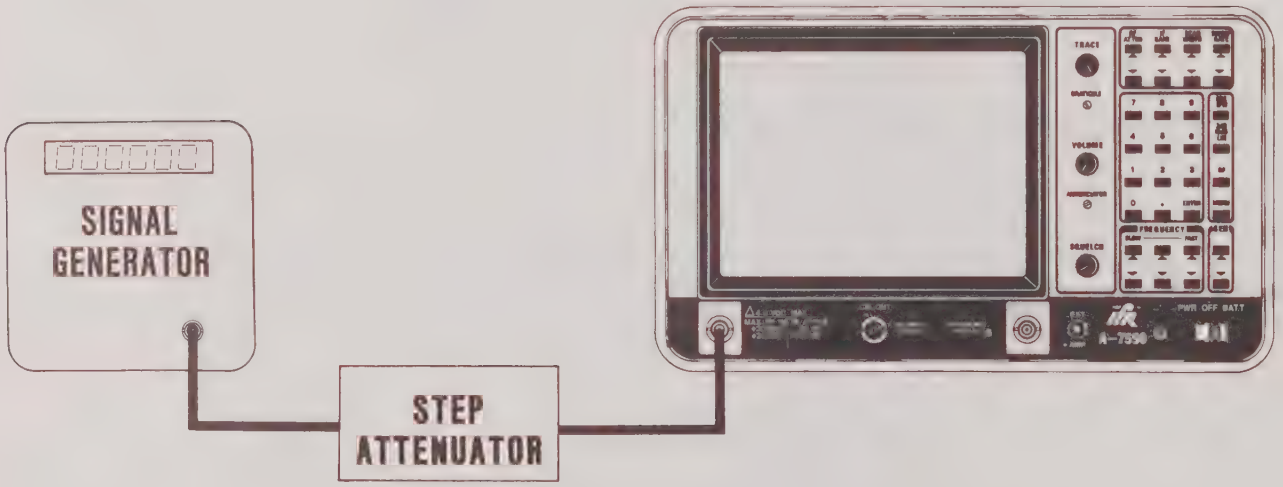


Figure 3-5 RF Attenuator Test Setup

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	225.0 MHz
RF ATTEN	0 dB
IF GAIN	30 dB
SCAN WIDTH	5 kHz
SCALE (2dB/LIN/10dB)	2 dB/Div

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
MODE (2)	LIVE (5)
FILTERS (4)	NONE (1)
SETUP (5) MANUAL (4)	Bw=A (1) Acal=0 (OFF) (3)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	225.0 MHz
AMPLITUDE	-8 dBm
MODULATION	NONE (OFF)

4. Set Precision Step Attenuator for 60 dB Attenuation.

5. Connect coax cable from RF Output of Signal Generator to 10 dB Step Attenuator. Connect 10 dB Step Attenuator to ANALYZER INPUT (10) Connector of the A-7550 Spectrum Analyzer.

Test 10 dB Step Accuracy

6. Adjust output level from the Signal Generator to indicate exactly -68 dBm on the A-7550 Spectrum Analyzer display.

7. Select the MODE Menu and store the signal. When the signal is stored, select COMPARE Mode of operation (Press: MENU 2 3 2).

8. Increase RF ATTEN 10 dB on A-7550 Spectrum Analyzer.

9. Use the Step Attenuator to increase the output level by exactly 10 dB.

STEP	PROCEDURE
10.	Record the algebraic difference between the stored signal level and the signal level from the Signal Generator on the Performance Evaluation Record (item 3-2-10a).
11.	Return to LIVE Mode. Repeat Steps 6 through 8 for RF ATTEN settings of 20 dB through 60 dB. Record the error at each step in the Performance Evaluation Record (items 3-2-10b through 3-2-10f).

3-2-11 10.7 MHZ RECEIVER PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 RF SIGNAL GENERATOR

PURPOSE OF TEST: To measure the channel rejection and selectivity performance of the 10.7 MHz Receiver.

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	225.0 MHz
RF ATTEN	0 dB
IF GAIN	0 dB
SCAN WIDTH	0 kHz/Div
SCALE (2dB/LIN/10dB)	10 dB/Div

2. Set the A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
RCVR (3)	FM1 (1) TSR 0 (OFF) (6)
SETUP (5)	dBm (1) 50Ω (2)

3. Set the Signal Generator controls to the indicated settings.

CONTROL	SETTING
FREQUENCY	225.0 MHz
AMPLITUDE	-101 dBm
MODULATION	5 kHz deviation @ 1 kHz rate

4. Adjust SQUELCH Control (5) to full counter-clockwise (ccw) position.

5. Connect RF Signal Generator output to ANALYZER INPUT (10) Connector of A-7550 Spectrum Analyzer.

Sensitivity

6. Adjust Volume Control (12), as necessary, to verify demodulated tone is distinguishable.

STEP	PROCEDURE

Adjacent Channel Rejection

7. Adjust RF Signal Generator to 225 MHz at -85 dBm with Modulation OFF.

8. Adjust Squelch Control (5) to threshold where receiver noise is squelched. Adjust RF Signal Generator level to -45 dBm.

9. Increase the frequency of the RF Signal Generator above 225 MHz. Record the frequency where the unit is squelched on the Performance Evaluation Record (item 3-2-11b).

10. Decrease the frequency of the RF Signal Generator below 225 MHz. Record the frequency where the unit is squelched on the Performance Evaluation Record (item 3-2-11b).

11. Subtract the lower frequency (Step 10) from the higher frequency (Step 9). Verify the difference is less than or equal to 54 kHz.

12. Change the A-7550 Receiver bandwidth setting to FM2 (Press: MENU 3 2 MENU).

13. Repeat Steps 7 through 10, above. Subtract the lower frequency (Step 10) from the higher frequency (Step 9). Verify the difference is less than or equal to 600 kHz.

14. Change the A-7550 Receiver bandwidth setting to AM1 (Press: MENU 3 4 MENU).

15. Repeat Steps 7 through 10, above. Subtract the lower frequency (Step 10) from the higher frequency (Step 9). Verify the difference is less than or equal to 24 kHz.

Selectivity

16. Set RF Signal Generator Amplitude to -80 dBm at 225 MHz.

17. Connect RF input of Signal Generator to ANALYZER INPUT (10) Connector of A-7550 Spectrum Analyzer.

18. Set RCVR Menu to FM2 (Press: MENU 3 2 MENU).

19. Quiet A-7550 Receiver with Squelch Control (5).

20. Using Table 3-4, increase RF Signal Generator frequency to correspond with the FM2 frequency that is greater than 225 MHz.

21. Verify level of RF Generator can be increased $\geq$3 dB before squelch is broken.

STEP PROCEDURE

22. Reset RF Signal Generator Amplitude to -80 dBm and refer again to Table 3-4. Decrease RF Signal Generator frequency to correspond with the FM2 frequency that is less than 225 MHz on this table. Verify level of RF Generator can be increased $\geq$3 dB before squelch is broken. Note results in Performance Evaluation Record (item 3-2-11c).

23. Set RCVR Menu to FM1 (Press: MENU 3 1 MENU). Reset RF Signal Generator Amplitude to -80 dBm and refer again to Table 3-4. Repeat Steps 19 through 22 for AM1.

24. Set RCVR Menu to AM1 (Press: MENU 3 4 MENU). Reset RF Signal Generator Amplitude to -80 dBm and refer again to Table 3-4. Repeat Steps 19 through 22 for AM1.

RF SIGNAL GENERATOR (MHz)	A-7550 FREQUENCY (MHz)	RCVR MENU
225.1000	225.0000	FM2
224.9000	225.0000	FM2
225.0075	225.0000	FM1
224.9925	225.0000	FM1
225.0030	225.0000	AM1
224.9970	225.0000	AM1

Table 3-4 Selectivity Settings

3-2-12 TRACKING GENERATOR AND OUTPUT ATTENUATOR PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF SIGNAL GENERATOR

1 SPECTRUM ANALYZER

1 MODULATION METER

1 POWER METER

1 FREQUENCY COUNTER

PURPOSE OF TEST: Measure Flatness, Tracking Adjustment, Residual FM, Spurious signal and Output Attenuation of Tracking Generator Option.

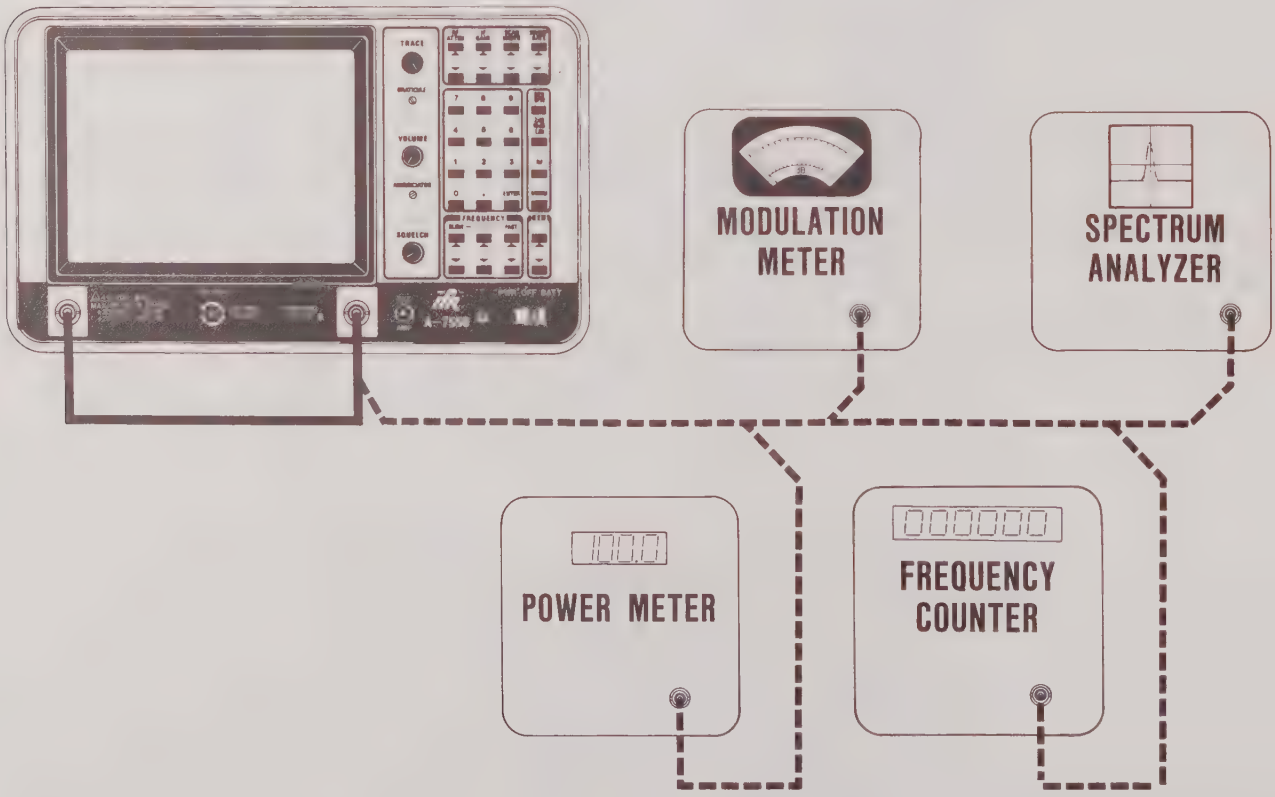


Figure 3-6 Tracking Generator/Output Attenuator Test Setup

STEP PROCEDURE

1. Set A-7550 Spectrum Analyzer Menu functions to the indicated values.

MENU	SETTING
SETUP (5)	dBm (1) 50Ω (2) GEN 1 (6)

2. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	10.0 MHz
GEN ATTEN	0 dB
SCAN WIDTH	0 kHz/Div
SCALE (2dB/LIN/10dB)	10 dB/Div

3. Connect a short 50Ω Coax Cable from the GENERATE OUTPUT (7) Connector of the A-7550 Spectrum Analyzer to the RF input of the external Spectrum Analyzer.

4. Set the external Spectrum Analyzer controls to easily view the amplitude of the Generator Output.

Flatness

5. Note the amplitude of the displayed signal on the external Spectrum Analyzer.

6. Move the coax cable from the GENERATE OUTPUT (7) Connector of the A-7550 Spectrum Analyzer to the RF output of the external signal generator.

7. Adjust the frequency and output level of the external Signal Generator for an exact match on the external Spectrum Analyzer as noted in Step 5.

8. Disconnect the coax cable at the external Spectrum Analyzer and measure the output power to the end of the coax cable with a Power Meter.

9. Note the Power Meter indication or plot on graph paper.

10. Increment the frequency of the A-7550 Spectrum Analyzer by 10 MHz.

11. Repeat Steps 3 through 10 to 990 MHz.

12. Calculate the difference between the minimum and maximum amplitude readings. Record these as item 3-2-12a on the Performance Evaluation Record.

STEP	PROCEDURE

Tracking Adjust

13. Set the A-7550 Spectrum Analyzer Center Frequency to 10 MHz.

14. Connect Coax Cable from GENERATE OUTPUT (7) Connector of the A-7550 Spectrum Analyzer to the Frequency Counter.

15. Use the TRACKING ADJUST (8) to verify Generator frequency varies from ≥3 kHz below 10 MHz to ≥6 kHz above 10 MHz (i.e., Generator frequency is ≤9.997 MHz to ≤10.006 MHz).

16. Set the TRACKING ADJUST (8) to 10 MHz before disconnecting Frequency Counter.

Residual FM

17. Set the A-7550 Spectrum Analyzer Center Frequency to 100 MHz.

18. Connect Modulation Meter to the GENERATE OUTPUT (7) Connector of the A-7550 Spectrum Analyzer.

19. Verify Residual FM is <100 Hz (RMS Peak).

20. Disconnect Coax Cable from the Modulation Meter.

Spurious

21. Set A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	500.0 MHz (RF, ENTER)
SWEEP RATE	2 Sec/Div

22. Connect an external Spectrum Analyzer to the GENERATE OUTPUT (7) Connector of the A-7550 Spectrum Analyzer.

23. Set the controls of the external Spectrum Analyzer to view 0 Hz to 1 GHz spectrum.

24. Verify the following:

    a. Harmonics are ≤20 dBc.
    b. Non-harmonics are ≤40 dBc.

STEP PROCEDURE

Output Attenuator

25. Set the A-7550 Spectrum Analyzer controls to the indicated settings.

CONTROL	SETTING
CENTER FREQUENCY	500 MHz (RF, ENTER)
RF ATTENUATION	40 dB
SCALE (2dB/LIN/10dB)	2dB/Div
GEN Output (GEN)	0 dBm

26. Connect coax cable from GENERATE OUTPUT (7) Connector to ANALYZER INPUT (10) Connector of the A-7550 Spectrum Analyzer.

27. Store the displayed signal and select the COMPARE Mode and REFERENCE Display (Press: MENU 2 3 0 1 3).

28. Decrease the Tracking Generator output level 1 dB.

29. Increase the IF GAIN 1 dB.

30. The displayed signal should match the horizontal center graticule ±2 dB (1 major division).

31. Repeat Steps 27 through 30 until Tracking Generator output level reaches -30 dBm.

SECTION 4 - CALIBRATION

4-1 GENERAL

This section contains the following calibration procedures:

Calibration Procedure	Title	Page
4-2	Power Supply Calibration	4-11
4-3	Display Calibration	4-15
4-4	CRT Calibration	4-17
4-5	Reference Oscillator Calibration	4-23
4-6	RF Control Calibration	4-25
4-7	Amplitude Calibration	4-29
4-8	10.7 MHz Receiver Calibration ..	4-38
4-9	Tracking Generator Calibration .	4-41
4-10	Quasi-Peak Filter Calibration ..	4-44

Paragraphs 4-2 through 4-7 comprise the normal calibration procedure. A calibration record sheet is provided for recording data from these procedures. Paragraphs 4-8 and on are performed only if the particular option is installed, as necessary. The normal calibration procedures should be performed when one or more of the following conditions are met:

A. If, during the course of normal operation, the A-7550 or any major function thereof fails to meet the performance specifications as provided in "SECTION 3 - PERFORMANCE EVALUATION".

B. If a module is found to be defective and requires replacement (see Table 4-1, Module Replacement & Calibration Requirements).

C. If the recommended 12-month calibration interval is due.

The A-7550 Calibration Record on pages 4-5 through 4-10 can be used to keep track of calibration procedures performed and measurements obtained. You may want to duplicate these pages for future use. Reference numbers (callouts) in parentheses refer to Front/Rear Panel designators. These correspond to the designators used in Figure 1-2.

4-1-1 SAFETY PRECAUTIONS

As with any piece of electronic equipment, extreme caution should be taken when working on "live" circuits. Certain circuits and/or components within the A-7550 contain extremely high voltage potentials, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. When performing the calibration procedures, be sure to observe the following WARNINGS:

WARNING! WHEN WORKING WITH "LIVE" CIRCUITS OF HIGH POTENTIAL:

KEEP ONE HAND IN POCKET OR BEHIND BACK, TO AVOID SERIOUS SHOCK HAZARD.

REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL.

USE ONLY INSULATED TROUBLESHOOTING TOOLS.

FOR ADDED INSULATION, PLACE RUBBER BENCH MAT UNDERNEATH ALL POWERED BENCH EQUIPMENT AND A RUBBER FLOOR MAT UNDERNEATH TECHNICIAN'S CHAIR.

HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.

4-1-2 CALIBRATION EQUIPMENT REQUIREMENTS

Appendix B contains a list of test equipment suitable for performing any of the procedures listed in this manual. Any other equipment meeting the specifications listed in Appendix B may be substituted for the recommended models. Allow A-7550 Spectrum Analyzer at least 10 minutes to warm-up to insure electrical stability.

NOTE: For certain procedures in this section, the equipment listed in Appendix B may exceed the minimum required specifications; for this reason, minimum use specifications appear with all calibration procedures where accessory test equipment is required.

4-1-3 DISASSEMBLY REQUIREMENTS

To perform any calibration procedure in this section, the case must be removed from the A-7550.

MODULES BEING REPLACED OR REPAIRED / CALIBRATION PROCEDURE(S) PERFORMED	POWER SUPPLY (4-2)	DISPLAY (4-3)	CRT (4-4)	REFERENCE OSCILLATOR (4-5)	RF CONTROL (4-6)	AMPLITUDE (4-7)	(4
POWER SUPPLY	●				●		●
REFERENCE OSCILLATOR				●			
I/P ATTENUATOR						●	
RECIEVE IF					●	●	
10.7 MHz RECIEVER							
ANALYZER IF						●	
QUASI PEAK						●	
LOG AMP						●	
SWEEP DIGITIZER BOARD		●			●		
VIDEO PROCESSOR BOARD		●					
CRT		●	●			●	
1st L.O. SAMPLING LOOP					●		
2nd L.O. SAMPLING LOOP					●		
SYNTHESIZER # 1					●		
SYNTHESIZER #2					●		
INTERFACE BOARD					●	●	
TRACKING GENERATOR							●
[1] O/P ATTENUATOR							●
[1] EXTERNAL AMPLIFIER							●
1350-2350 MHz VCO					●		
[2] RF MOTHERBOARD	[2]						
[2] CONTROL PROCESSOR BOARD	[2]						

TRACKING GENERATOR (4-8)	10.7 MHz RECEIVER (4-9)	QUASI PEAK FILTER (4-10)
●		
	●	
		●
●		
●		
●		

1 Perform only if Tracking Generator is installed
2 Check operation only: Select different frequencies and amplitude

Table 4-1 Module Replacement and Calibration Requirements

TABLE 4-2: A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

Date: _____

	Para (Step)	Value/Checked
1. Power Supply:	4-2	
Power Supply Lines:		
+16V, ±0.5V	(1,2,3)	_____
+5.2V, ±0.05V	(1,2,3)	_____
+12V, ±0.2V	(1,2,3)	_____
-12V, ±0.5V	(1,2,3)	_____
+40V, +32V to +45V	(1,2,3)	_____
Batt Charge: +14.5V at 0.3A	(4-6)	_____
Current Limit: 1.1A to 1.7A	(7)	_____
Batt Monitor:		
Low: 5.0V, ±0.1V	(8)	_____
High: 7.5V, ±0.1V	(9)	_____
Low Voltage Cutoff: 11.0V to 11.8V	(12)	_____
Batt Timer: 10 min ± 2 min	(13)	_____
Line Interrupt: 2 sec. minimum	(14,15)	_____
External DC: +12V to 30 VDC (operates)	(16)	Yes/No
2. Display:	4-3	
Reset to LOGO on Power-up	(2)	_____
Grid Display Alignment	(3)	_____
Alpha Display	(4)	_____
Keyboard Operation	(5)	_____
Keyboard Annunciator Adj.	(6)	_____
Graticule Intensity	(7)	_____
Trace Intensity Adj.	(8)	_____
Yoke		
3. CRT:	4-4	
Preset Pots (check only):	(5a-h)	_____
Reset Power	(6)	_____
Master Brightness (R71012)	(7)	_____
Vertical	(8)	_____
Width	(9)	_____
Interlace	(10)	_____
Focus	(11)	_____
Trace	(12)	_____
Graticule	(13)	_____
Yoke	(14-23)	_____

TABLE 4-2 (CONTINUED): A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

Date: _____

	Para (Step)	Value/Checked
4. Oscillator:	4-5	
Frequency: 100 MHz, ±2500 Hz	(1)	_____
Amplitude: -30 dB, ±.1 dBm	(2-5)	_____
5. RF Control:	4-6	
Syn #1		
Tune offset cal @ 50.0000 MHz: 0V, ±1V	(3)	_____
Tune offset cal @ 50.0999 MHz: 0V, ±1V	(4)	_____
Regenerative divider: smooth operation	(5,6,7)	_____
Sampler offset: 0 V, ±5 mV	(8-9)	_____
VCO:		
Low limit: 1325 MHz	(12)	_____
High limit: 2390 MHz	(13)	_____
VCO Sampler DAC:		
Tune offset @ 1350 MHz: 0V, ±1V	(15)	_____
Tune gain @ 2300 MHz: 0V, ±1V	(16)	_____
Sampler Loop/Syn #1 disp. gain:		_____
Centered	(20)	_____
Sampler DAC tune dispersion gain:		
Centered	(21)	_____
RF null cal: -45 dBm < RF < -35 dBm	(22)	_____
6. Amplitude:	4-7	
Auto cal OFF	(1)	_____
Receive IF level cal @ -10 dBm:		
10.7 MHz	(4-6)	_____
Resolution BW levels		
3 MHz	(7-8)	_____
300 kHz	(10)	_____
30 kHz	(11)	_____
3 kHz	(12)	_____
300 Hz	(13)	_____
10 dB LOG cal: ±0.5 dB	(14-29)	_____
2 dB LOG cal: ±0.1 dB	(30-34)	_____

TABLE 4-2 (CONTINUED): A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

Date: _____

	Para (Step)	Value/Checked
6. Amplitude (Continued):		
LINEAR: Within 2%	(35-39)	_____
Auto Cal OFF Level: -10 dB ±0.5 dB @ 225 MHz	(42)	_____
Auto Cal ON level: -10 dB ±0.5 dB @ 225 MHz	(43-47)	_____
IF Gain linearity: ±2 dB	(48)	_____
RF Attenuation linearity ±0.5 dB	(49)	_____
Sweep flatness: ±2 dB	(51)	_____
IF filter flatness: ±2 dB	(52-54)	_____
Noise floor: -125 dBm	(55-57)	_____
Sidebands: ±65 dBc	(58-59)	_____
Video filter: 300 Hz	(60-64)	_____
Base Line Rise: -70 dBc max, ±5 kHz	(65-66)	_____
Spurious Signal Level	(67-68)	_____
75Ω Test: level rises 6 dB	(69)	_____
7. 10.7 MHz Receiver (Option):	4-8	
Bandpass on RCVR Menu: FM2 (200 kHz bandpass)	(5-6)	_____
Bandpass on FM1: 15 kHz bandpass	(9)	_____
Bandpass on AM1: 6 kHz bandpass		
Distortion:		
FM2 Audio: 6V p-p, >5% distortion	(13-16)	_____
FM1: 6V p-p, >3 distortion	(17)	
AM1 & AM2: >1% distortion	(18-19)	_____
Sensitivity: 10 dB SINAD, -71 dBm or less	(20-21)	_____
SSB Injection: 1V p-p	(22-24)	_____
Squelch: Audio present	(25)	_____
Audio Blanking: Audio present TSR	(26-27)	_____
8. Tracking Generator (Option):	4-9	
Tracking Adjust: -3 kHz to +6 kHz from CF	(1)	_____
Output level adjust: (-10 dB)	(2-3)	_____
Gen Keys: 0 to -75 dB Atten	(8-10)	_____
75Ω test display level: Decreases 6 dB	(11-12)	_____
Harmonics less than 20 dBc	(13-14)	_____

TABLE 4-2 (CONTINUED): A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

Date: _____

	Para (Step)	Value/Checked
8. Tracking Generator (Option):	4-9	
Non-harmonics less than 40 dBc	(13-14)	_____
Frequency Deviation (Residual FM):		
±100 Hz (RMS PEAK) @ 100 MHz	(15-16)	_____
External Amp: +11.7V, ±0.2V	(17)	_____
9. Quasi-Peak (Option):	4-10	
FILTERS CHECK		
Levels OK	(14)	_____
TC1 (200 Hz) Bandwidth (170-220 Hz)	(18)	_____
Shape within limits	(18)	YES/NO
TC2 (9 kHz) Bandwidth (±1 kHz)	(20)	_____
Shape within limits	(21)	YES/NO
TC3 (120 kHz):		
Freq Accuracy (±60 kHz)	(25)	_____
Bandwidth (±20 kHz)	(27)	_____
Shape within limits	(28)	YES/NO
PULSE MEASUREMENTS		
TC3 (120 kHz):		
CW Level (A) (dBµV)	(6)	_____
1st Zero Crossing (δF_3 MHz)	(7)	_____
Top of Screen Level (dBµV)	(14)	_____

PRF (Hz)	RANGE (dBµV)		ACTUAL:
100	60.0 (±2.0)	(18)	_____
1000	68.0 (±1.5)	(22)	_____
20	51.0 (±1.5)	(24)	_____
10	46.0 (±1.5)	(27)	_____
2	34.0 (±2.0)	(29)	_____
1	31.5 (±2.0)	(31)	_____
ISOLATED PULSE	28.5 (±2.0)	(33)	_____

TABLE 4-2 (CONTINUED): A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

Date: _____

	Para (Step)	Value/Checked
9. (Continued)		
TC2 (9 kHz):		
CW Level (A) (dBμV)	(38)	_____
1st Zero Crossing (δF_2 MHz)	(39)	_____
Top of Screen Level (dBμV)	(44)	_____
PRF (Hz) / RANGE (dBμV)		ACTUAL:
100 60.0 (±2.0)	(48)	_____
1000 64.5 (±1.0)	(52)	_____
20 53.5 (±1.0)	(54)	_____
10 50.0 (±1.5)	(56)	_____
2 39.5 (±2.0)	(58)	_____
1 37.5 (±2.0)	(60)	_____
ISOLATED PULSE 36.5 (±2.0)	(62)	_____
TC1 (200 Hz):		
CW Level (A) (dBμV)	(67)	_____
1st Zero Crossing (δF_1 MHz)	(68)	_____
Top of Screen Level (dBμV)	(73)	_____
PRF (Hz) / RANGE (dBμV)		ACTUAL:
25 60.0 (±2.0)	(77)	_____
60 63.0 (±1.0)	(81)	_____
100 64.0 (±1.5)	(83)	_____
10 56.0 (±1.0)	(85)	_____
5 52.5 (±1.5)	(87)	_____
2 47.0 (±2.0)	(89)	_____
1 43.0 (±2.0)	(91)	_____
ISOLATED PULSE 41.0 (±2.0)	(93)	_____

TABLE 4-2 (CONTINUED): A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

Date: _____

	Para (Step)	Value/Checked

9. (Continued)

IMPULSE MEASUREMENTS

TC3:

PRF (Hz)	RANGE (dBμV)	CALC'ED (dBμV)	ACTUAL (dBμV)
100	40.0 (±2.0)	(5) _____	(5) _____
40	D_3 (±1.0)	(6) _____	(7) _____

TC2:

PRF (Hz)	RANGE (dBμV)	CALC'ED (dBμV)	ACTUAL (dBμV)
100	10.0 (±2.0)	(13) _____	(13) _____
20	D_2 (±1.5)	(14) _____	(15) _____

TC1:

PRF (Hz)	RANGE (dBμV)	CALC'ED (dBμV)	ACTUAL (dBμV)
20	10.0 (±2.0)	(21) _____	(21) _____
10	D_1 (±1.0)	(22) _____	(23) _____
60	S_1 (±1.0)	(24) _____	(25) _____

NOTES: 1. When errors occur relative to high repetition rate, check the resolution bandwidth calibration of the unit.

2. When errors occur relative to low repetition rate, check time constant calibration in the Quasi-peak Assembly.

4-2 POWER SUPPLY CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 DC Voltmeter--Any

1 Insulated Tuning Tool

1 Battery Load Simulator (IFR Part No. 1003-9801-600)--See Appendix D

1 DC Power Supply--Variable from +10.9V to +30V Current--5A (Surges to 15A)

FIGURE REFERENCES:

Figure 5-2	Power Supply Assembly
FIgure 5-17	Interface PC Board Assembly
Figure 4-23	Composite and Adjustments

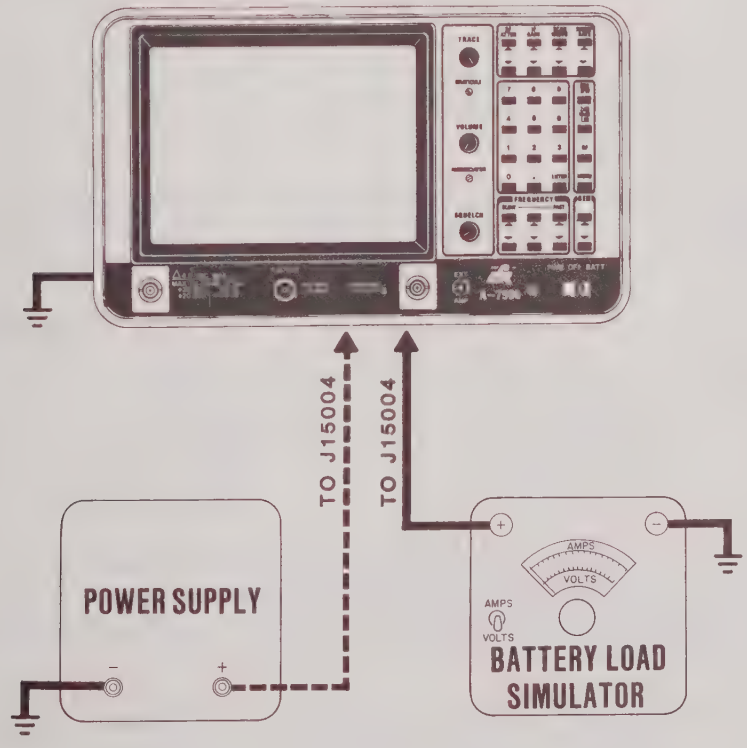


Figure 4-1 Power Supply Calibration Test Setup

WARNING! THE DIFFERENCE OF POTENTIAL BETWEEN THE FLOATING GROUND AND CIRCUIT OR CHASSIS GROUND CAN EXCEED 300 V. THIS POTENTIAL CAN CAUSE SERIOUS INJURY OR EVEN DEATH. ALWAYS USE AN ISOLATION TRANSFORMER AND TAKE EXTREME CARE WHEN WORKING WITH AC VOLTAGES INSIDE THE POWER SUPPLY MODULE.

STEP PROCEDURE

Power Supply Lines

1. Test resistance between Power Supply lines and chassis ground as follows:

Line	Pin # of J15003	Resistance
+12V (red)	1,2	>20Ω
+5V (orange)	4,5	>100Ω
-12V (yellow)	7	>300Ω
+40V (green)	12	>15KΩ

2. Connect AC power cord to A-7550 and place PWR/OFF/BATT switch to "PWR".

3. Verify Power Supply output voltage on Power Supply lines as shown on chart below. If necessary, adjust indicated trimpot to desired voltage level.

Line	Tolerance	Adjustment
+16 V (blue)	±0.5 V	R17068
+12 V (red)	±0.2 V	R17056
+5.2 V (orange)	±0.05 V	R17062
-12 V (yellow)	±0.5 V	None (tracks +12 V line)
+40 V (green)	+32 V to +45 V	None (tracks +12 V line)

NOTE: To gain access to the adjustment holes in the Power Supply, the Receive IF Module must be moved. Leave hard-wire connections attached to these modules if they are moved.

NOTE: The +16V line is only used in the Power Supply. If other lines are within tolerance, checking the +16V line is not necessary.

Batt Charge

4. Remove bracket covering battery to gain access to battery connector (J15004). Disconnect J15004 from the battery.

STEP	PROCEDURE

5. Connect the Battery Load Simulator to J15004 (Figure 4-1).

6. Verify a battery charge voltage of +14.5V at a 0.3A load. If necessary, adjust R17006 (BATT CHARGE) to desired level.

CAUTION: IN STEP 7, DO NOT LEAVE BATTERY LOAD SIMULATOR SET TO MAXIMUM CURRENT LOAD FOR AN APPRECIABLE LENGTH OF TIME. A QUICK GLANCE IS ALL THAT IS NECESSARY. THIS PREVENTS POSSIBLE DAMAGE TO THE SET.

Current Limit

7. Set Battery Load Simulator to give a maximum current load. Verify that battery charge current limit is between 1.1A and 1.7A. Disconnect Battery Load Simulator from J15004.

Batt Monitor

8. Measure the voltage at pin 4 of U19007 (IC) on the Interface PC Board. If the voltage is not +5 V (±0.1 V), adjust R19029 (BATT REF ADJ), as necessary, to the desired voltage.

9. Measure the voltage at pin 8 of U19007 (IC) on the Interface PC Board. If the voltage is not +7.5 V (±0.1 V), adjust R19030 (BATT CAL), as necessary, to the desired voltage.

Battery Operation

10. Turn set OFF. Disconnect AC power cord from A-7550. Connect variable DC power supply, set at +14.2 VDC, to J15004 (battery connector - Figure 4-1). Turn set on to "BATT".

Voltage Display

11. Select TEST menu on the A-7550. Vary the DC Power Supply in half-volt increments from +11.5V to +15V. At each increment, select "5" on the TEST menu to measure battery charging voltage. Verify that BATT voltage changes for each half-volt increment on CRT.

Low Voltage Cutoff

12. Slowly decrease DC power supply voltage and verify that the set turns off between +11.0V and +11.8V.

Batt Timer

13. Increase DC power supply to approximately +14V. Toggle the PWR/OFF/BATT Switch to "BATT" to turn on the battery power. Verify battery timer operation by observing the A-7550 shuts off in 10 minutes (±2 minutes).

STEP	PROCEDURE

Line Interrupt

14. Disconnect DC power supply. Connect J15004 to battery and connect AC power to A-7550. Set PWR/OFF/BATT Switch (2) to "PWR".

15. Remove AC power cord and verify the A-7550 continues to operate for at least 2 seconds. This is not a critical time period. Merely verify there is some delay.

External DC

16. Connect DC power supply, set at +12 to +30 VDC, to DC input connector on A-7550. Set PWR/OFF/BATT Switch (2) to "PWR". Verify A-7550 operates with +12 to +30 VDC input.

4-3 DISPLAY CALIBRATION

SPECIAL ACCESSORY
EQUIPMENT REQ'D: 1 Insulated Tuning Tool--w/Common Tip

FIGURE REFERENCES: Figure 5-4 Front Panel & Keyboard

STEP PROCEDURE

NOTE: If the CRT display is skewed, rolling or tilted in the following steps, go to Paragraph 4-4, CRT Calibration.

1. Connect AC power cord to A-7550. Set PWR/OFF/BATT Switch (2) to "PWR".

Reset to LOGO

2. Verify IFR logo is present on CRT display. Press any key on the keyboard and verify analyzer grid is present on CRT display or grid appears within 8 seconds.

Grid Display Alignment

3. Verify grid is correct in size and shape (straight lines and square corners).

Alpha Display

4. Verify alpha display (letters and numbers) is clear and legible.

Keyboard Operation

5. Verify keyboard controls alpha display.

Keyboard Annunciator Adjustment

6. Verify "beep" is audible when keys are pressed. Adjust ANNUNCIATOR pot on front panel for desired audible level.

Graticule Intensity Adjustment

NOTE: If the brightness intensity is too low in the following steps, do Steps 7 through 9 of Paragraph 4-4 to adjust master brightness level.

7. Verify grid display brightness is variable. Adjust GRATICULE Intensity Adjust (IA) (13) on front panel for desired brightness (see NOTE above).

STEP	PROCEDURE

Trace Intensity Adjustment

8. Verify alpha display brightness is variable. Adjust TRACE Intensity Adjust (IA) (14) on front panel for desired brightness (see NOTE in Step 7, above).

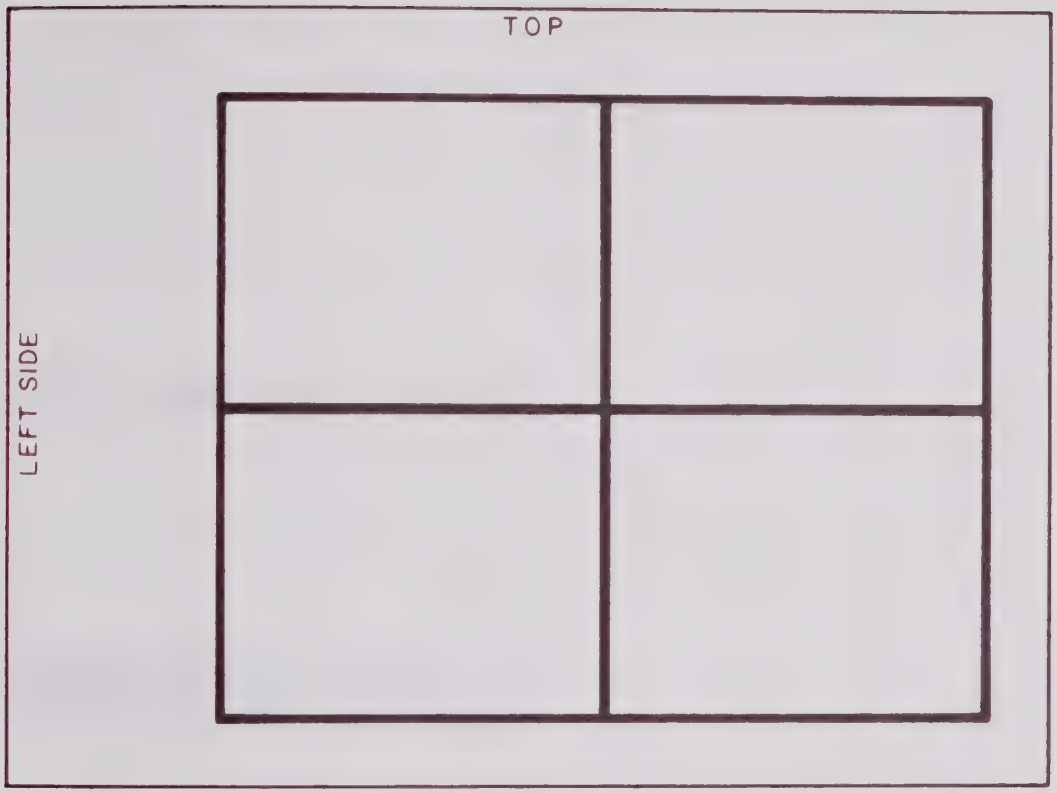


Figure 4-3 Overlay For CRT Calibration.

4-4 CRT CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Insulated Tuning Tool

1 Insulated Hex (0.100) Tuning Tool

FIGURE REFERENCES: Figure 4-23 Composite and Adjustments
Figure 5-29 CRT Display Assembly

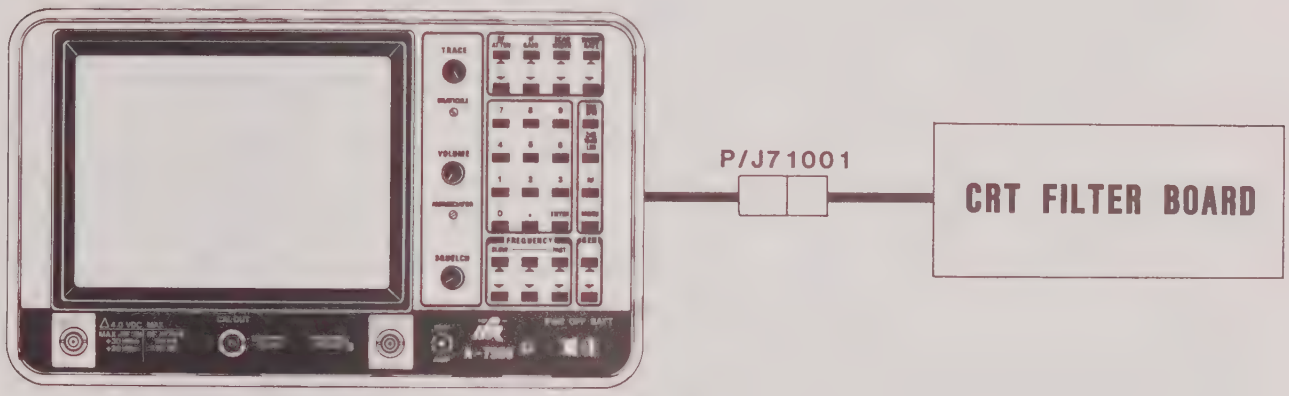


Figure 4-2 CRT Calibration Test Setup

NOTE: This procedure is performed only as needed.

STEP PROCEDURE

WARNING! HIGH VOLTAGES ARE PRESENT ON THE CRT MODULE DURING OPERATION. DO NOT TOUCH ANY METAL PARTS ON THE CRT SATELLITE PC BOARD. KEEP HANDS AWAY FROM METAL CONNECTIONS ON TOP AND BOTTOM OF YOKE.

1. Disconnect J71001 on the CRT Filter Board and remove CRT Assembly from A-7550.

2. Remove Figure 4-3 (Overlay for CRT Calibration) from manual. Cut on outside of line as indicated. Carefully center the cut line within the white viewing area of the CRT and, using transparent tape, tape overlay onto face of the CRT. The dimensions of the cut line are the dimensions of the CRT bezel when the CRT is mounted in the set. The cut edge of the overlay will be approximately the same as the white part of the CRT.

STEP	PROCEDURE

NOTE: At all times during this procedure, keep the CRT Module oriented so that the display faces magnetic North or South. This will keep any earth magnetic effects from distorting the display after reinstallation of the mu-metal shield.

3. Connect J71001 on the CRT Filter Board to P71001. (Fabricating an extender cable may be necessary.)

4. Set R203 (CONTRAST) as far as possible to the left and VR200 (FOCUS) as far as possible to the right.

5. Preset pots to the following specifications:

   A. R71006 (VERT) on CRT Filter Bd. - midrange

   B. R71004 (WIDTH) on CRT Filter Bd. - midrange

   C. R71005 (INTERLACE) on CRT Filter Bd. - midrange

   D. VR103 (VIDEO) on CRT Main Bd. - fully CW

   E. R71012 (MASTER BRIGHT) is on CRT Filter Bd for later sets.

   F. VR200 (FOCUS) on CRT Satellite Bd. - midrange

   G. TRACE Intensity Adjust on Front Panel - fully CW

   H. GRATICULE Intensity Adjust on Front Panel - fully CW

6. Set PWR/OFF/BATT Switch (2) to "PWR". Wait 30 seconds for warmup.

7. IFR logo should appear, but may be unstable. Adjust R71012 (MASTER BRIGHT) until the green background just disappears.

8. Adjust R71006 (VERT) until the image stops rolling vertically. Adjust in one direction if image rolls up, adjust in the other direction if image rolls down. Adjust midway between rolls.

9. Adjust R71004 (WIDTH) until logo covers about 3/4 of screen width.

10. Adjust R71005 (INTERLACE) until the display is stable horizontally.

11. Press any key on the KEYBOARD (1). The graticules should then be displayed. Using eyepiece, adjust VR200 (FOCUS) until the lettering at the top edge is at its sharpest.

STEP	PROCEDURE

12. Set TRACE Intensity Adjust (14) and GRATICULE Intensity Adjust (13) for comfortable viewing.

13. Observe graticules (horizontal and vertical) to see if the yoke is properly positioned. If both horizontal and vertical graticules seem to be turned slightly in the same direction, rotate the yoke as described in Step 14. Otherwise, go to Step 15.

14. Loosen Phillips-head screw on back of yoke. Carefully cut into putty on front of tube so wires are not cut or broken. Twist gently to break the putty bond, holding the yoke to the tube. Rotate yoke until the center horizontal graticule line is perfectly horizontal. Tighten Phillips-head screw.

    NOTE: There are eight evenly-spaced square magnets at the front of the deflection yoke. One edge of the magnets is identified with a color code indicating magnetic strength as follows:

    Yellow - Weakest
    Green
    Red
    Blue
    Large White - Strongest (Avoid)

    The magnets should not need adjustment unless they have been moved or if the yoke and/or CRT have been replaced.

    The magnets affect the display as shown in Figures 4-4 and 4-6. Avoid rotating magnets unless abnormal effects result, as shown in Figures 4-4 and 4-6.

    If alignment cannot be accomplished, a weaker or stronger magnet may have to be substituted for any of the existing magnets.

15. Rotate each of the corner magnets (see Figure 4-4) in turn, to square up the corners.

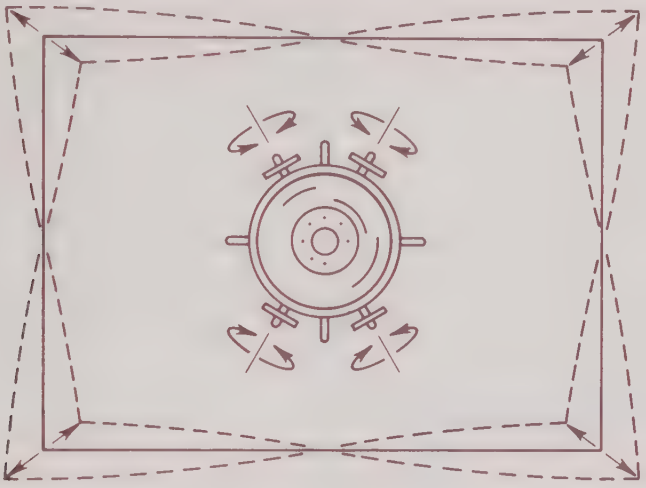


Figure 4-4 Trapezoidal Adjustments

16. There are two black centering tabs (ring magnets) toward the back of the yoke (see Figure 4-5). These center the display. Adjust the tabs to align the graticules with the furnished overlay.

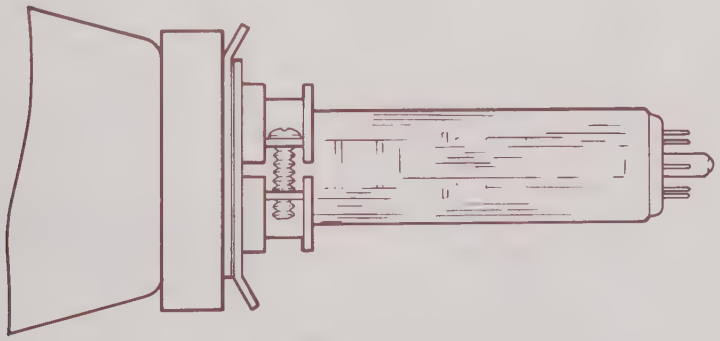


Figure 4-5 Partial View of CRT Neck/Deflection Yoke

17. Adjust the two side magnets and the two top magnets (see Figure 4-6) to align the sides of the display.

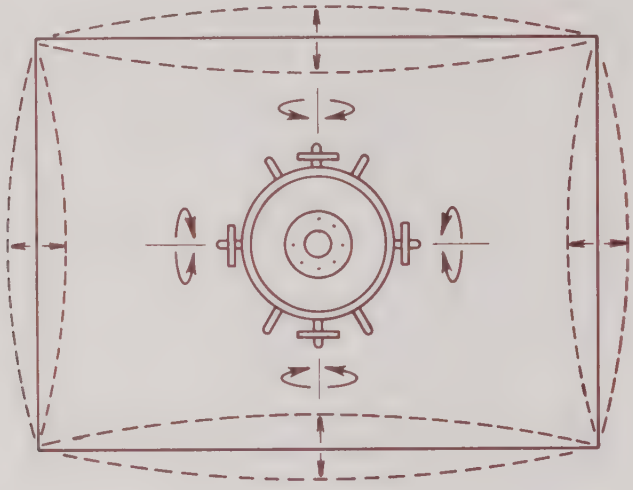


Figure 4-6 Pincushion/Barrel Adjustments

18. If necessary, readjust the black centering tabs.

    NOTE: R71004 (WIDTH) may have to be adjusted to align the width of the display with the furnished overlay.

19. Repeat Steps 13 through 18 until display is aligned.

20. Install mu-metal shield and observe display. Adjust WIDTH and HEIGHT (R71004 and L101) and, if necessary, the right edge of screen (R103) to align display. It may also be necessary to adjust the magnets and centering tab to align the display.

21. Demagnetize the mu-metal before replacing it on the PC board assembly. When the mu-metal is reinstalled, observe the display. Repeat Step 20 until the display is aligned.

22. If the yoke was rotated in Step 14, apply putty to the front of the yoke to secure the yoke to the glass tube. Keep the putty away from the wires in the yoke.

23. Install CRT Module in set and observe display. If display is acceptable, this procedure is complete; otherwise, repeat Steps 13 through 22.

4-5 REFERENCE OSCILLATOR CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Spectrum Analyzer

1 Frequency Counter

1 RF Signal Generator

1 Power Meter w/Thermistor Mount

FIGURE REFERENCES: Figure 5-20 Reference Oscillator Assembly
Figure 4-23 Composite and Adjustments

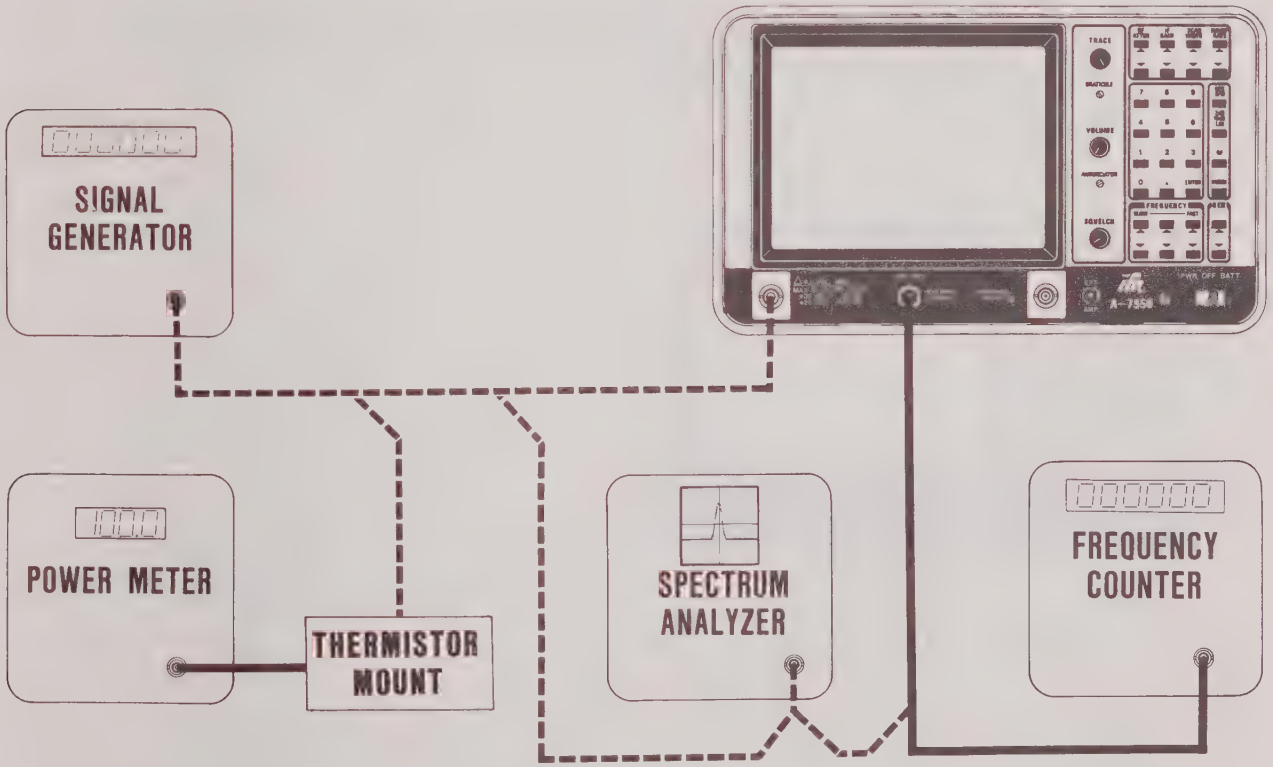


Figure 4-7 Reference Oscillator Calibration Test Setup

STEP	PROCEDURE

Frequency

1. Using Frequency Counter, measure the reference frequency at CAL OUT Connector on A-7550. Verify frequency is 100 MHz (±2500 Hz) at room temperature. Adjust L47002 (REF FREQ) in Reference Oscillator module.

STEP	PROCEDURE

Amplitude

2. Disconnect Frequency Counter. Set RF Signal Generator to 100 MHz at -30 dBm and verify level with Power Meter.

3. Connect RF Signal Generator to an external Spectrum Analyzer and note signal level.

4. Disconnect RF Signal Generator.

5. Then, using the same coax cable used in Step 2, connect CAL OUT (9) to external Spectrum Analyzer. Verify signal level is the same as noted in Step 2 (±0.1 dB). If necessary, adjust R47025 (CAL ADJ) in Reference Oscillator Module.

   NOTE: Reference Frequency and CAL ADJ interact, some times as much as 2 dB and/or 500 kHz. Repeat Step 1 after adjusting R47025 or L47002.

4-6 RF CONTROL CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Oscilloscope

1 DC Power Supply

1 Digital Voltmeter

1 Tune Control Pot--Appendix D

1 Spectrum Analyzer

FIGURE REFERENCES:

Figure 4-23 Composite and Adjustments
Figure 5-7 Receive IF Assembly
Figure 5-17 Interface PC Board Assembly
Figure 5-20 Reference Oscillator Assembly
Figure 5-22 First LO Sampling Loop Assembly
Figure 5-25 Synthesizer #1 Assembly

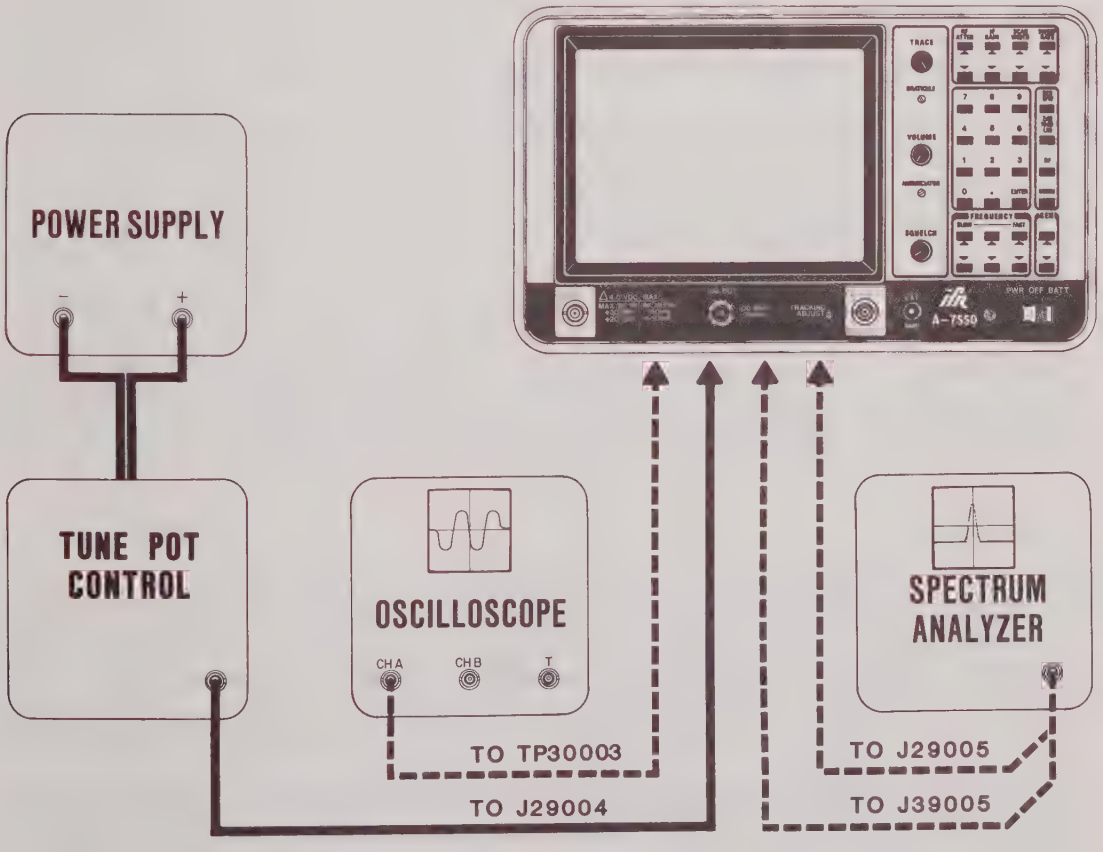


Figure 4-8 RF Control Calibration Test Setup

STEP PROCEDURE

1. Connect test equipment (Figure 4-8) and AC power cord to A-7550 Spectrum Analyzer. Place PWR/OFF/BATT Switch (2) to "PWR".

2. Set SCAN WIDTH to 0 kHz/DIV and center frequency to 50.0000 MHz. (Press: RF 50. ENTER).

Syn. #1 Tune Offset

3. Verify 0 VDC (±1 V) is present at TP23001 in Synthesizer #1 module If necessary, adjust R19013 (SYN #1 OFFSET) on Interface Board to desired voltage level.

Syn. #1 Tune Gain

4. Select 50.0999 MHz as center frequency. (Press: RF 50.0999 ENTER). Verify 0 V (±1 V) at TP23001. If necessary, adjust R19007 (SYN #1 GAIN) on Interface Board to desired voltage level.

Regenerative Divider

5. Remove jumper from JTB30001 on 1st LO Sampling Loop Module. Disconnect coax #11 from J29004 on 1st LO Sampling Loop Module. Put a tee on J29004 and connect coax #11 on one side of tee. Connect Tune Control Pot to other side of tee.

6. Connect an external Spectrum Analyzer to J39005 on 1350-2350 MHz VCO Module. (Disconnect coax #13 from J39005 if Tracking Generator option is installed.) Manually tune the VCO from 1325 to 2450 MHz with the Tune Control Pot to verify manual control of the VCO frequency.

7. Connect an Oscilloscope to TP30003 on the 1st LO Sampling Loop module. While manually tuning the VCO between 1325 MHz and 2450 MHz, verify a smooth voltage change on the Oscilloscope (i.e., -2 to -4 V). If necessary, adjust R30033 (DIVIDER TUNE GAIN) in 1st LO Sampling Loop Module to desired voltage level (i.e., -2 to -4 V).

Sampler Offset

8. Manually tune the VCO for a 1500 MHz signal display on the external Spectrum Analyzer. Disconnect external Spectrum Analyzer from J39005, and connect it to J29005 in the 1st LO Sampling Loop module. Adjust external Spectrum Analyzer until signal is centered on 0 MHz with 5 MHz/DIV scan width. Adjust Tune Control Pot until the tallest spurs are within 5 MHz from the signal center.

9. Using digital voltmeter, measure DC voltage at TP30004 on 1st LO Sampling Loop Module. If the voltage is not 0 VDC (±5 mV), adjust R30070 (SAMPLER OFFSET) in the 1st LO Sampling Loop module to the desired voltage level.

STEP	PROCEDURE

10. Disconnect external Spectrum Analyzer from J29005 and connect it to J39005 on the 1350-2350 MHz VCO Module. Connect coax #12 to J29005. Disconnect tee from J29004 and connect coax #11 to J29004. Install jumper on JTB30001.

CAUTION: HEREON, DO NOT ALLOW THE DC POWER SUPPLY TO EXCEED +5 VDC. IT SHOULD BE SET TO 0 VDC BEFORE CONNECTING TO J29002.

Low Limit Cal

11. Disconnect coax #18 from J29002 on the 1st LO Sampling Loop module. Connect Tune Control Pot to J29002 for manual tuning. Verify manual control from 1325 MHz to 2450 MHz as seen on external Spectrum Analyzer.

12. Manually tune the VCO below 1350 MHz as displayed on the external Spectrum Analyzer. Adjust R30049 (LOW LIMIT) in the 1st LO Sampling Loop module to stop VCO frequency at 1325 MHz.

High Limit Cal

13. Manually tune the VCO above 2350 MHz as displayed on the external Spectrum Analyzer. Adjust R30045 (HIGH LIMIT) on the 1st LO Sampling Loop module to stop VCO frequency at 2390 MHz.

Sampler DAC Tune Offset

14. Disconnect Tune Control Pot from J29002. Connect coax #18 to J29002. Set SCAN WIDTH to 0 kHz/DIV and set 0.0050 MHz center frequency on A-7550 (Press: RF 0 ENTER).

15. Verify 1350 MHz VCO frequency as read on external Spectrum Analyzer. Verify voltage on TP30007 on 1st LO Sampling Loop module is 0V (±1V). If necessary, adjust R19009 (SAMPLER OFFSET) on the Interface PC Board, to desired voltage level.

Sampler DAC Tune Gain

16. Select 950.0 MHz center frequency on A-7550. Verify VCO frequency as read on external Spectrum Analyzer is 2300 MHz. Verify voltage at TP30007 is 0V (±1V). If necessary, adjust R19005 (SAMPLER GAIN) on the Interface PC Board.

17. Repeat Steps 15 and 16 and verify voltage at TP30007 is 0 V (±1 V).

18. Disconnect External Spectrum Analyzer from J39005 and connect coax #13 (if Tracking Generator is installed) to J39005.

STEP	PROCEDURE

Sampler Loop/SYN #1 Dispersion Gain

19. Connect COAX from CAL OUT to ANALYZER INPUT. Press key sequence: RF ENTER to select full scan operation.

20. Reset SCAN WIDTH to 500 kHz/DIV and adjust R19021 (SYN #1 SWEEP GAIN) on the Interface Board, to center 500 MHz signal (±1.25 minor divisions) of center graticule. Step down scan width to verify 500 MHz signal stays within 1.25 minor divisions of center frequency division.

    NOTE: R32023 (SWEEP RAMP ADJ) on Sweep Digitizer PC Board may require adjustment if R19021 cannot supply the necessary adjustment to center the 500 MHz signal on the center graticule.

21. Reset the unit to full scan (Press: RF ENTER). If necessary, adjust R19024 (SAMPLER SWEEP GAIN) on Interface PC Board until there is one 100 MHz harmonic/DIV aligned on each major division. The 1000 MHz harmonic should be aligned with the right-most graticule.

RF Null Cal

22. Disconnect CAL OUT (9) from ANALYZER INPUT (10). Select zero Frequency Mode (Press: RF 0 ENTER) and zero SCAN WIDTH (0 kHz/DIV). Remove COAX #34 from J41005 on the Receive IF Module. Connect an External Spectrum Analyzer to J41005. Verify the 189.3 MHz signal level is between -35 and -45 dBm. If necessary, adjust R45002 (1350 MHz NULL #1) and R45003 (1350 MHz NULL #2) in the Receive IF module. Connect Coax #34 to J41005 when finished.

4-7 AMPLITUDE CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF Signal Generator

1 Spectrum Analyzer

1 Power Meter w/Thermistor Mount

FIGURE REFERENCES:

Figure 4-23	Composite and Adjustments
Figure 5-7	Receive IF Assembly
Figure 5-8	Analyzer IF Assembly
Figure 5-11	Spectrum Analyzer Log Amp Assembly
Figure 5-17	Interface PC Board Assembly

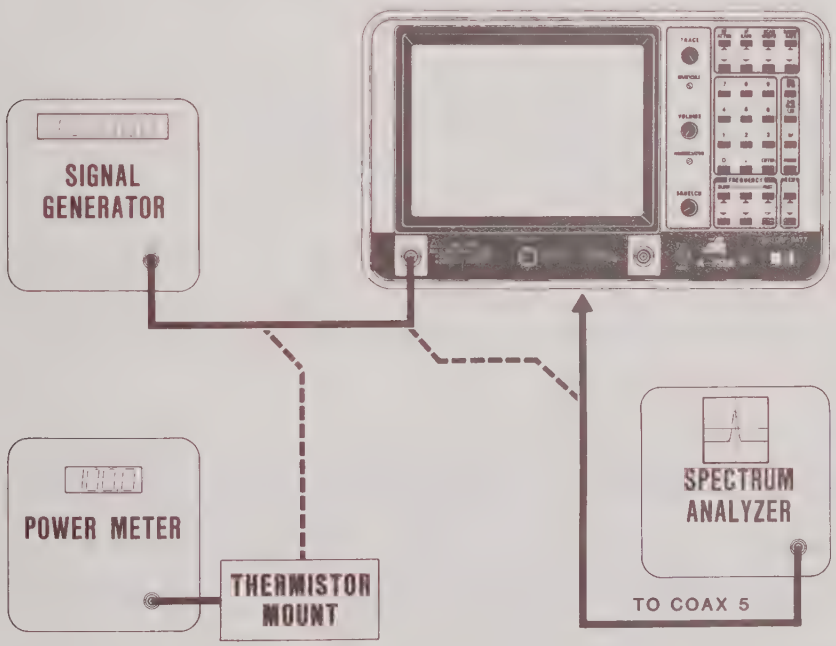


Figure 4-9 Amplitude Calibration Test Setup

STEP PROCEDURE

Auto Cal OFF

1. Jumper together the two posts of JTB19001 on the Interface PC Board to disable Auto-Cal.

2. Connect AC power cord to A-7550. Set PWR/OFF/BATT Switch (2) to "PWR".

3. Set the following CRT values:

CONTROL	SETTING
Center Frequency	225.0000 MHz
SCAN WIDTH	0
RES BW	3 MHz
RF ATTEN	30 dB
2dB/10dB/LIN Scale	2 dB/DIV
FILTERS menu	None

4. Connect RF Signal Generator to a power meter and set RF Signal Generator output to 10.7 MHz at -10 dBm. Disconnect power meter and connect external Spectrum Analyzer, set at 10.7 MHz center frequency and 2 dB/DIV, to output of RF Signal Generator. Note or store the calibrated signal level.

Receive IF Level Cal

5. Disconnect coax #5 from J41008 on the Receive IF Module. Connect an external Spectrum Analyzer to coax #5. Connect RF Signal Generator, set to 225 MHz at -10 dBm as calibrated on a power meter, to ANALYZER INPUT (10) on A-7550.

6. Verify signal is 10.7 MHz at -10 dBm to -14 dBm. (Signal level may be as low as -14 dBm, if the remainder of the steps in this procedure are to be accomplished.) If necessary, adjust R42029 (IF GAIN ADJ) in Receive IF module to set level.

3 MHz BW

7. Connect coax #5 to J41008. Disconnect coax #6 from J26003 on LOG AMP module. Connect an external Spectrum Analyzer to coax #6.

8. Verify signal is 10.7 MHz at -10 dBm, ±0.5 dB. If necessary, adjust R22020 (IF LEVEL GAIN) in Analyzer IF module to desired signal level. Connect coax #6 to Log Amp.

9. Press SCAN WIDTH pushbutton (up) until scan width setting is 2 kHz/DIV. Select the 3 MHz B/W again. Note, or store in memory, the trace level on the CRT display.

300 kHz BW

10. Select 300 kHz RES BW. Verify trace level is identical to Note in Step 9. If necessary, adjust R22015 (300 kHz LEVEL ADJ) in Analyzer IF module to desired level.

STEP PROCEDURE

30 kHz BW

11. Select 30 kHz RES BW. Verify trace level is the same as noted in Step 9. If necessary, adjust R22031 (30 kHz LEVEL ADJ) in Analyzer IF module to desired level.

3 kHz BW

12. Select 3 kHz RES BW. Verify trace level is the same as noted in Step 9. If necessary, adjust R22052 (3 kHz LEVEL ADJ) in Analyzer IF module to desired level.

300 Hz BW

13. Select 300 Hz RES BW. Verify trace level is the same as noted in Step 9. If necessary, adjust R22087 (300 Hz LEVEL ADJ) in Analyzer IF module to desired level.

10 dB LOG Cal Linearity

14. Set the following CRT values:

CONTROL	SETTING
Center Frequency	225 MHz
SCAN WIDTH	5 kHz/DIV
RES BW	3 kHz
RF ATTEN	30 dB
IF GAIN	0
2dB/10dB/LIN Scale	10 dB/DIV
FILTERS Menu	None

15. Set RF Signal Generator to 225 MHz at -70 dBm. Connect RF Signal Generator to ANALYZER INPUT Connector.

16. Verify -70 dBm (±0.5 dB) on the CRT. If necessary, adjust R26151 (10 dB OFFSET) in the Log Amp module to the desired level.

17. Recalibrate RF Signal Generator to 225 MHz at -10 dBm.

18. Verify -10 dBm (±0.5 dB) on the CRT. If necessary, adjust R26161 (10 dB GAIN) in the Log Amp module to desired level. If adjustment was necessary, repeat Steps 15 through 18.

19. Recalibrate RF Signal Generator to 225 MHz at 0 dBm.

20. Verify the signal is within 0.5 dB from the top of the screen display. If necessary, adjust R26066 (REF LINE COMPRESSOR) in the Log Amp module. If adjustment was necessary, repeat Steps 15 through 18.

STEP	PROCEDURE

21. Recalibrate RF Signal Generator to -60 dBm, -50 dBm and -40 dBm. If the corresponding levels on the CRT are within 0.5 dB, go to Step 25. If not, continue at Step 22.

22. Recalibrate RF Signal Generator to -50 dBm.

24. Observe the error on the CRT. If necessary, adjust R26097 (LOG LINEARITY LOW) in the Log Amp Module for twice the error shown. Repeat Steps 15 through 18.

25. Recalibrate RF Signal Generator to -20 dBm, -30 dBm and -40 dBm.

26. If the corresponding levels on the CRT are within 0.5 dB, go to Step 29. If not, continue at Step 27.

27. Recalibrate RF Signal Generator to -30 dBm.

28. Observe the error on the CRT. If necessary, adjust R26074 (LOG LINEARITY HIGH) in the Log Amp module for twice the error shown. Repeat Steps 15 through 18.

29. Step RF Signal Generator in 10 dB increments from -70 dBm to 0 dBm Verify at each increment that each corresponding level on the CRT agrees with 0.5 dB.

2 dB LOG Cal Linearity

30. Select 2 dB/DIV scale. Recalibrate RF Signal Generator to -10 dBm.

31. Verify a -10 dBm (±0.5 dB) level on the CRT. If necessary, adjust R26156 (2 dB OFFSET) in the Log Amp module to desired level.

32. Recalibrate RF Signal Generator to 0 dBm.

33. Verify a 0 dBm (±0.5 dB) level on the CRT. If necessary, adjust R26159 (2 dB GAIN) in the Log Amp module to desired level.

34. Repeat Steps 30 through 33 to verify levels are within 0.5 dB of corresponding inputs.

LINEAR

35. Select Linear scale. Recalibrate RF Signal generator to 0 dBm.

36. Verify the top graticule on the CRT agrees with input. If necessary, adjust R26123 (LINEARITY GAIN Adjust) in the Log Amp module to desired level.

37. Disconnect RF Signal Generator.

STEP PROCEDURE

38. Verify the base line on the CRT is on the bottom graticule. If necessary, adjust R26195 (LINEAR OFFSET) in the Log Amp module to desired level.

39. Repeat Steps 35 through 38 to verify Linear calibration is accurate within 2%.

40. Repeat Steps 30 through 34 before Step 41.

41. Set RF Signal Generator to 225 MHz, -10 dBm, and check level with the Power Meter. Reset the following CRT values:

CONTROL	SETTING
Center Frequency	225.0 MHz
SCAN WIDTH	2 kHz/DIV
RES BW	3 MHz
RF ATTEN	30 dB
IF GAIN	0
2dB/10dB/LIN Scale	2 dB/DIV

Auto Cal OFF Level

42. Verify trace on CRT is at -10 dB level (±0.5 dB). If trace is more than 0.5 dB off, restart the calibration procedure from Step 3.

Auto Cal ON Level

43. Remove shorting jumper from JTB19001 on the Interface PC Board to enable Auto Cal.

44. Set PWR/OFF/BATT Switch (2) OFF, then back to PWR to cycle the Auto Cal.

45. Verify trace level on CRT of -10 dB. If necessary, adjust R43010 (AUTO CAL LEVEL) in Receive IF module to desired level. If adjustment was made, set PWR/OFF/BATT Switch (2) OFF, then back to PWR.

46. Repeat Steps 43 through 45 until trace stays at -10 dB after power cycle.

47. Reset the following CRT values:

CONTROL	SETTING
Center Frequency	225 MHz
SCAN WIDTH	2 kHz/DIV
RES BW	3 kHz
RF ATTEN	30 dB
IF GAIN	0
FILTERS Menu	none
2dB/10dB/LIN Scale	10 dB/DIV

IF Gain Linearity

48. Set the RF Signal Generator to 225 MHz at -10 dBm, and check level with Power Meter. Connect RF Signal Generator to ANALYZER INPUT (10) to verify tolerance is met for values shown in Table 4-3. Measure from trace to first graticule down from top.

RF Signal Generator (dBm)	A-7550 IF GAIN (dB)	Tolerance	Actual
-10	0	±2 dB	_____
-20	10	±2 dB	_____
-30	20	±2 dB	_____

Table 4-3 IF GAIN Linearity

RF Attenuation Linearity

49. Select 0 IF GAIN and 0 RF ATTEN. Check RF Signal Generator levels with a Power Meter and make settings as shown in Table 4-4. Measure tolerance from 3rd graticule down from top. If check fails, repair or replace 0-60 dB Input Attenuator.

RF Signal Generator (dBm)	A-7550 RF ATTEN (dB)	Tolerance*	Actual
-60	0	±0.5 dB	_____
-50	10	±0.5 dB	_____
-40	20	±0.5 dB	_____
-30	30	±0.5 dB	_____
-20	40	±1.0 dB	_____
-10	50	±1.0 dB	_____
0	60	±1.5 dB	_____

*Tolerance is cumulative at each stage of the Attenuator up to 1.5 dB total.

Table 4-4 RF Attenuation Linearity

STEP PROCEDURE

50. Reset the following CRT values:

CONTROL	SETTING
Center Frequency	500 MHz
SCAN WIDTH	100 MHz/DIV
RES BW	3 MHz
RF ATTEN	30 dB
IF GAIN	0
SWEEP RATE	20 msec/Div
2dB/10dB/LIN Scale	2 dB/Div

Sweep Flatness

51. Step RF Signal generator from 100 kHz to 999 MHz in 50 MHz increments. At each increment, verify a -10 dBm output level with a power meter and verify A-7550 is within 2 dB of actual level.

52. Reset the following CRT values:

CONTROL	SETTING
SCAN WIDTH	1 kHz/DIV
RES BW	300 kHz
RF ATTEN	30 dB
IF GAIN	0
Center Frequency	100.005 MHz

IF Filter Flatness

53. Set RF Signal Generator to 100.005 MHz at -5 dBm. Connect RF Signal Generator to A-7550 and note, or store, level. Change A-7550 to 100.004 MHz center frequency.

54. Press Slow Scan (-1 step). Verify level is the same (±2 dB), as previously noted or stored. If check fails, repair or replace Receive IF Module.

NOTE: To store a signal and check the stored signal, use the "STORE" and "COMPARE" features in the MODE menu.

Noise Floor

55. Reset the following CRT values:

CONTROL	SETTING
Scan width	1 kHz/DIV
Center Frequency	225 MHz
RES BW	300 Hz
MODE Menu	Average
RF ATTEN	0 dB
Video Filter	300 Hz

56. Disconnect RF Signal Generator.

57. Verify the trace baseline on the CRT is lower than -125 dBm by raising IF Gain. When check is complete, return IF Gain to 0.

Sidebands

58. Connect CAL OUT Connector (9) to ANALYZER INPUT Connector (10). Reset the following CRT values:

CONTROL	SETTING
Center Frequency	100 MHz
SCAN WIDTH	10 kHz/DIV
RES BW	3 kHz

59. Verify sidebands, at five times the resolution BW, are more than 65 dB below the carrier.

Video Filter

60. Disconnect CAL OUT Connector (9) from ANALYZER INPUT Connector (10). Set RF Signal Generator to 100 MHz at -10 dBm, and check level with a Power Meter.

61. Modulate the Generator signal with a 1 kHz signal to 80% AM.

62. Connect RF Signal Generator into ANALYZER INPUT Connector (10). Reset the following CRT values:

CONTROL	SETTING
Center Frequency	100 MHz
SCAN WIDTH	0
RES BW	3 MHz
2dB/10dB/LIN Scale	Linear
FILTERS Menu	None
RF ATTEN	30 dB

63. Reset the FILTERS Menu to 300 Hz.

64. Verify an approximate 60% drop in detected modulation. If no drop is detected in the video, repair the 300 Hz filter in the Log Amp Module.

STEP PROCEDURE

Base Line Rise

65. Set RF Signal Generator to 50 MHz at 0 dBm, with no modulation. Reset the following CRT values:

CONTROL	SETTING
Center Frequency	50 MHz
SCAN WIDTH	1 kHz/DIV
RES BW	300 Hz
RF ATTEN	30 dB
FILTERS Menu	300 Hz

66. Vary the RF Signal Generator frequency slowly across the 50 MHz point. Verify the base line floor at ±5 kHz is not greater than -70 dBc.

Spurious Signal at 100 MHz

67. Set RF Signal Generator to 100 MHz at 0 dBm. Reset the following CRT values:

CONTROL	SETTING
Center Frequency	100 MHz
SCAN WIDTH	20 kHz/DIV

68. Record the level of the spurious signal, if any, about 30 kHz above 100 MHz on the CRT.

75Ω Test

69. Select 75Ω on the SETUP menu. Verify signal level on the CRT rises 6 dB. When test is complete, select 50Ω on the SETUP menu.

4-8 10.7 MHz RECEIVER CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Oscilloscope

1 RF Signal Generator

1 Distortion Analyzer

1 Spectrum Analyzer

FIGURE REFERENCES: Figure 4-23 Composite and Adjustments
Figure 5-10 10.7 MHz Receiver Assembly

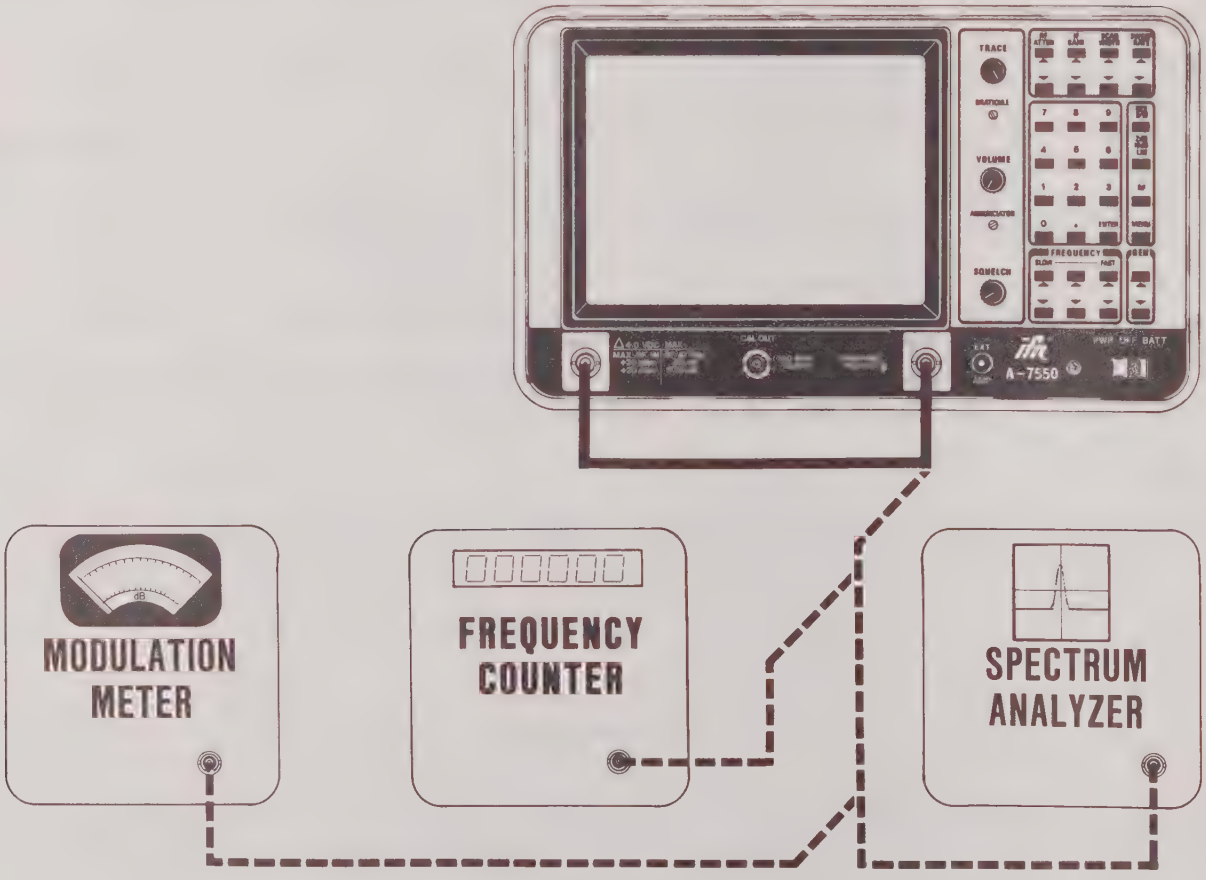


Figure 4-10 10.7 MHz Receiver Calibration Test Setup

STEP	PROCEDURE
1.	Remove coax cable from 10.7 MHz Receiver and 10.7 MHz Receiver module from its slot. Remove 10.7 MHz Receiver PC board from can. Using extender board, reinstall 10.7 MHz Receiver PC Board. Do not connect coaxes.

STEP	PROCEDURE

2. Set the CRT to the following values:

CONTROL	SETTING
SCAN WIDTH	0
RCVR Menu	FM2

3. Terminate J57003 on 10.7 MHz Receiver PC Board with a 50Ω termination.

4. Connect RF Signal Generator output, set at 10.7 MHz at -60 dBm, to J57002.

5. Connect external Spectrum Analyzer input to TP57001 on 10.7 MHz Receiver Module.

6. Center external Spectrum Analyzer on 10.7 MHz at 50 kHz/DIV. Adjust 200 kHz bandpass for maximum and best shape using FL58001, FL58003, FL58004 and FL58005.

7. Connect Oscilloscope to TP58002 on 10.7 MHz Receiver PC board.

8. Adjust FL58006 for maximum AGC as shown on Oscilloscope.

9. Select "FM1" in RCVR menu. Set external Spectrum Analyzer to 5 kHz/DIV. Adjust 15 kHz bandpass for maximum and best shape using C58029, C58030, C58034 and C58035.

10. Select "AM1" in RCVR menu. Set external Spectrum Analyzer to 2 kHz/DIV.

11. Adjust 6 kHz Bandpass for maximum and best shape using C58019, C58020, C58024 and C58025. Disconnect external Spectrum Analyzer.

Distortion

12. Select "FM2" on RCVR menu. Set an RF Signal Generator for 0 dBm and a 1 kHz tone with 50 kHz deviation.

13. Connect the Oscilloscope to pin 23 of P57001.

14. Verify audio is about 6 V peak-to-peak. Disconnect Oscilloscope.

15. Connect Distortion Analyzer to pin 23 of P57001 using the Distortion Meter setting.

16. Verify distortion is less than 0.5%. If necessary, adjust L58019 to lower distortion level.

17. Select "FM1" on RCVR menu. Set RF Signal Generator to 5 kHz deviation. Verify less than 3% distortion.

STEP	PROCEDURE

18. Set RF Signal Generator to 10.7 MHz at -10 dBm with 50% AM and select "AM1". Verify less than 1% distortion for both selections.

19. Repeat Step 16 for "AM2".

Sensitivity

20. Reset Distortion Analyzer to SINAD setting. Set RF Signal Generator to 10.7 MHz at -10 dBm with 5 kHz deviation. Select "FM1" on RCVR menu.

21. Verify 10 dB SINAD is typically -71 dBm or less. Disconnect Distortion Analyzer.

SSB Injection

22. Select "SSB" on RCVR menu. Set RF Signal Generator to 10.7 MHz at -70 dBm with no modulation.

23. Connect Oscilloscope to pin 23 of P57001.

24. Adjust R58077 (SSB INJECTION LEVEL) for a 1 V peak-to-peak beat-frequency level.

Squelch

25. Rotate SQUELCH Control (5) on A-7550 and verify audio switches on and off.

Audio Blanking

26. Select "TSR" on RCVR menu and verify audio switches on and off when SCAN WIDTH is ±0 kHz/DIV.

27. Turn off TSR on RCVR menu when finished with test.

4-9 TRACKING GENERATOR CALIBRATION

PREREQUISITE: RF Control Calibration (paragraph 4-5)
Amplitude Calibration (paragraph 4-6)

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Boonton Modulation Meter
1 Spectrum Analyzer
1 Frequency Counter

FIGURE REFERENCES: Figure 4-23 Composite and Adjustments
Figure 5-28 Tracking Generator Installation

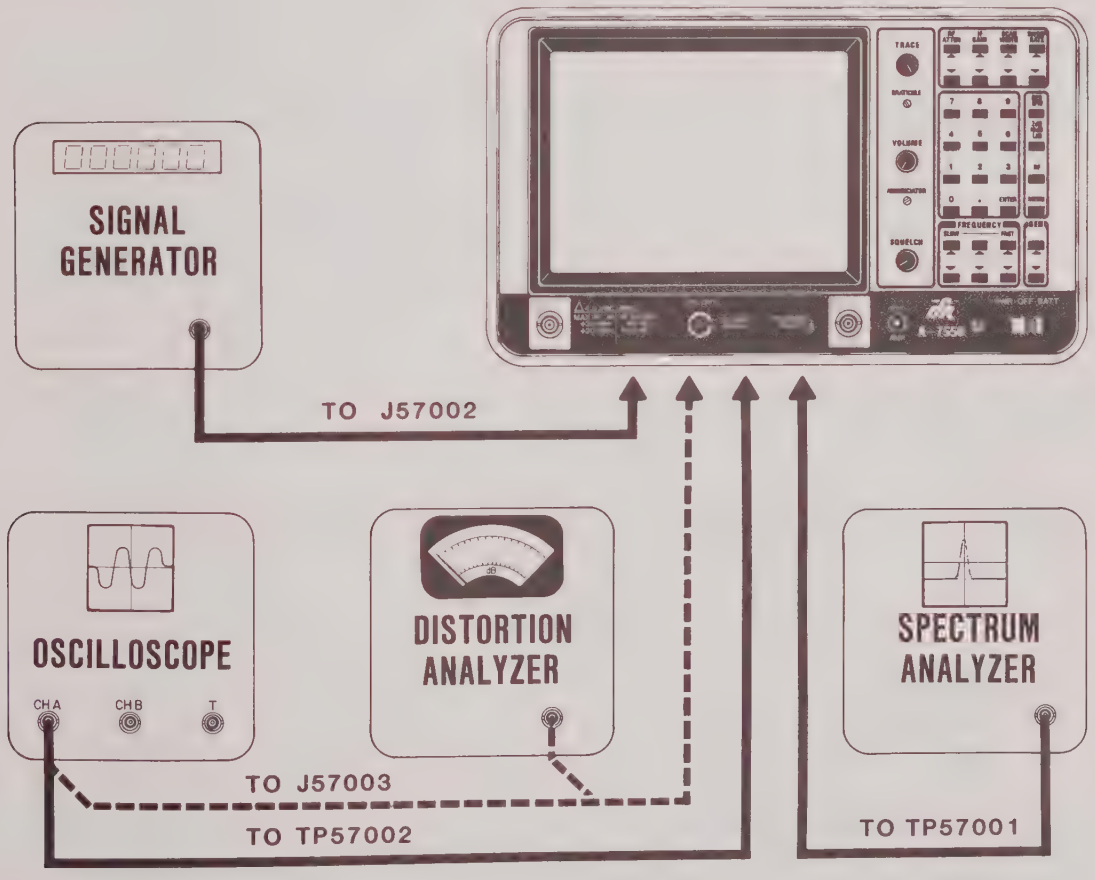


Figure 4-11 Tracking Generator Calibration Test Setup

STEP	PROCEDURE

1. Set the following CRT values:

CONTROL	SETTING
SETUP Menu	6 GEN 1
Center Frequency	1.0000 MHz
SCAN WIDTH	0
GEN	-20 dBm

2. Using a frequency counter, verify the range of TRACKING ADJUST (8) on the front panel is at least -3 kHz and +6 kHz from the selected RF Frequency.

3. When test is complete, return generate frequency to the selected frequency. Disconnect frequency counter.

4. Reset the following CRT values:

CONTROL	SETTING
SETUP Menu	GEN 1, 50Ω, dBm
Center Frequency	500 MHz
SCAN WIDTH	100 MHz/DIV
RES BW	3 MHz
RF ATTEN	30 dB
GEN	-10 dB
2dB/10dB/LIN Scale	2 dB/DIV

5. Connect A-7550 Spectrum Analyzer, GENERATE OUTPUT Connector (7) to A-7550 ANALYZER INPUT Connector (10).

6. Verify generate output level on display is centered on -10 dB graticule. If necessary, adjust R54022 (OUTPUT LEVEL ADJ) in Generate Amp module to desired level.

7. Reset the following CRT values:

CONTROL	SETTING
RF ATTEN	0 dB
GEN	0 dB

8. Verify 0 dB attenuation.

9. Using GEN keys, step output attenuation from 0 to -75 dB.

10. Verify that output level is within 2 dB of each selection. Step output attenuation up to 10 dB (-10 dB Gen Output).

11. Select 75Ω on SETUP menu.

STEP PROCEDURE

12. Verify IF Gain increases 6 dB and generator display level decreases 6 dB.

13. Select 50Ω on the SETUP menu when test is complete.

14. Connect an external Spectrum Analyzer to the GENERATE OUTPUT (7).

15. Verify that for Generate Output signals at a sweep rate of 2 Sec/Div, harmonics are lower than 20 dBc and non-harmonics are lower than 40 dBc.

16. Reset the following CRT values:

CONTROL	SETTING
Center Frequency	100 MHz
SCAN WIDTH	0

17. Connect modulation meter to A-7550 GENERATE OUTPUT Connector (7). Verify frequency deviation (Residual FM) ±100 Hz (RMS PEAK).

+20 dB External Amplifier (Optional)

18. Select "Gen 1" in the SETUP menu. Verify voltage on EXT AMP Connector (6) is +11.7 VDC (±0.2 V).

4-10 QUASI-PEAK FILTER CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF Signal Generator: Hewlett-Packard 8641 or equivalent
1 Frequency Counter: Capable of counting 1 to 1000 Hz with .1 Hz Resolution
1 Pulse Generator: WaveTech 145 or equivalent
1 Impulse Generator: Electrometrics C16-25 or equivalent
1 Spectrum Analyzer: A-7550 or equivalent
1 Solid State Switcher: Watkins-Johnson SI or equivalent
3 Frequency Bandpass Filters: a. 150 kHz low-pass
b. 30 MHz low-pass
c. 30 MHz high-pass

NOTE: Diagrams to construct the frequency band filters are included in Appendix D.

Figure References: Figure 4-23 Composite and Adjustments
Figure 5-9 Quasi-peak Assembly

4-10-1 HEADROOM MEASUREMENT

STEP	PROCEDURE

1. Select the following A-7550 control settings.

CONTROL	SETTING
CENTER FREQUENCY	100 MHz
RF ATTEN	10 dB

2. Select the following RF Signal Generator settings.

CONTROL	SETTING
FREQUENCY	100 MHz
LEVEL	-10 dBm

3. Connect RF Signal Generator to ANALYZER INPUT Connector (10) of A-7550 Spectrum Analyzer under test. Verify -10 dBm at 10.7 MHz Receive IF block.

4. Increase RF level to +4 dBm. Verify output is at least +3 dBm at 10.7 MHz. Record output level in Calibration Record (item 3-2-13a).

STEP PROCEDURE

5. Decrease RF Signal Generator level to -17 dBm. Verify Analyzer IF Level is at least +2 dBm at 10.7 MHz. Record output level in Calibration record (item 3-2-13b).

NOTE: If output of tests in Steps 3 through 5 are less than specified, unit must be recalibrated.

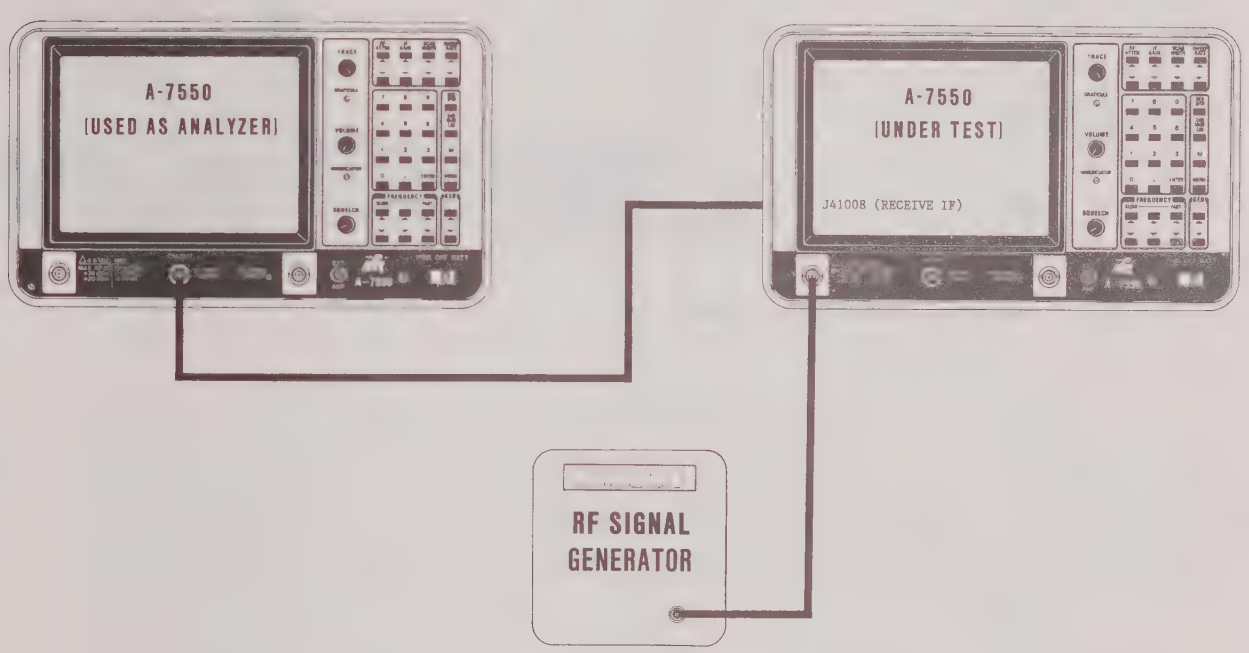


Figure 4-12 Headroom Test Setup

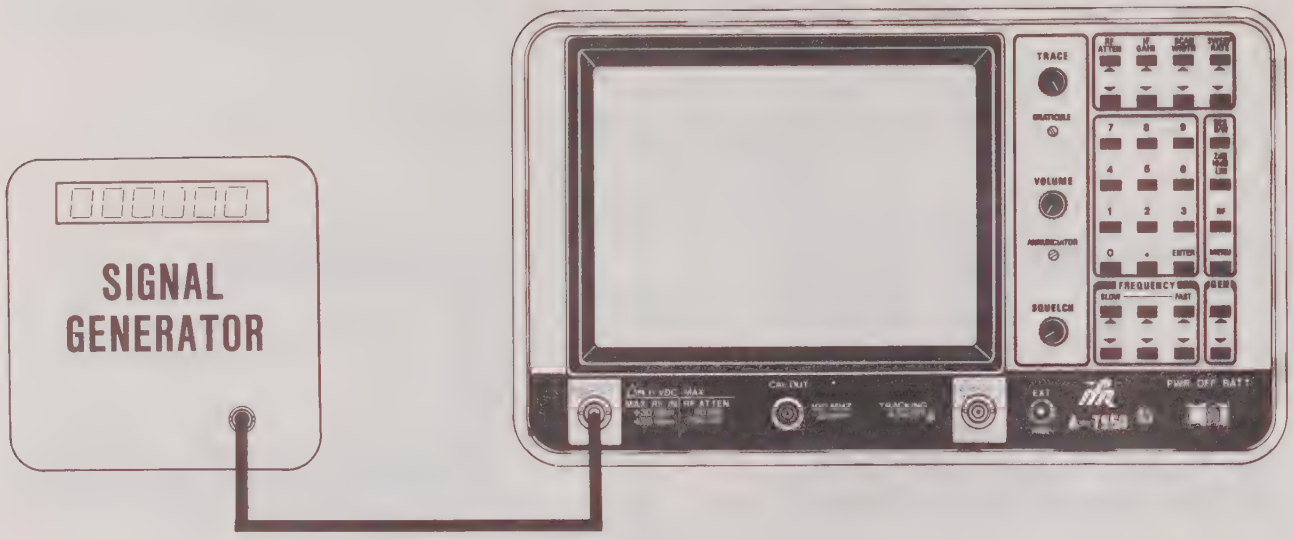


Figure 4-13 Filter Test Setup

STEP PROCEDURE

1. Select the following A-7550 control settings:

CONTROL	SETTING
Center Frequency	100 MHz
RF ATTEN	0 dB
IF GAIN	0 dB
Scan Width	1 kHz/Div
Resolution Bandwidth (RES BW)	300 Hz
Scale	2 dB/DIV

2. The following controls are set via A-7550 menu operation:

MENU	PARAMETER
SETUP (5)	50Ω (1) dBm (2)
SETUP (5) MANUAL (4)	Bw=M (MANUAL) (1) Swp=M (MANUAL) (2) Acal=0 (OFF) (3)

STEP PROCEDURE

3. Select the following RF Signal Generator control settings:

CONTROL	SETTING
FREQUENCY	100.0000 MHz
LEVEL	-30 dBm

4. Connect coax #8 to LOG AMP OUT (J25002) to bypass the Quasi-peak Detector.

5. Connect coax from CAL OUT (9) of external Spectrum Analyzer to ANALYZER INPUT Connector (10) of the A-7550 Spectrum Analyzer. Store the signal (PRESS: MENU 2 5 3).

6. Disconnect the coax from the CAL OUT Connector (9) of the external Spectrum Analyzer and connect the RF Signal Generator to the A-7550 ANALYZER INPUT Connector (10).

7. Compare this signal to the stored signal (PRESS: 2). Adjust frequency of RF Signal Generator to match stored signal.

8. Select 3 MHz Resolution Bandwidth and store this signal.

9. Compare levels of the 300 kHz, 30 kHz, 3 kHz and 300 Hz Resolution Bandwidth settings with the stored signal level. Each level should be within 1 dB of the 3 MHz level; otherwise, recalibrate the Analyzer IF module (see Paragraph 4-7, "Amplitude Calibration", before proceeding).

Adjust TC Levels

10. Select TC3 in Quasi-peak filter menu (PRESS: 0 4 3). Compare the live display level to the stored signal level.

    NOTE: It may be necessary to increase Scan Width to see actual peak of signal. Be sure to return Scan Width to 1 kHz/Div before continuing.

11. Adjust 120 kHz Amplitude trimpot (R63056) as needed to match the levels (±0.2 dB).

12. Select TC2 in Quasi-peak filter menu (PRESS: 2). Compare the live display level to the stored signal level. Adjust 9 kHz AMPLITUDE trimpot (R63036) as needed to match the levels (±0.2 dB).

13. Select TC1 in Quasi-peak filter menu (PRESS: 1) and .1 sec Sweep Rate. Compare the live display level to the stored signal level. Adjust 200 Hz AMPLITUDE trimpot (R63011) as needed to match the levels (±0.2 dB).

14. Record the level on the Calibration Record.

Filter Frequency and Resolution Bandwidth Accuracy

15. Select the following A-7550 Control settings:

CONTROL	SETTING
Scan Width	0 kHz/Div
RF Atten	10 dB
Scale	Linear

16. The following controls are set via A-7550 menu operation:

MENU	PARAMETER
Mode (2)	Live (5)
Filters (4) Quasi (4)	TC1 (1)

17. Adjust frequency from the Signal Generator for peak signal and RF level on RF Signal Generator, as needed, to set signal peak at top of screen display.

18. Slew the frequency left or right to measure bandwidth at 6 dB point (mid-screen). Record the measured Bandwidth (tolerance: 170 to 220 Hz). THE BANDWIDTH SHAPE SHOULD AGREE WITH THE SHAPE SHOWN IN FIGURE 4-14.

NOTE: The 200 Hz filter is a non-adjustable crystal filter which must be replaced if out of tolerance.

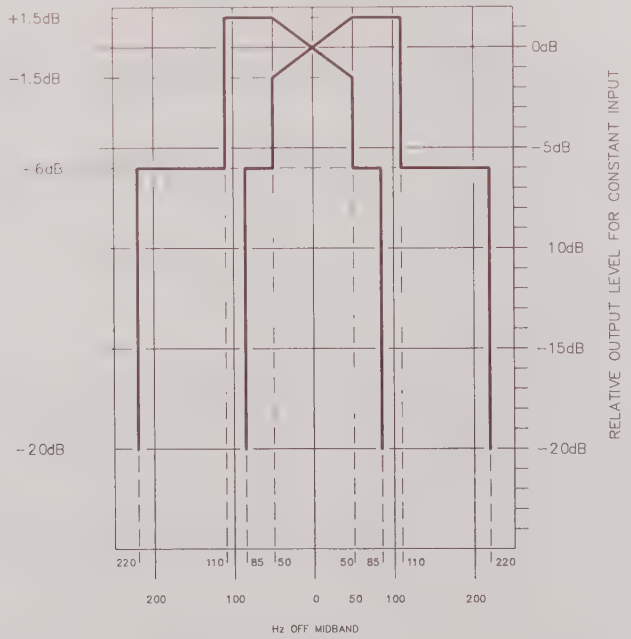


Figure 4-14 200 Hz Bandwidth Filter Shape

19. Select the following A-7550 Control settings:

CONTROL	SETTING
Scan Width	2 kHz/Div
Sweep Rate	50 msec

20. Select TC2 in the Quasi-peak menu (PRESS: MENU 4 4 2).

21. Adjust RF level on RF Signal Generator as needed to set signal peak at top of screen display. Measure and record bandwidth at 6 dB point (mid-screen). Bandwidth should be 9 kHz (±1 kHz).

22. Verify filter shape per Figure 4-15. If shape is within limits, indicate on Calibration Record; otherwise, adjust C63021, C63022, C63025, C63026, C63029 and C63030 aligning for frequency, shape and amplitude. Repeat Steps 17 and 18 to recalibrate the amplitude.

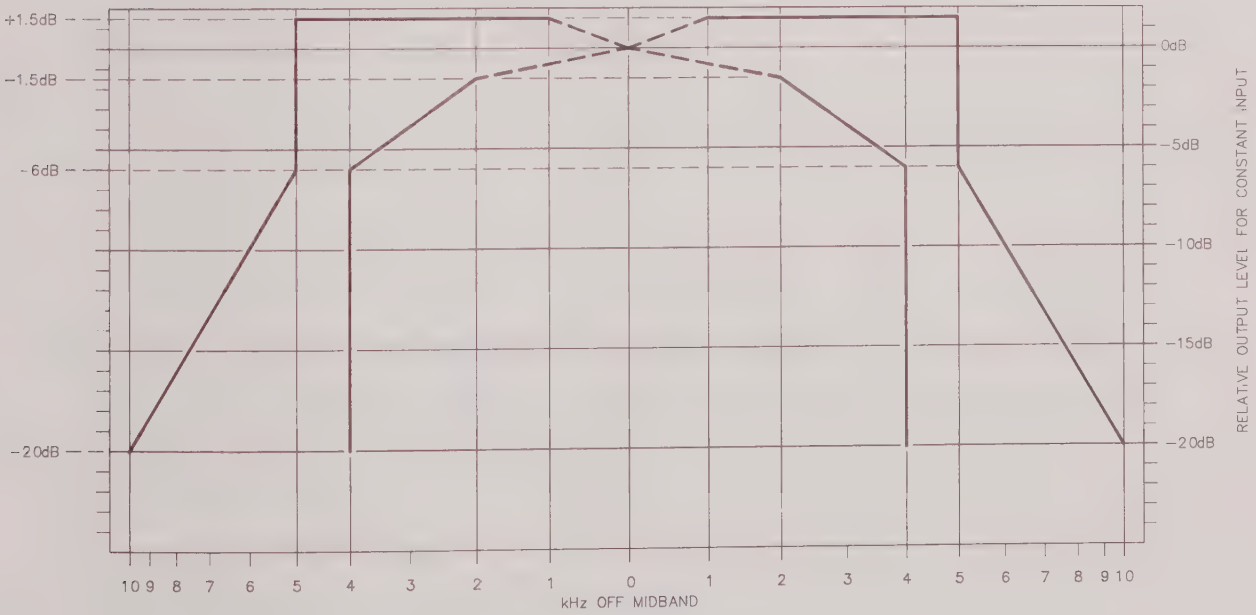


Figure 4-15 9 kHz Filter Limits (9 kHz from Mid-band)

NOTE: 1.5 dB below top of screen is 6.7 major divisions from bottom of screen.

23. Set Scan Width to 10 kHz/Div.

24. Select TC3 in the Quasi-peak menu (PRESS: MENU 4 4 3).

STEP	PROCEDURE

25. Use the FREQUENCY (1) keys to center the signal on the screen. Record difference between center frequency of filter and 100.0000 MHz. The tolerance is ±60 kHz. If out of tolerance, adjust L63011 through L63018 to align frequency.

26. Select Scan Width of 20 kHz/Div.

27. Adjust RF level from RF Signal Generator as needed to set peak signal to top of screen. Measure and record bandwidth 6 dB from top of screen. Bandwidth should be 120 kHz (±20 kHz).

28. Verify filter shape per Figure 4-16. If shape is within limits, indicate on Calibration record. If Steps 27 or 28 are out of tolerance, perform the following:

    a. Adjust L63011 through L63018 to align shape, frequency, and amplitude.

    b. Repeat calibration Steps 21 through 27.

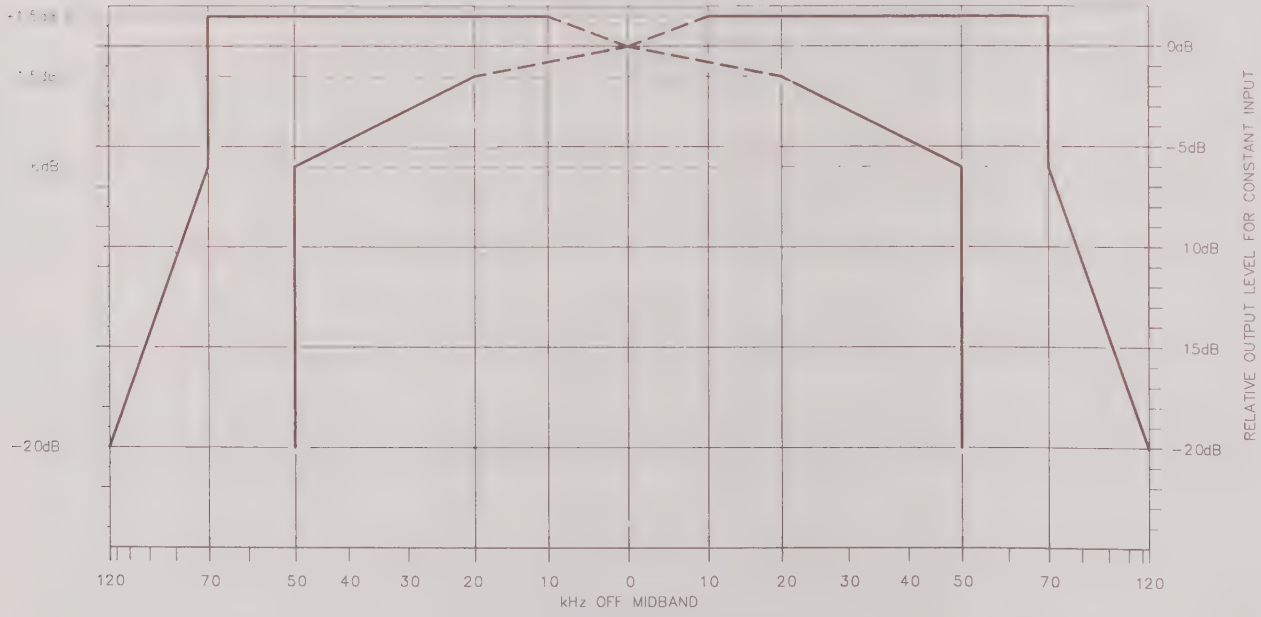


Figure 4-16 120 kHz Filter Limits (120 kHz from Mid-band)

4-10-3 PULSE MEASUREMENTS

The response of the Quasi-peak filters to pulses is the main part of calibration. The set must meet the specifications set forth in Table 4-5 (ref., ANSI C63.2-1980).

NOTE: It is best to continue through entire pulse measurement test before deciding to recalibrate module if any of these tests are out of calibration. All Quasi-peak measurements are taken in LINEAR mode.

FREQ REP RATE (Hz)	QUASI-PEAK FILTER		
	TC1 (dBμV)	TC2 (dBμV)	TC3 (dBμV)
1000	--	64.5 $\pm d_2$ (±1.0)	68.0 $\pm d_3$ (±1.5)
100	64.0 $\pm d_1$ (±1.5)	60.0 $\pm d_2$	60.0 $\pm d_3$
60	63.0 $\pm d_1$ (±1.5)	--	--
25	60.0 $\pm d_1$	--	--
20	--	53.5 $\pm d_2$ (±1.0)	51.0 $\pm d_3$ (±1.5)
10	56.0 $\pm d_1$ (±1.0)	50.0 $\pm d_2$ (±1.5)	46.0 $\pm d_3$ (±2.0)
5	52.5 $\pm d_1$ (±1.5)	--	--
2	47.0 $\pm d_1$ (±2.0)	39.5 $\pm d_2$ (±2.0)	34.0 $\pm d_3$ (±2.0)
1	43.0 $\pm d_1$ (±2.0)	37.5 $\pm d_2$ (±2.0)	31.5 $\pm d_3$ (±2.0)
Isolated Pulse	41.0 $\pm d_1$ (±2.0)	36.5 $\pm d_2$ (±2.0)	28.5 $\pm d_3$ (±2.0)

NOTE: Absolute value of d1, d2 and d3 are less than or equal to 2.0 dBμV.

Table 4-5 Quasi-peak Amplitude Pulse

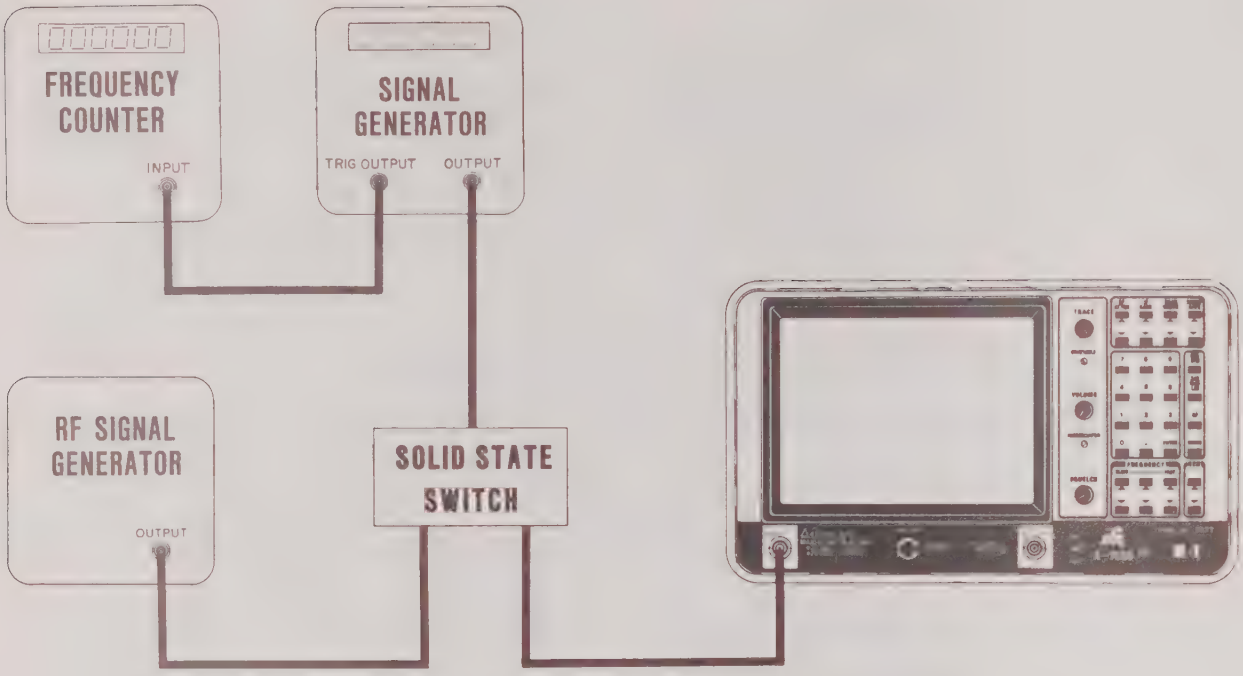


Figure 4-17 Quasi-peak Test Setup

STEP PROCEDURE

1. Select the following A-7550 control settings:

CONTROL	SETTING
Center Frequency	99.9999 MHz
RF ATTEN	30 dB
Scan Width	200 kHz/Div
IF Gain	0 dB
Scale	Linear
Resolution Bandwidth	300 kHz

2. The following controls are set via A-7550 menu operation:

MENU	PARAMETER
Filters (4)	None (1)
Setup (5)	50Ω (1)
	dBμV (2)
Setup (5) Manual (4)	Acal=0 (OFF) (3)

3. Set RF Signal Generator level to -10 dBm.

4. Select the following Pulse Generator settings:

CONTROL	SETTING
Amplitude	4 V p-p
Frequency Repetition Rate	1000 Hz
Pulse Width	1 µsec (approximate)
DC offset	full CW
Generator Mode	Continuous

5. Connect coax #8 to the Quasi-peak Detector (J62005). Connect coax #41 to the LOG AMP module (J25002).

TC3 Pulse Response Test

6. Vary DC offset on Pulse Generator to peak CW signal. Measure and record peak signal level.

EXAMPLE 4-1: T = Top of Screen level at 100 dBµV.
D = Number of major divisions from bottom of screen resolved to .25 minor divisions (i.e., IF signal peak one minor division above third major division, D = 3.25).
A = Signal Amplitude.

EQUATION 4-1: A = T + 20 * LOG(D/8)

IF T = 100 dBµV
D = 3.1 major divisions:
A = 100 + 20 * LOG(3.1/8)
A = 91.8 dBµV

7. Calculate first zero crossing for TC3 (δF_3):

EQUATION 4-2: δf_3 = {10 ** ((A+3)/20)/.044}

EXAMPLE 4-2: A (from Example 4-1) = 91.9 dBµV
δf_3 = {10 ** ((91.8 + 3)/20)/.044}
= 1.249 MHz

8. Select the following A-7550 Control settings:

CONTROL	SETTING
RF ATTEN	10 dB
IF GAIN	10 dB

9. Vary DC offset on Pulse Generator until pulse spectrum appears on A-7550 display (see Figure 4-18).

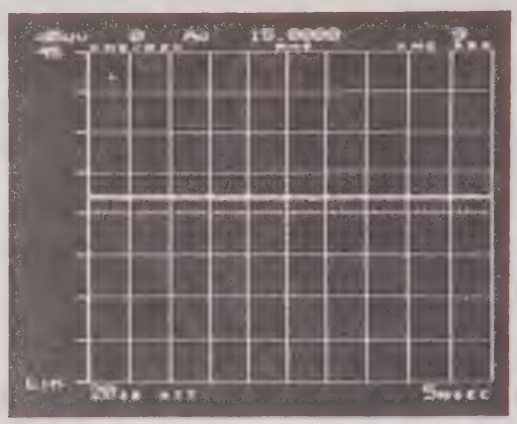


Figure 4-18 Pulse Spectrum

10. Adjust DC OFFSET to minimize carrier feed-through without changin spectrum amplitude (i.e., no carrier feed-through is visible on display).

11. Select A-7550 Center Frequency of 99.9999 MHz + δf_3.

    EXAMPLE 4-3: CF = 99.9999 + (from Step 7) 1.249
    = 101.2489 MHz

12. Adjust Pulse Width on Pulse Generator to put first zero crossing at center of screen (see Figure 4-19).

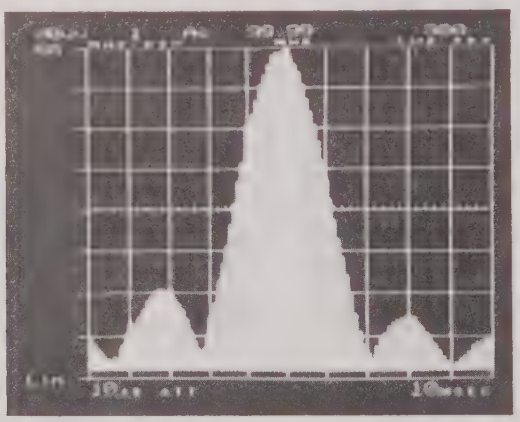


Figure 4-19 δf_3 Zero Crossing

13. Reset the A-7550 Center Frequency to 99.9999 MHz.

STEP	PROCEDURE

14. Adjust IF Gain as high as possible without setting the pulse spectrum above the top of screen display. Record this level in the Calibration Record.

15. Set A-7550 Scan Width to 0 kHz/Div.

16. Set Quasi-peak filter menu to TC3 (PRESS: MENU 4 4 3).

17. Set Frequency Repetition Rate of Pulse Generator to 100 Hz (±1.0 Hz).

    NOTE: To increase resolution, up to 10 dB IF GAIN may be introduced using TC3. However, increasing the IF Gain more than 10 dB can cause compression of the pulse spectrum.

18. Calculate the trace level difference (d_3) using Table 4-5 at 60 dBµV and record in the Calibration Record.

19. Adjust A-7550 IF Gain to show top of screen at 66 dBµV.

20. Adjust RF Signal level to set trace at mid-screen (60 dBµV). This adds d_3 to the pulse, allowing d_3 to be ignored for the remainder of TC3 pulse response testing.

21. Select 1000 Hz (±10 Hz) Pulse Generator Frequency.

    NOTE: The IF Gain may be changed to keep the trace on the screen display. To avoid compression, do not increase the IF Gain more than 10 dB from the level recorded in Step 14.

22. Calculate the level per Table 4-5 and record in the Calibration Record.

23. Select 20 Hz (±0.2 Hz) Pulse Generator Frequency.

24. Calculate the level per Table 4-5 and record in the Calibration Record.

25. Select 10 Hz (±0.1 Hz) Pulse Generator Frequency.

26. Set the A-7550 MODE Menu to "PkHold" (PRESS: 0 0 2 6).

27. Calculate the level per Table 4-5 and record in the Calibration Record.

28. Select 2 Hz (0.1 Hz) Pulse Generator Frequency. Reset the A-7550 MODE Menu to "Live" and return to "PkHold" (PRESS: 5 6).

29. Calculate the level per Table 4-5 and record in the Calibration Record.

30. Select 1 Hz (±0.1 Hz) on the Pulse Generator Frequency. Reset the A-7550 MODE Menu to "Live" and return to "PkHold" (PRESS: 5 6).

31. Calculate the level per Table 4-5 and record in the Calibration Record.

32. Reset MODE on the Pulse Generator to GEN. Reset the A-7550 MODE Menu to "Live" and return to "PkHold" (PRESS: 5 6).

33. Manually trigger the Pulse Generator. Calculate the level per Table 4-5 and record in the Calibration Record.

    NOTE: Do not use manual trigger function faster than three second intervals, to allow filters to discharge to ground level.

TC2 Pulse Response Test

34. Select the following A-7550 control settings, as needed:

CONTROL	SETTING
Center Frequency	99.9999 MHz
Scan Width	20 kHz/Div
RF Atten	30 dB
Scale	Linear
Resolution Bandwidth	30 kHz

35. The following controls are set via A-7550 menu operation, as needed:

MENU	PARAMETER
MODE (2)	Live (5)
FILTERS (4)	None (1)
SETUP (5)	dBµV (1)
SETUP (5) MANUAL (4)	Bw=M (1)
	Acal=0 (OFF) (3)

36. Set the Level on RF Signal Generator to -10 dBm.

37. Select the following settings on the Pulse Generator:

CONTROL	SETTING
Frequency	1000 Hz
Pulse Width	5 µsec (approximate)
DC Offset	Full CW
Gen Mode	Continuous

STEP PROCEDURE

38. Vary DC Offset on Pulse Generator to peak the CW signal. Measure and record peak signal level (A) in the Calibration Record (see Step 6).

39. Calculate first zero crossing point for TC2 (δf_2):

EQUATION 4-3: $\delta f_2 = \{10 ** ((A+3)/20)/.316\}$

EXAMPLE 4-4:
$A = 90.88\ dB\mu V$
$\delta f_2 = \{((90.88+3)/20)/.316\}$
$= 0.1565\ MHz$

40. Select the following A-7550 control settings:

CONTROL	SETTING
RF Atten	10 dB
IF Gain	0 dB

41. Vary DC OFFSET on Pulse Generator until pulse spectrum appears on display. Adjust DC OFFSET to minimize carrier feed-through without decreasing pulse spectrum amplitude (see Figure 4-17).

42. Select Center Frequency of 99.9999 MHz + δf_2.

EXAMPLE 4-5: CF = 99.9999 MHz + (from Step 39) 0.1565
= 100.1564 MHz

43. Adjust pulse width to put first zero crossing at center of screen (see Figure 4-20).

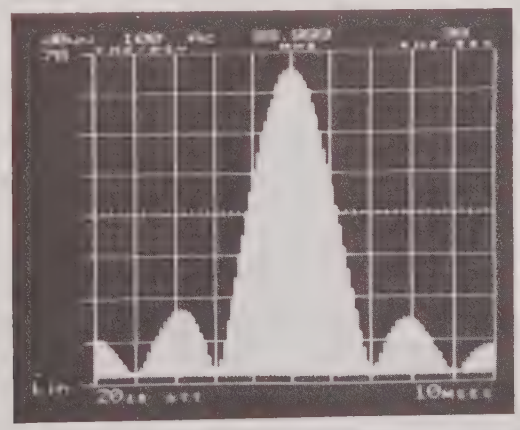


Figure 5-20 δf_2 Zero Crossing

STEP	PROCEDURE

44. Reset A-7550 Center Frequency to 99.9999 MHz. Adjust IF GAIN as high as possible without setting pulse display above top of screen. Record the top of screen level in the Calibration Record.

45. Select 0 kHz/Div Scan Width.

46. Select TC2 in the Quasi-peak filter menu (PRESS: MENU 4 4 2).

47. Select Frequency Repetition Rate (FRP) of 100 Hz (±1.0 Hz) on the Pulse Generator.

    NOTE: Up to 20 dB of IF GAIN may be used to increase the display resolution in TC2. However, introducing more than 20 dB of IF Gain can cause compression in the pulse spectrum.

48. Calculate the trace level (d_2) per Table 4-5 and record in the Calibration Record.

49. Adjust IF Gain to set the top of screen to 66 dBµV.

50. Adjust the Amplitude from the Pulse Generator to position the signal at mid-screen (60 dBµV).

51. Select Frequency Repetition Rate of 1000 Hz (±10.0 Hz) on Pulse Generator.

    NOTE: It may be necessary to adjust the IF GAIN to keep trace on screen. However, introducing more than 20 dB of IF Gain can cause compression in the pulse spectrum.

52. Calculate the trace level per Table 4-5 and record in the Calibration Record.

53. Reset the Frequency Repetition Rate to 20 Hz (±0.2 Hz) on the Pulse Generator.

54. Calculate the trace level per Table 4-5 and record in the Calibration Record.

55. Reset the Frequency Repetition Rate to 10 Hz (±0.1 Hz) on the Pulse Generator.

56. Calculate the trace level per Table 4-5 and record in the Calibration Record.

57. Reset the Frequency Repetition Rate to 2 Hz (±0.1 Hz) on the Pulse Generator. Select "PkHold" in the MODE menu (PRESS: MENU 2 6).

58. Calculate the trace level per Table 4-5 and record in the Calibration Record.

STEP PROCEDURE

59. Reset Frequency Repetition Rate to 1 Hz (±0.1 Hz) on the Pulse Generator. Reset the Mode to "Live" and return to "PkHold" in the MODE menu (PRESS: 5 6).

60. Calculate the trace level per Table 4-5 and record in the Calibration Record.

61. Reset MODE on the Pulse Generator to GEN. Reset Mode to "Live" and return to "PkHold" in the MODE menu (PRESS: 5 6).

62. Manually trigger the Pulse Generator. Calculate the trace level per Table 4-5 and record in the Calibration Record.

NOTE: Do not use manual trigger function faster than three second intervals, to allow filters to discharge to ground level.

TC1 Pulse Response Test

63. Select the following A-7550 control settings, as needed:

CONTROL	SETTING
Center Frequency	99.9999 MHz
Scan Width	1 kHz/Div
RF Atten	30 dB
Scale	Linear
Resolution Bandwidth	3 kHz
Sweep Rate	.2 sec/Div

64. The following controls are set via A-7550 menu operation, as needed:

MENU	PARAMETER
MODE (2)	Live (5)
FILTERS (4)	None (1)
SETUP (5)	dBµV (1)
SETUP (5) MANUAL (4)	Bw=M (1)
	Swp=M (1)
	Acal=0 (OFF) (3)

65. Set the RF Signal Generator Level to -10 dBm.

66. Select the following Pulse Generator settings:

CONTROL	SETTING
Frequency	25 Hz (±0.2 Hz)
Pulse Width	200 µsec
DC Offset	Full CW
Gen Mode	Continuous

67. Vary DC Offset on Pulse Generator to peak the CW signal. Measure and record peak signal level in the Calibration Record (see Step 6).

68. Calculate first zero crossing point for TC1 (δF_1):

EQUATION 4-4: $\delta F_1 = \{10 ** ((A+3)/20)/13.5\ \mu VSEC\}$.

EXAMPLE 4-6: A = 92.82 dBµV
$\delta F_1 = \{((92.82+3)/20)/13.5\}$.

69. Select the following A-7550 control settings:

CONTROL	SETTING
RF Atten	10 dB
IF Gain	5 dB

NOTE: Top of screen should be 75 dBµV.

70. Vary DC OFFSET on Pulse Generator until pulse spectrum appears on display. Adjust DC OFFSET to minimize carrier feed-through without decreasing pulse spectrum amplitude (see Figure 4-15).

NOTE: Top of spectrum should not be flat and bleed-through should disappear from screen.

71. Select Center Frequency of 99.9999 MHz + δF_1.

EXAMPLE 4-7: CF = 99.9999 MHz = (from Step 67) 0.0046
= 100.0046 MHz

72. Adjust pulse width to put first zero crossing at center of screen (see Figure 4-21).

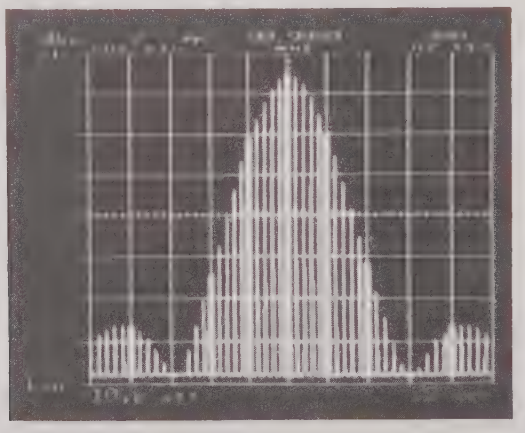


Figure 4-21 δf_1 Zero Crossing

STEP	PROCEDURE

73. Reset A-7550 Center Frequency to 99.9999 MHz. Adjust IF GAIN as high as possible without setting pulse display above top of screen. Record the top of screen level in the Calibration Record.

74. Select 0 kHz/Div Scan Width and 5 msec/Div Sweep Rate.

75. Select TC1 in the Quasi-peak Filter menu (PRESS: MENU 4 4 1).

76. Select Frequency Repetition Rate of 25 Hz (±0.25 Hz) on the Pulse Generator.

    NOTE: Up to 15 dB of IF GAIN may be used to increase the display resolution in TC1. However, introducing more than 15 dB of IF Gain can cause compression in the pulse spectrum.

77. Calculate the trace level (d_1), per Table 4-5 and record in the Calibration Record.

78. Adjust IF Gain to set the top of screen to 66 dBµV.

79. Adjust the Amplitude from the Pulse Generator to position the signal at mid-screen (60 dBµV).

80. Select Frequency Repetition Rate of 60 Hz (±0.6 Hz) on the Pulse Generator.

    NOTE: It may be necessary to adjust the IF GAIN to keep trace on screen. However, introducing more than 15 dB of IF GAIN can cause compression in the pulse spectrum.

81. Calculate the trace level per Table 4-5 and record in the Calibration Record.

82. Reset the Frequency Repetition Rate to 100 Hz (±1.0 Hz) on the Pulse Generator.

83. Calculate the trace level per Table 4-5 and record in the Calibration Record.

84. Reset the Frequency Repetition Rate to 10 Hz (±0.1 Hz) on the Pulse Generator.

85. Calculate the trace level per Table 4-5 and record in the Calibration Record.

86. Reset the Frequency Repetition Rate to 5 Hz (±0.1 Hz) on the Pulse Generator.

87. Calculate the trace level per Table 4-5 and record in the Calibration Record.

STEP PROCEDURE

88. Reset the Frequency Repetition Rate to 2 Hz (±0.1 Hz) on the Pulse Generator. Select "PkHold" in the MODE menu (PRESS: MENU 2 6).

89. Calculate the trace level per Table 4-5 and record in the Calibration Record.

90. Reset the Frequency Repetition Rate to 1 Hz (±0.1 Hz) on the Pulse Generator. Reset Mode to "Live" and return to "PkHold" in the MODE menu (PRESS: 5 6).

91. Calculate the trace level per Table 4-5 and record in the Calibration Record.

92. Reset the MODE on Pulse Generator to GEN. Reset A-7550 Mode to "Live" and return to "PkHold" in the MODE menu (PRESS: 5 6).

93. Manually trigger the Pulse Generator. Calculate the trace level per Table 4-5 and record in the Calibration Record.

NOTE: Do not use manual trigger function faster than three second intervals, to allow filters to discharge to ground level.

94. IF ANY PART OF THE PULSE MEASUREMENT TESTS FAILED SPECIFICATIONS, REPEAT PARAGRAPHS 3-2-13 AND 4-10-2.

4-10-4 FILTER TESTS

CAUTION: IT IS EXTREMELY EASY TO OVERLOAD THE FIRST MIXER IN THE A-7550 WITH IMPULSE SIGNALS. DO NOT CONNECT A-7550 TO IMPULSE GENERATOR UNTIL SETUP IS COMPLETE FOR EACH FILTER RANGE. PERFORM FILTER TESTS BEFORE PROCEEDING.

STEP PROCEDURE

1. Select the following A-7550 controls:

CONTROL	SETTING
Center Frequency	225.0000 MHz
IF Gain	0 dB
RF Atten	30 dB
Scan Width	5 kHz/Div
Scale	2 dB/Div

2. The following controls are set via A-7550 menu operation:

MENU	PARAMETER
SETUP (5) MANUAL (4)	Bw=A (1)
	Swp=A (2)
	Acal=0 [OFF] (3)

STEP PROCEDURE

3. Select the following RF Signal Generator controls:

CONTROL	SETTING
FREQUENCY	225.0 MHz
AMPLITUDE	-10 dBm

4. Verify -10 dBm level on Power Meter.

5. Connect 30 MHz high-pass filter between RF Signal generator and ANALYZER INPUT Connector (10) of A-7550 Spectrum Analyzer.

6. Record the following levels and calculate TC3 OFFSET:

Filter level: _____
+ 10 dB: 10
+ d_3 : _____ (Difference between 40 dBµV and filter level)
TC3 OFFSET _____

7. Disconnect 30 MHz high-pass filter.

8. Select 15.0000 MHz Center Frequency on the A-7550 Spectrum Analyzer and the RF Signal Generator.

9. Connect 30 MHz low-pass filter between RF Signal Generator and Analyzer Input Connector (10).

10. Record the following levels and calculate TC2 OFFSET:

Filter level: _____
+ 10 dB: 10
+ d_2 : _____ (Difference between 40 dBµV and filter level)
TC2 OFFSET _____

11. Disconnect 30 MHz low-pass filter from ANALYZER INPUT Connector (10).

12. Select 0.1000 Center Frequency on the A-7550 Spectrum Analyzer and the RF Signal Generator.

13. Connect 150 kHz low-pass filter in series with the 30 MHz low-pass filter between the RF Signal Generator and the A-7550 Analyzer Input Connector (10).

STEP	PROCEDURE

14. Record the following levels and calculate TC1 OFFSET:

    Filter level: _____
    + 10 dB: 10
    + d_1 : _____ (Difference between 10 dBµV and filter level)
    TC1 OFFSET _____

15. Disconnect low pass filters and RF Signal Generator from A-7550 Analyzer Input-Connector (10).

4-10-5 IMPULSE TEST

Refer to Figure 4-22 for hookup of Impulse Test equipment.

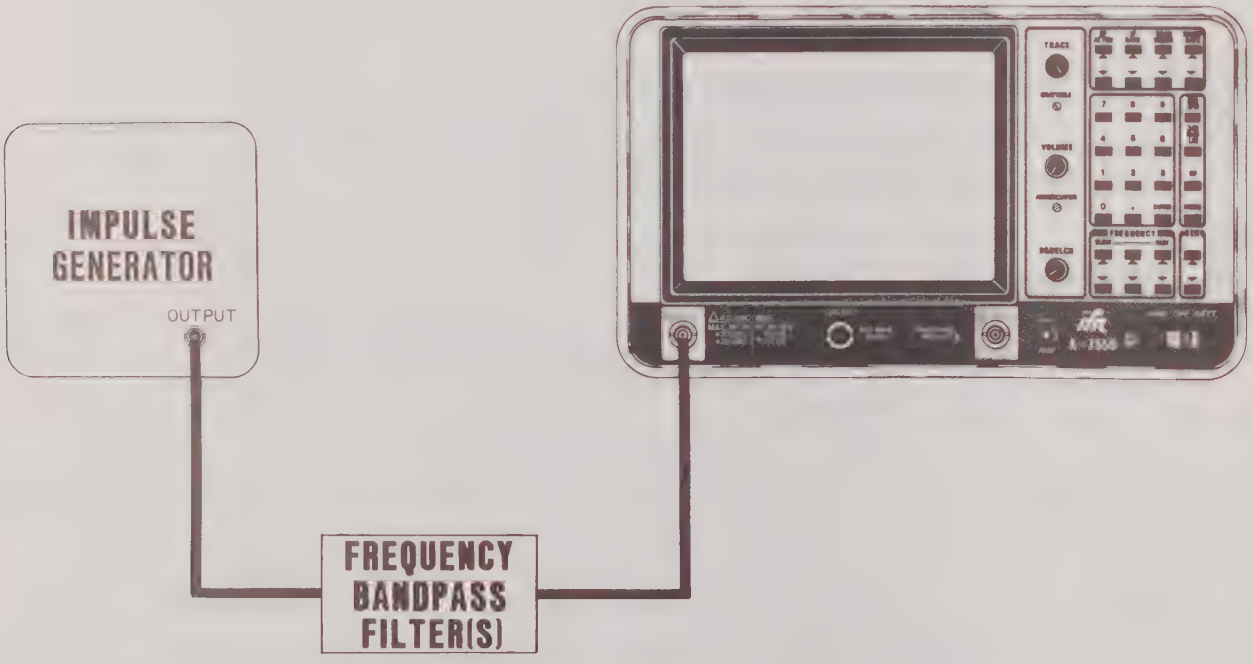


Figure 4-22 Impulse Test Setup

TC3 Impulse Measurement

1. Select the following A-7550 control settings:

CONTROL	SETTING
Center Frequency	225.0 MHz
RF ATTEN	20 dB
Scan Width	0 kHz/Div
Scale	Linear
IF Gain	45 dB (see NOTE)

NOTE: IF Gain should be set to display 45 dBµV at top of screen.

2. The following controls are set via A-7550 menu operation:

MENU	PARAMETER
SETUP (5) MANUAL (4)	Bw=A (1) Swp=A (2)
FILTERS (4) QUASI (4)	Acal=0 (OFF) (3) TC3

3. Select the following Impulse Generator control settings:

CONTROL	SETTING
Output Level	70 dBµV/MHz
Repetition Rate	100 Hz

CAUTION: BE SURE PULSES ARE TURNED OFF FROM THE IMPULSE GENERATOR BEFORE CONNECTING TO A-7550 SPECTRUM ANALYZER.

4. Connect the Impulse Generator using the inline 30 MHz high-pass filter to the ANALYZER INPUT Connector (10) of the A-7550 Spectrum Analyzer.

5. Calculate TC3 OFFSET, trace level for the 100 Hz impulse rate:

   Equation 4-5: LEVEL @ 100 Hz = 40 dBµV + TC3 OFFSET (±2.0 dBµV)

   Record the actual (measured) level for TC3 Offset in the Calibration Record.

6. Subtract 7.0 dB from the measured level recorded in Step 5.

7. Select 20 Hz Repetition Rate on the Impulse Generator. The level should be ±1.5 dB of the level calculated in Step 6. Record the measured level in the Calibration Record.

   NOTE: Up to 5 dB IF Gain may be selected at this time, as needed. However, do not exceed 40 dBµV top of screen indication.

8. Disconnect coax from A-7550 Analyzer Input Connector (10).

TC2 Impulse Measurement

9. Select the following A-7550 control settings:

CONTROL	SETTING
Center Frequency	15.0 MHz
RF ATTEN	20 dB
Scan Width	0 kHz/Div
IF Gain	45 dB (see NOTE)

NOTE: IF Gain should be set to display 45 dBµV at top of screen.

10. Set the Quasi-peak Filter menu to TC2 (PRESS: MENU 4 4 2).

11. Select the following Impulse Generator control settings:

CONTROL	SETTING
Output Level	87 dBµV/MHz
Repetition Rate	100 Hz

CAUTION: BE SURE PULSES ARE TURNED OFF FROM THE IMPULSE GENERATOR BEFORE CONNECTING TO A-7550 SPECTRUM ANALYZER.

12. Connect the Impulse Generator using the inline 30 MHz Low-pass filter to the ANALYZER INPUT Connector (10) of the A-7550 Spectrum Analyzer.

13. Calculate TC2 OFFSET, trace level for the 100 Hz impulse rate:

Equation 4-6: LEVEL @ 100 Hz = 40 dBµV + TC2 OFFSET (±2.0 dBµV)

Record the actual (measured) level of TC2 Offset in the Calibration Record.

14. Subtract 6.5 dB from measured level recorded in Step 13.

NOTE: Up to 8 dB IF Gain may be selected at this time, as needed. However, do not exceed 40 dBµV top of screen indication.

15. Select 20 Hz Repetition Rate on the Impulse Generator. The level should be ±1.5 dB of the level calculated in Step 14. Record this level in Calibration Record.

16. Disconnect coax from A-7550 Analyzer Input Connector (10).

STEP PROCEDURE

TC1 Impulse Measurement

17. Select the following A-7550 control settings:

CONTROL	SETTING
Center Frequency	0.1000 MHz
RF ATTEN	0 dB
Scan Width	0 kHz/Div
IF Gain	55 dB (see NOTE)

NOTE: IF Gain should be set to display 15 dBµV at top of screen.

18. Set the Quasi-peak Filter menu to TC1 (PRESS: MENU 4 4 1).

19. Select the following Impulse Generator control settings:

CONTROL	SETTING
Output Level	90 dBµV/MHz
Repetition Rate	20 Hz

CAUTION: BE SURE PULSES ARE TURNED OFF FROM THE IMPULSE GENERATOR BEFORE CONNECTING TO A-7550 SPECTRUM ANALYZER.

20. Connect the Impulse Generator using the inline 30 MHz and 150 kHz low-pass filters, in series, to the ANALYZER INPUT Connector (10) of the A-7550 Spectrum Analyzer.

21. Calculate TC1 OFFSET, trace level for the 20 Hz impulse rate:

Equation 4-7: LEVEL @ 20 Hz = 10 dBµV - TC1 OFFSET (±2.0 dBµV)

Record the actual (measured) level of TC1 Offset in the Calibration Record.

22. Subtract 4.0 dB from the measured level in Step 21.

23. Select 10 Hz Repetition Rate on the Impulse Generator. The trace level should be ±1 of the calculated level in Step 22. Record this level in the Calibration Record.

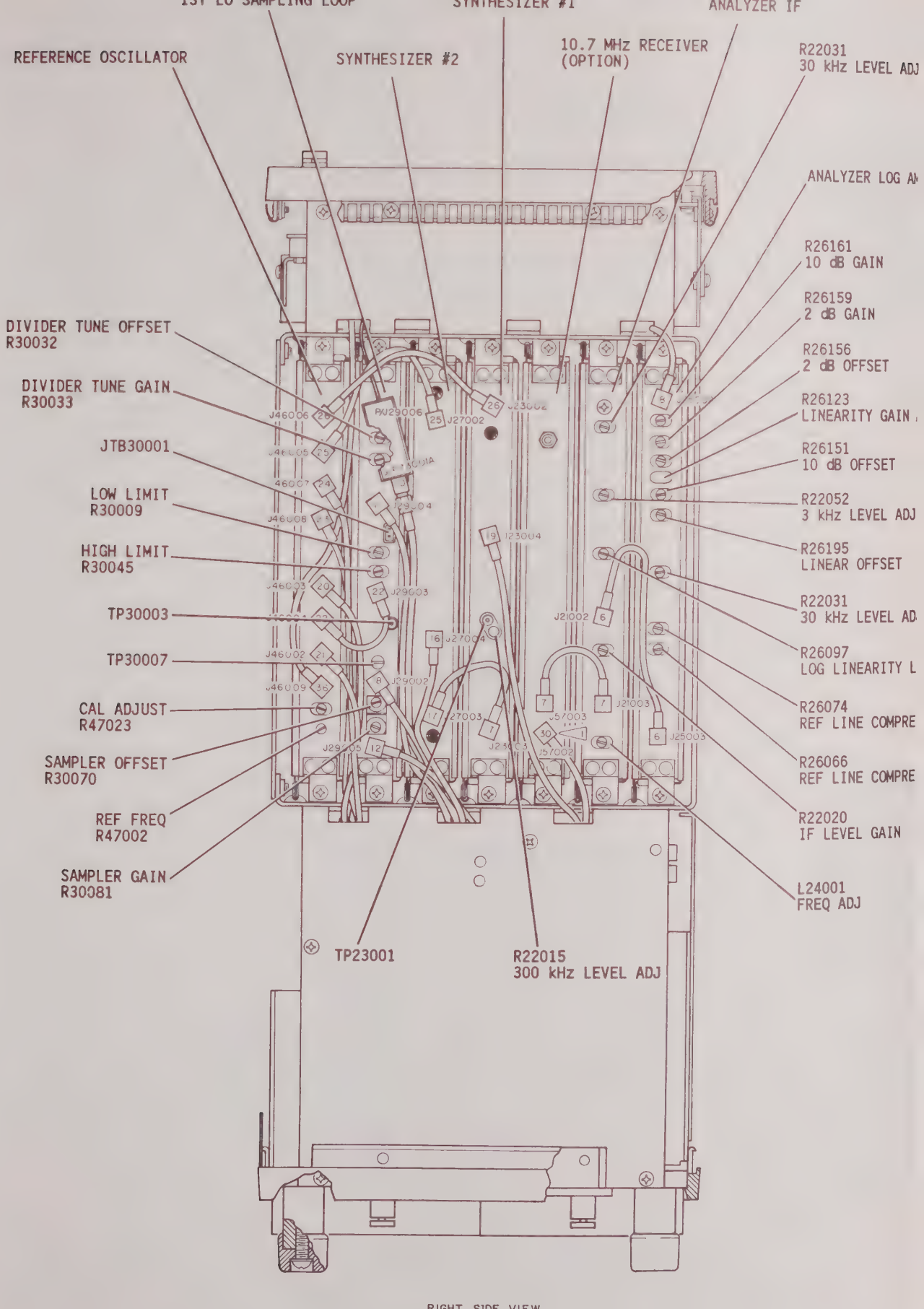
NOTE: Up to 6 dB IF Gain may be selected at this time, as needed. However, do not exceed 9 dBµV top of screen indication.

24. Add 3.0 dB to the measured level in Step 21.

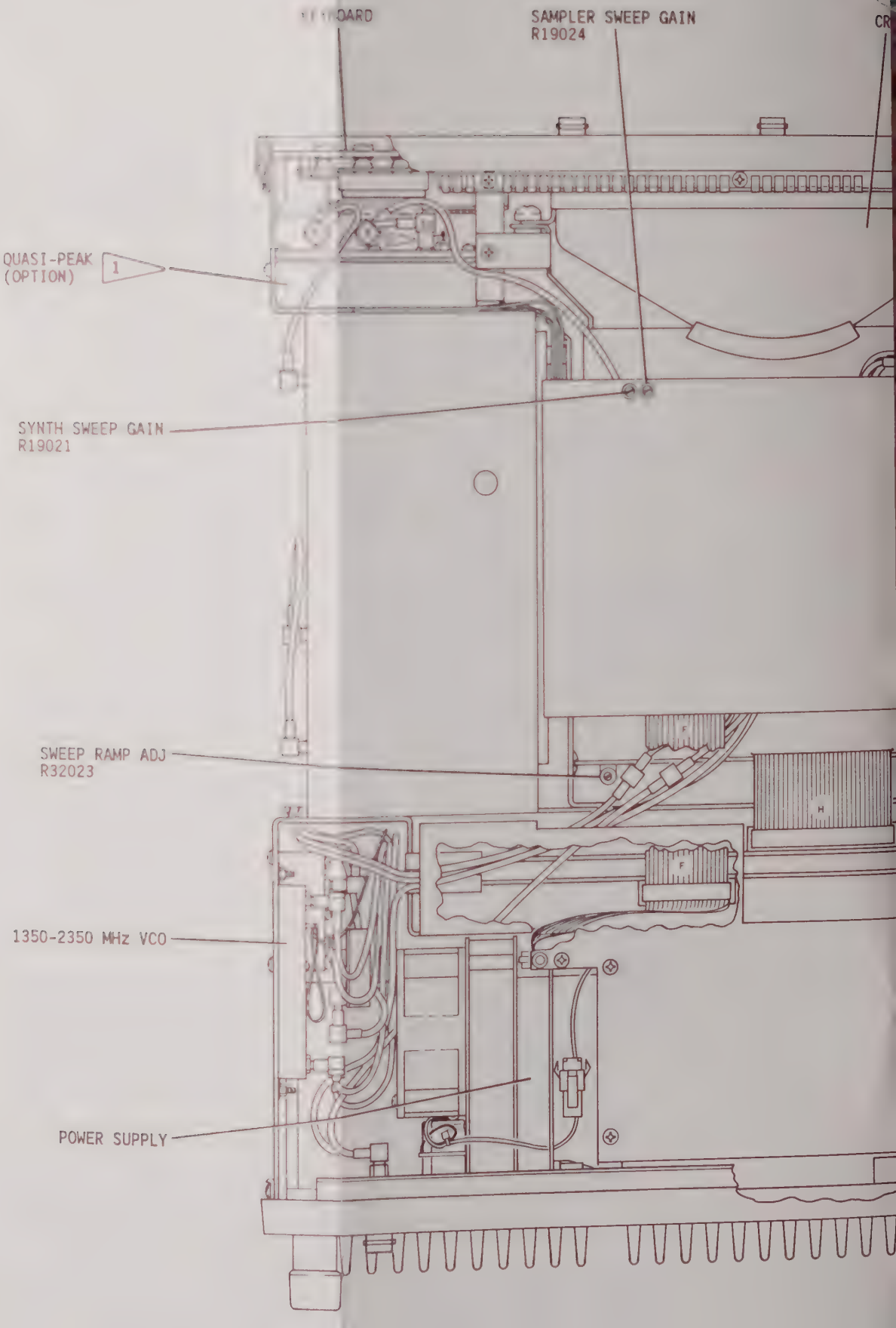
25. Select 60 Hz Repetition Rate on the Impulse Generator. The trace level should be ±1 of the calculated level in Step 24. Record this level in the Calibration Record.

26. Disconnect all equipment.

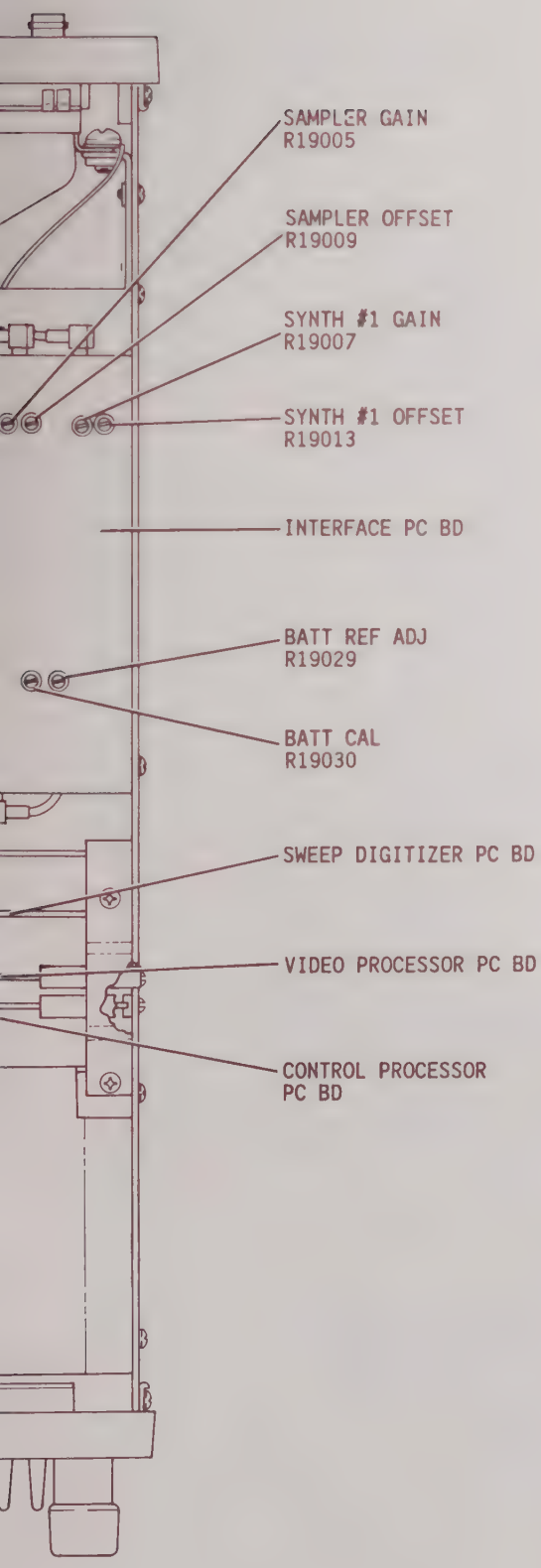
END OF TEST



RIGHT SIDE VIEW


SAMPLER SWEEP GAIN
R19024
QUASI-PEAK
(OPTION)
1
SYNTH SWEEP GAIN
R19021
SWEEP RAMP ADJ
R32023
1350-2350 MHz VCO
POWER SUPPLY

TOP VIEW



NOTE:

1. COAX NUMBERS TO/FROM QUASI-PEAK/10.7 MHz RECEIVER MODULES VARY DEPENDING ON INSTALLED OPTIONS. REFER TO COAX RUNNING LIST/INTERCONNECT DRAWINGS IN SECTION 5.

Figure 4-23 Composite and Adjustments (Sheet 1 of 2)

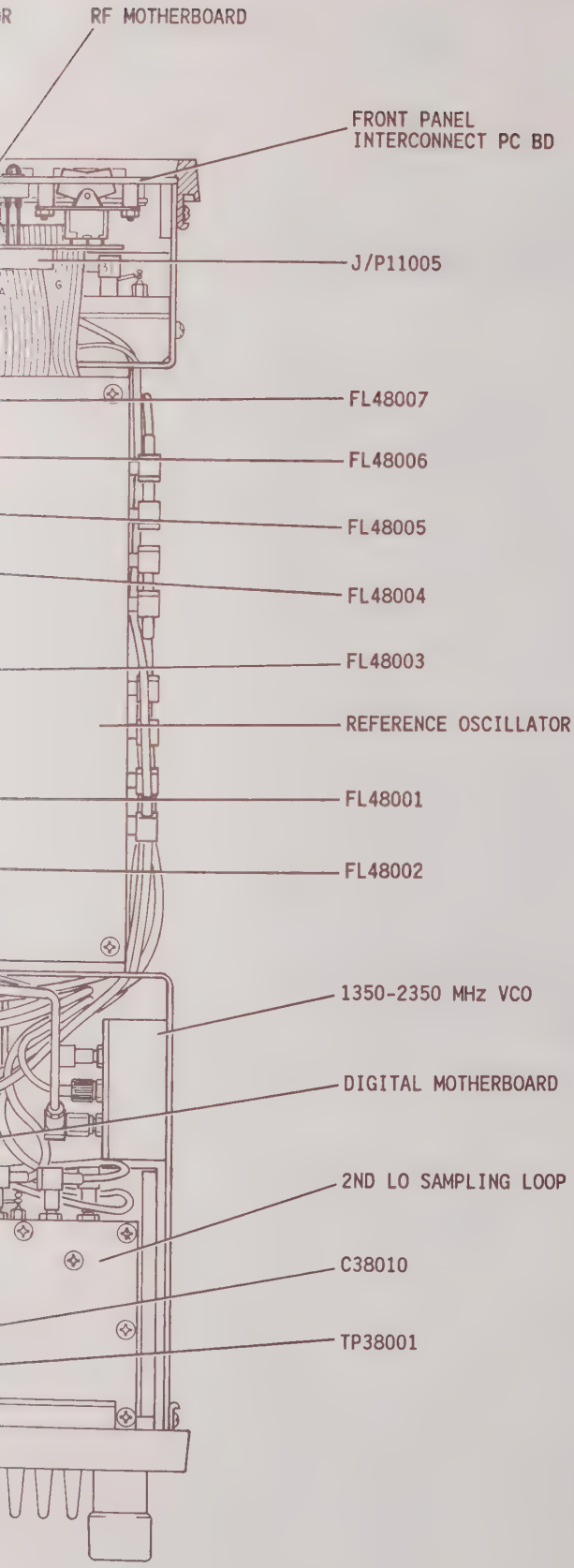


Figure 4-23 Composite and Adjustments (Sheet 2 of 2)

SECTION 5 - ASSEMBLIES, PC BOARDS & SCHEMATICS

5-1 GENERAL

This section contains the mechanical drawings, PC board layouts, Schematic diagrams, and other supportive illustrations to assist the Technician in maintaining the A-7550 Spectrum Analyzer. The drawings are in relative sequence of the corresponding module description in the Theory of Operations (Section 2). Due to space requirements, however, several of these drawings may not appear exactly as described in the Theory. Also, only units with Serial Numbers 2400 and On are covered in this text. An index of drawings is contained in Paragraph 5-3.

5-2 HOW TO USE SCHEMATICS

To trace coaxial cable conductors from one schematic to another, follow the procedures outlined in Paragraph 5-2-1. To trace conductors for multiple pin connectors, see Paragraph 5-2-2.

5-2-1 COAXIAL CABLES

A. Locate desired module on the A-7550 Interconnect diagram (Figure 5-1).

B. Locate the desired coaxial cable on the Interconnect diagram. (Coaxial connectors are identified by reference designators and by a callout number, which corresponds to a physically affixed tag on the coaxial cable).

C. Follow coaxial cable on Interconnect diagram to locate opposite end of connector. Note module reference designator on destination end of coaxial cable.

D. Locate schematic of desired module in the Index of Technical Drawings in Paragraph 5-3.

E. Locate reference designator of coaxial connector and continue tracing circuit.

5-2-2 MULTIPLE PIN CONNECTORS

A. Locate desired module on Interconnect diagram (Figure 5-1).

B. Locate desired multiple pin connector on Interconnect diagram. Note reference designator of the mating connector.

C. Note module or wire harness onto which the connector is to be mounted or grouped.

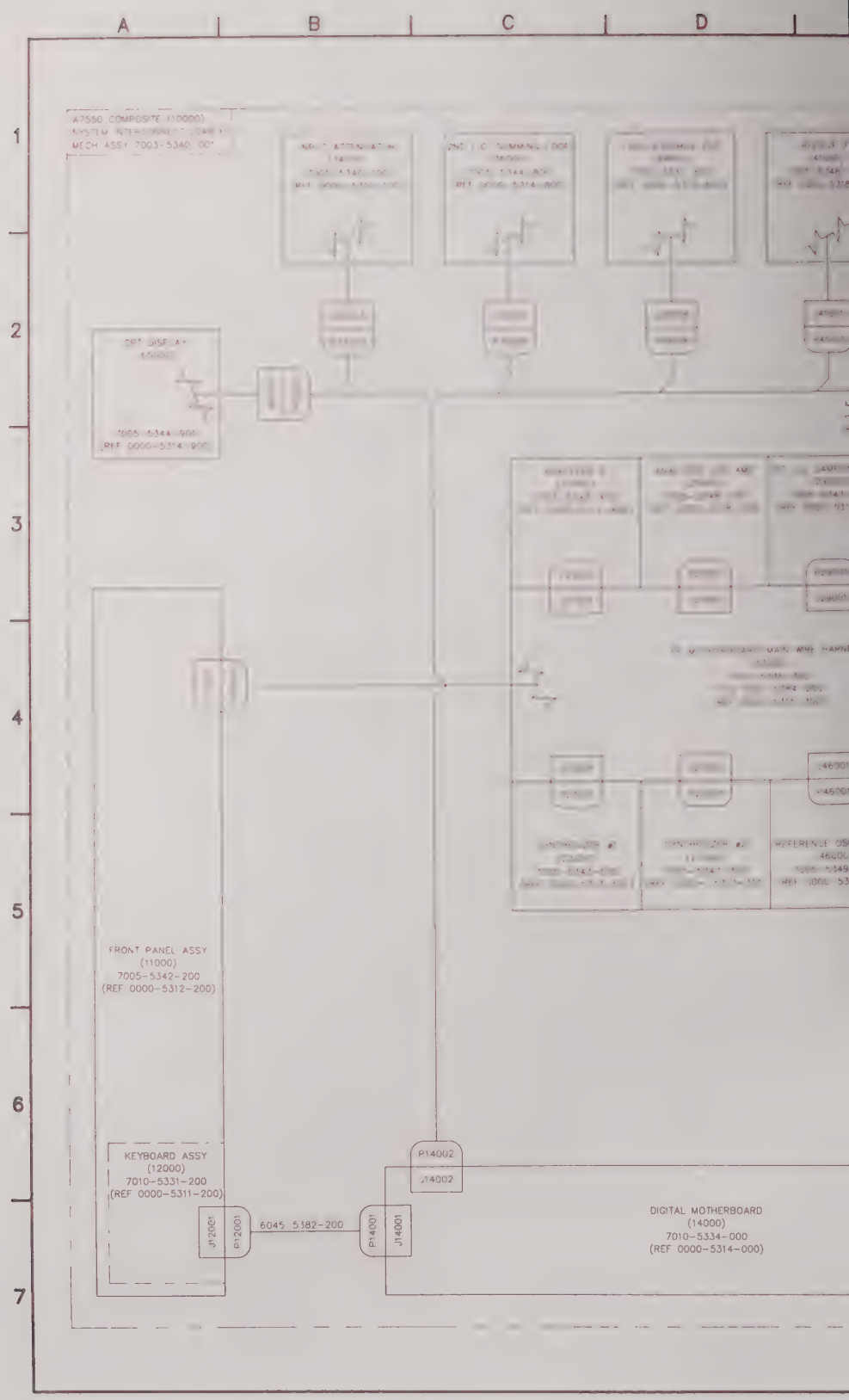
D. Locate schematic of desired module in the Index of Technical Drawings in Paragraph 5-3.

E. Using the module schematic, locate reference designator of connector and corresponding pin number. Continue tracing circuit.

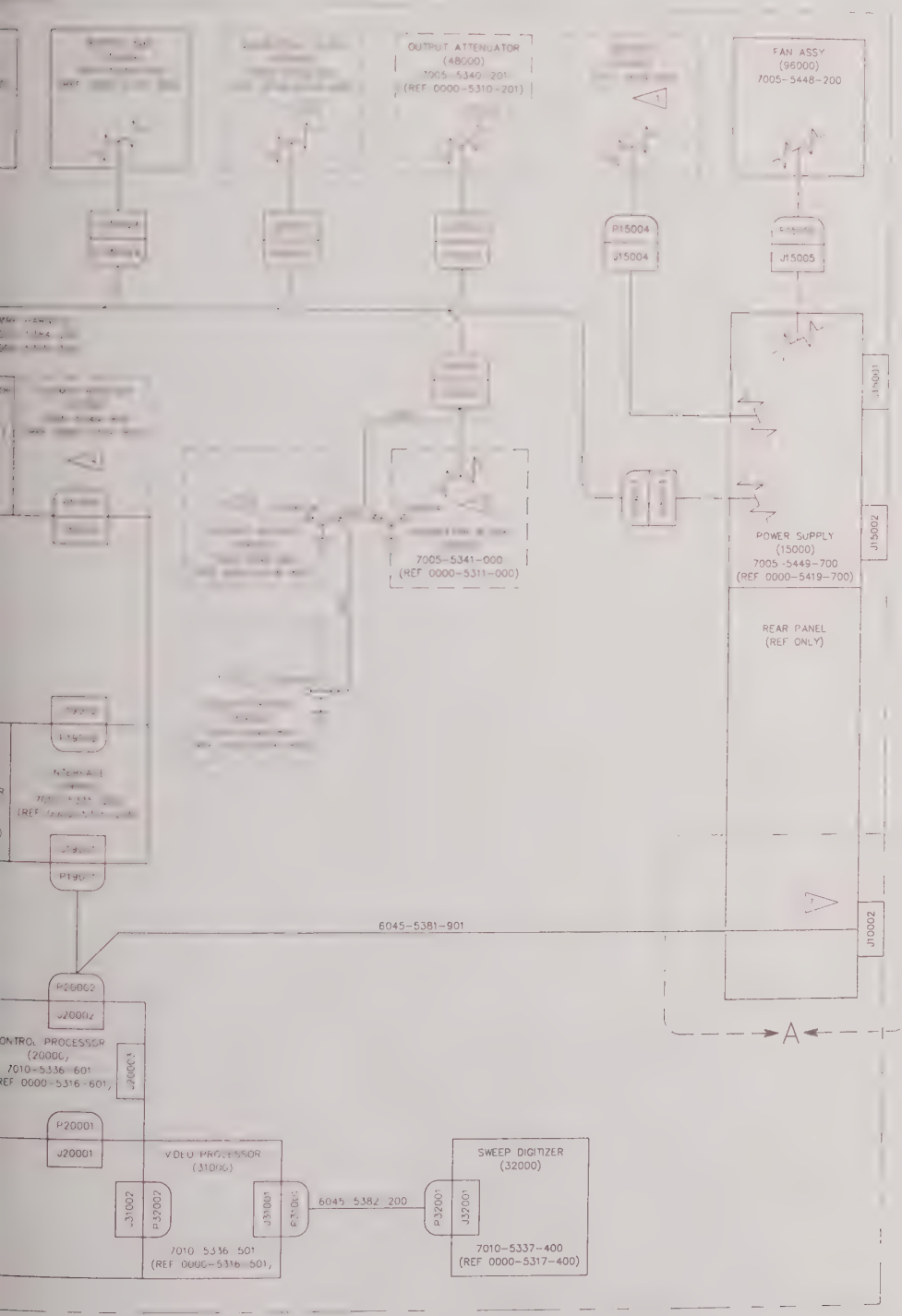
5-3 ALPHABETICAL INDEX OF TECHNICAL DRAWINGS

Title	Page
Analyzer IF Assembly	5-16
Analyzer Log Amp Assembly	5-22
A-7550 Interconnect w/Block Diagram and Coax Running List	5-4
A-7550 Power Supply Assembly	5-6
Line Rectifier PC Board Assembly	5-6
Power Supply PC Board Assembly	5-6
Battery Assembly	5-24
CRT Display Assembly	5-54
Digital Motherboard PC Board Assembly	5-25
Fan Assembly	5-12
First LO Sampling Loop Assembly	5-38
First LO Sampling Loop PC Board Assembly	5-38
Front Panel & Keyboard Assembly	5-10
GPIB PC Board Assembly	5-34
Interface PC Board Assembly	5-32
Processor PC Board Assembly	5-30
Quasi-peak Assembly	5-18
Detector PC Board Assembly	5-18
Filter PC Board Assembly	5-18
Receive IF Assembly	5-14
Auto Cal PC Board Assembly	5-14
Buffer Amp PC Board Assembly	5-14
189.3 MHz Bandpass Filter PC Board Assembly	5-14
1000 MHz Low-Pass Filter PC Board Assembly	5-14
1300 MHz Receive IF PC Board Assembly	5-14
Reference Oscillator Assembly	5-36
Reference Oscillator PC Board Assembly	5-36
RF Motherboard w/Wire Harness Assembly	5-8
RS-232C PC Board Assembly	5-35
Second LO Summing Loop Assembly	5-46
1000 MHz Multiplier PC Board Assembly	5-46
1160 MHz VCO PC Board Assembly	5-46
Second LO Mixer PC Board Assembly	5-46
Sweep Digitizer PC Board Assembly	5-26
Synthesizer #1 Assembly	5-42
Synthesizer #1 PC Board Assembly	5-42
Synthesizer #2 Assembly	5-44
Synthesizer #2 PC Board Assembly	5-44

Title	Page
Tracking Generator Installation	5-48
Generator Assembly	5-48
Generator Source PC Board Assembly	5-48
Generate Amp PC Board Assembly	5-48
1000 MHz Low-Pass Filter PC Board Assembly	5-48
1300 MHz Generate IF PC Board Assembly	5-48
Output Attenuator Assembly	5-50
0-15 dB Attenuator PC Board Assembly	5-50
0-60 dB Attenuator PC Board Assembly	5-50
Oscillator Buffer Assembly	5-52
Oscillator Buffer PC Board Assembly	5-52
Output Buffer PC Board Assembly	5-52
Output Buffer PC Board Assembly	5-52
Video Processor PC Board Assembly	5-28
0-60 dB Attenuator Assembly	5-13
0-60 dB Attenuator PC Board Assembly	5-13
10.7 MHz (FM/AM/SSB) Receiver Assembly	5-20
10.7 MHz Receiver PC Board Assembly	5-20
+20 dB External Amplifier Assembly	5-41
+20 dB External Amp PC Board Assembly	5-41
1350-2350 MHz VCO Assembly	5-40
1380-2350 MHz VCO Filter PC Board Assembly	5-37


A
B
C
D
1
2
3
4
5
6
7
A7550 COMPOSITE (10000)
SYSTEM INTERCONNECT CABLE
MECH ASSY 7003-5340-00*
FRONT PANEL ASSY
(11000)
7005-5342-200
(REF 0000-5312-200)
KEYBOARD ASSY
(12000)
7010-5331-200
(REF 0000-5311-200)
J12001
P12001
6045 5382-200
P14001
J14001
P14002
J14002
DIGITAL MOTHERBOARD
(14000)
7010-5334-000
(REF 0000-5314-000)

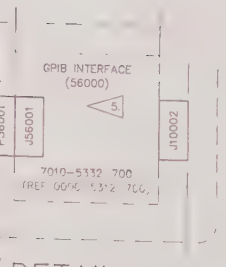
E F G H J K


OUTPUT ATTENUATOR
(48000)
7005-5340-201
(REF 0000-5310-201)
FAN ASSY
(96000)
7005-5448-200
P15004
J15004
J15005
J15001
J15002
POWER SUPPLY
(15000)
7005-5449-700
(REF 0000-5419-700)
7005-5341-000
(REF 0000-5311-000)
REAR PANEL
(REF ONLY)
J10002
6045-5381-901
A
P20002
J20002
ONTRO. PROCESSOR
(20000)
7010-5336-601
REF 0000-5316-601)
J20003
P20001
J20001
VIDEO PROCESSOR
(31000)
J31002
P31002
J31001
P31001
6045-5382-200
SWEEP DIGITIZER
(32000)
P32001
J32001
7010-5336-501
(REF 0000-5316-501)
7010-5337-400
(REF 0000-5317-400)

NOTES:

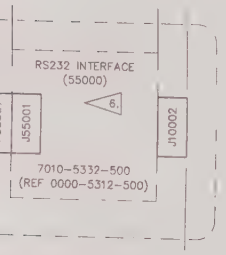
1. OPTION 1, RECHARGEABLE BATTERY.
2. OPTION 2, TRACKING GENERATOR: INCLUDES GEN BLOCK, OUTPUT ATTENUATOR. OUTPUT BUFFERS, COAX CABLES & ATTACHING HARDWARE.
3. +20 dB EXTERNAL AMPLIFIER (ACCESSORY ITEM): USED WITH TRACKING GENERATOR (OPTION 2).
4. OPTION 4, 10.7 MHz (FM/AM/SSB) RECEIVER: SEE NOTE 8 WHEN QUASI-PEAK OPTION IS INSTALLED.
5. OPTION 5, GPIB (IEEE 488-1978): SEE NOTE 7.
6. OPTION 6, RS-232C INTERFACE: SEE NOTE 7.
7. WHEN GPIB IS INSTALLED, J10002 IS P56001. WHEN RS-232C IS INSTALLED, J10002 IS P55001. GPIB AND RS-232C OPTIONS CANNOT BE INSTALLED AT THE SAME TIME.
8. OPTION 8, QUASI-PEAK MODULE: INCLUDES COAXES AND ATTACHING HARDWARE. FOLLOWING IS A CHART OF COAX CABLE HOOKUP USING QUASI-PEAK AND/OR 10.7 MHz RECEIVER OPTIONS:

TAG NO	FROM	TO	WHEN USED
5	J41008	J21003	STD COAX
	J41008	J57002	W/OPT 4 ONLY
	NOT USED		W/OPT 8
7	J57003	J21003	W/OPTS 4 & 8
8	J62005	J32003	STD COAX
30	J62003	J57002	W/OPTS 4 & 8
	J62003	J21003	W/OPT 8 ONLY
31	J41008	J62002	W/ALL OPT 8
41	J62004	J25002	W/ALL OPT 8



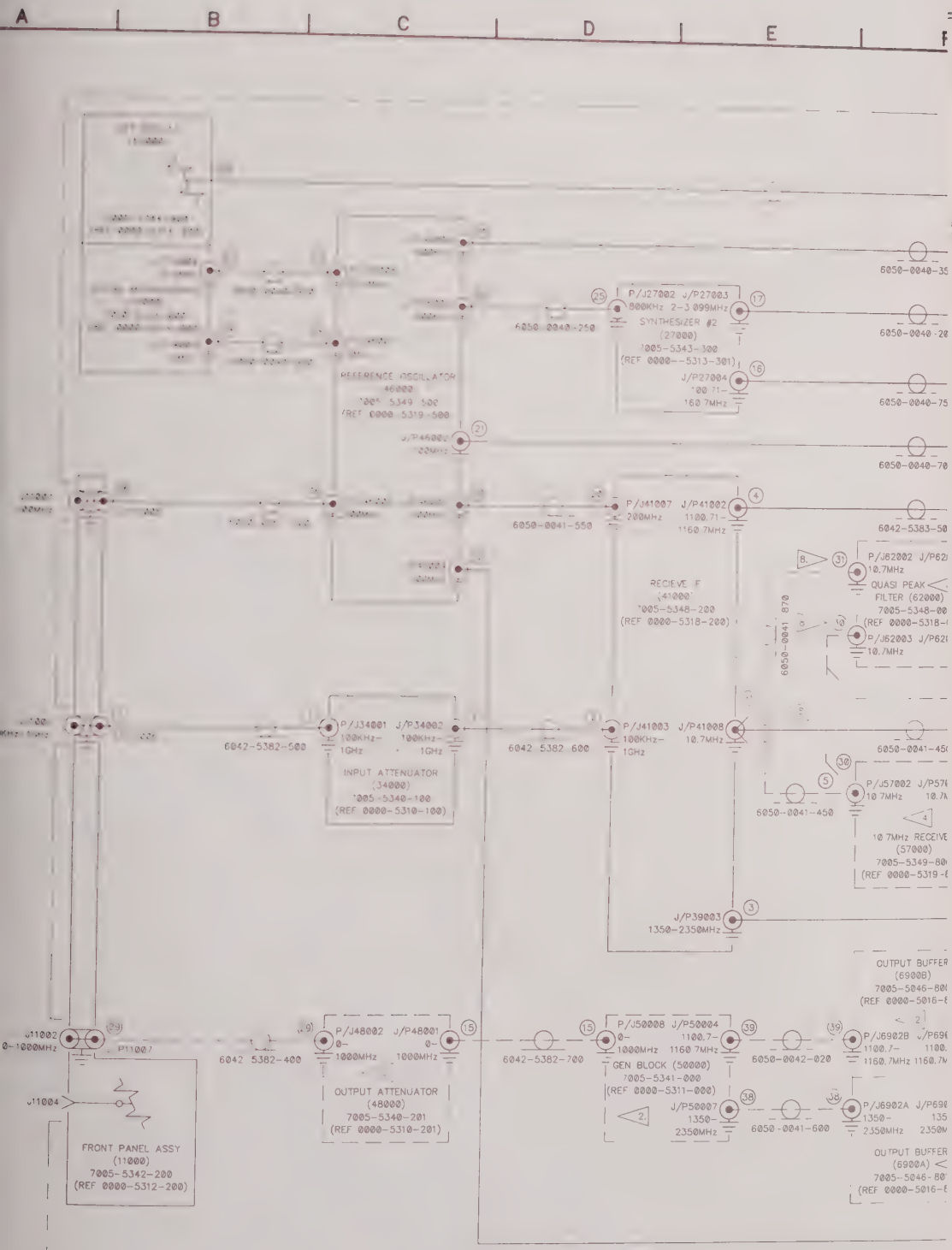
DETAIL A

TION 5 (GPIB INTERFACE) IS INSTALLED



DETAIL A

ON 6 (RS232 INTERFACE) IS INSTALLED


A
B
C
D
E
F
REFERENCE OSCILLATOR
(46000)
7005-5349-500
(REF 0000-5319-500)
P/J27002 J/P27003
800KHz 2-3 099MHz
SYNTHESIZER #2
(27000)
7005-5343-300
(REF 0000--5313-301)
J/P27004
160.7MHz
6050-0040-250
6050-0040-35
6050-0040-28
6050-0040-75
6050-0040-70
P/J41007 J/P41002
200MHz 1160.7MHz
6050-0041-550
6042-5383-50
RECEIVE IF
(41000)
7005-5348-200
(REF 0000-5318-200)
P/J62002 J/P62
10.7MHz
QUASI PEAK
FILTER (62000)
7005-5348-00
(REF 0000-5318-
P/J62003 J/P62
10.7MHz
6050-0041-870
P/J34001 J/P34002
100KHz- 100KHz-
1GHz 1GHz
INPUT ATTENUATOR
(34000)
7005-5340-100
(REF 0000-5310-100)
6042-5382-500
6042-5382-600
P/J41003 J/P41008
100KHz- 10.7MHz
1GHz
6050-0041-45
P/J57002 J/P57
10.7MHz 10.7
6050-0041-450
10.7MHz RECEIVE
(57000)
7005-5349-80
(REF 0000-5319-
J/P39003
1350-2350MHz
OUTPUT BUFFER
(69008)
7005-5046-80
(REF 0000-5016-
J11002
0-1000MHz
P11007
J11004
FRONT PANEL ASSY
(11000)
7005-5342-200
(REF 0000-5312-200)
6042-5382-400
P/J48002 J/P48001
0- 0-
1000MHz 1000MHz
OUTPUT ATTENUATOR
(48000)
7005-5340-201
(REF 0000-5310-201)
6042-5382-700
P/J50008 J/P50004
0- 1100.7-
1000MHz 1160.7MHz
GEN BLOCK (50000)
7005-5341-000
(REF 0000-5311-000)
J/P50007
1350-
2350MHz
6050-0042-020
6050-0041-600
P/J6902B J/P69
1100.7- 1100.
1160.7MHz 1160.7M
P/J6902A J/P69
1350- 135
2350MHz 2350M
OUTPUT BUFFER
(6900A)
7005-5046-80
(REF 0000-5016-

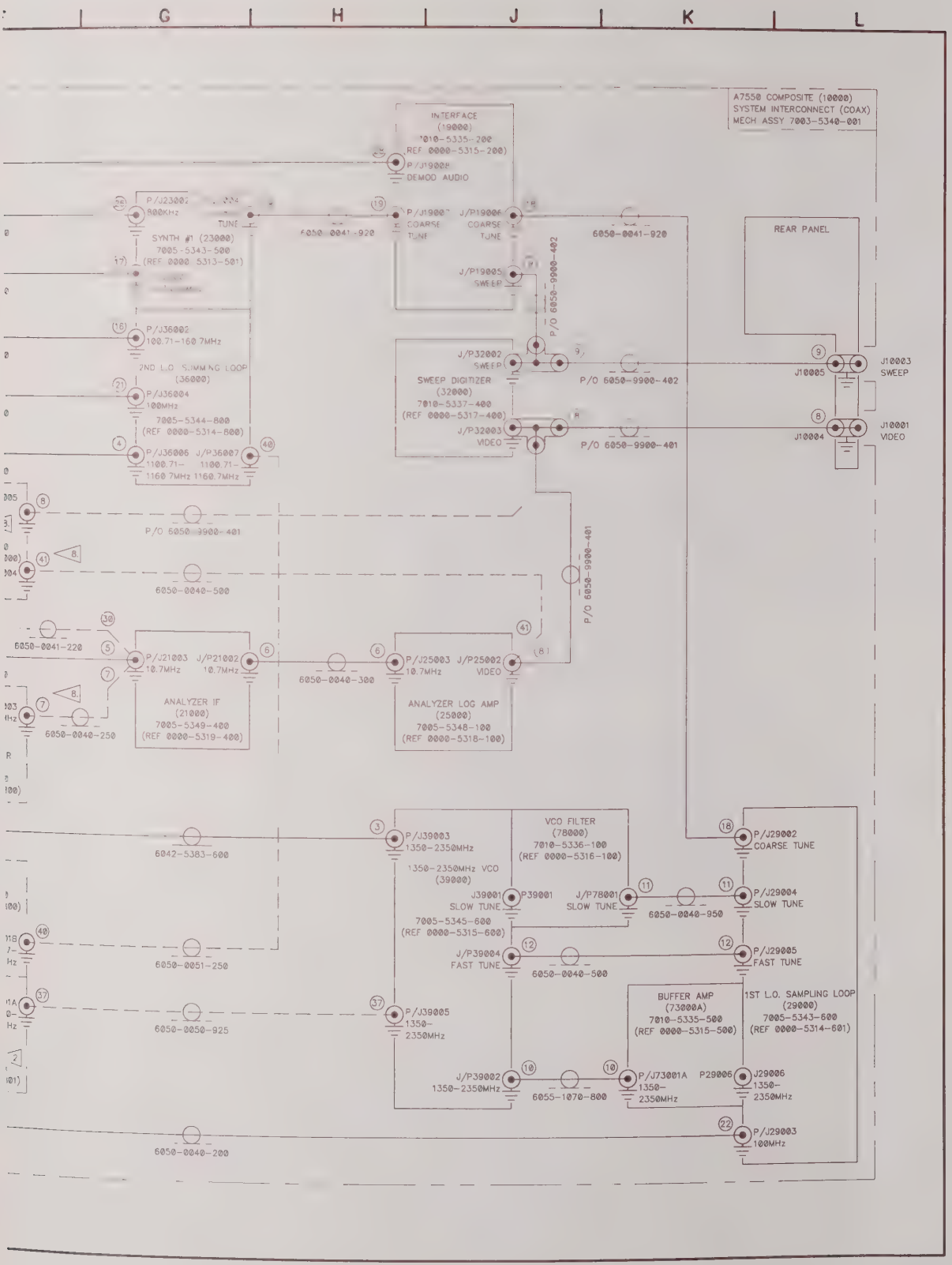


Figure 5-1 A-7550 Interconnect w/Block Diagram and Coax Running List (Sheet 1 of 2) (0000-5310-001-D)

COAX	DPN	FROM	TO	SIGNAL	
1	6042-5382-500	J/P11001-JP/11006 (Front Panel)	J34001 (Input Attenuator)	100 kHz to 1000 MHz	-12
2	6042-5382-600	J/P34002 (Input Attenuator)	J/P41003 (Receive IF)	100 kHz to 1000 MHz	-12
3	6042-5383-600	J/P39003 (VCO)	J/P73001B (Receive IF via Buffer Amp)	1350 to 2350 MHz	+5
4	6042-5383-500	J/P36006 (2nd LO)	J/P41002 (Receive IF)	1100.7 to 1160.7 MHz	+5
**#5	6050-0041-450	J/P41008 (Receive IF)	J/P21003 (Analyzer IF) or J/P57002 (10.7 MHz Receiver)	10.7 MHz	0 d
#6	6050-0040-300	J/P21002 (Analyzer IF)	J/P25003 (Analyzer Log Amp)	10.7 MHz	0 d
*7	6050-0040-250	J/P57003 (10.7 MHz Receiver)	J/P21003 (Analyzer IF)	10.7 MHz	0 d
**8	6050-9900-401	J/P25002 (Log AMP) or J/P62005 (Quasi-Peak)	J/P32003 & J/P10004-J/P10001 (Sweep Digitizer Analog Video Out)	Video	0 t (Va
9	6050-9900-402	J/P32002 (Sweep Digitizer)	J/P19005 & J/P10005-J/P10003 (Interface/Rear Panel & Sweep Out)	Sweep (Ramp)	+5
10	6055-1070-800	J/P39002 (VCO)	J/P73001A (1st LO via Buffer Amp)	1350 to 2350 MHz	+5
11	6050-0040-950	J/P78001 (1st LO)	J/P29004 (1st LO)	Slow Tune	0 t
12	6050-0040-500	J/P29005 (1st LO)	J/P39004 (VCO)	Fast Tune	0 t
*15	6042-5382-700	J/P50008 (Tracking Gen)	J/P48001 (Output Atten)	0 to 1000 MHz	0 d
16	6050-0040-750	J/P27004 (Synth #2)	J/P36002 (2nd LO)	100.7 to 160.7 MHz	+5
17	6050-0040-200	J/P23003 (Synth #1)	J/P27003 (Synth #2)	.2 to 3.099 MHz	TTL
18	6050-0041-920	J/P19006 (Interface)	J/P29002 (1st LO)	Coarse Tune	0 t
19	6050-0041-920	J/P19007 (Interface)	J/P23004 (Synth #1)	Coarse Tune	0 t
20	6050-0041-550	J/P46003 (Ref Osc)	J/P41007 (Receive IF)	200 MHz	+5
21	6050-0040-700	J/P46002 (Ref Osc)	J/P36004 (2nd LO)	100 MHz	+5
22	6050-0040-200	J/P46004 (Ref Osc)	J/P29003 (1st LO)	100 MHz	+5

LEVEL
) to +30 dBm
) to +30 dBm
Bm
Bm
m REF
m REF
m REF
0.8 V id Video)
, 50 mS
Bm
20 VDC
5 VDC
m
Bm
5 VDC
2.5 VDC
Bm
Bm
Bm

COAX	DPN	FROM	TO
23	6050-0040-950	J/P46008 (Ref Osc)	J/P14004 (Digital Motherboard)
24	6050-0040-950	J/P46007 (Ref Osc)	J/P14003 (Digital Motherboard)
25	6050-0040-250	J/P46005 (Ref Osc)	J/P27002 (Synth #2)
26	6050-0040-350	J/P46006 (Ref Osc)	J/P23002 (Synth #1)
27	6050-0040-550	J/P36008 (2nd LO)	J/P36009 (2nd LO)
28	6050-1050-850	J/P19008 (Interface)	Speaker (CRT)
*29	6042-5382-400	J/P48002 (Output Atten)	J/P11002-J/P11007 (Front Pnl/Gen Out)
*30	6050-0041-220	J/P62003 (Quasi-Peak Filter)	J/P21003 (Analyzer IF) or J/P57002 (10.7 MHz Receiver)
*31	6050-0041-870	J/P41008 (Receive IF)	J/P62002 (Quasi-Peak Filter)
*32	6050-0040-250	J/P50002 (Tracking Gen)	J/P50003 (Tracking Gen)
*33	6050-0040-250	J/P50006 (Tracking Gen)	J/P50005 (Tracking Gen)
34	6050-0040-450	J/P41005 (Receive IF)	J/P41006 (Receive IF
35	6050-0040-250	J/P36005 (2nd LO)	J/P36003 (2nd LO)
36	6050-0561-300	J/P46009 (Ref Osc)	J/P11003-J/P11008 (Front Panel CAL Output)
*37	6050-0050-925	J/P39005 (VCO)	J/P6901A (Output Buffer-Tracking Gen)
*38	6050-0041-600	J/P6902A (Output Buffer-Tracking Gen)	J/P50007 (Tracking Gen)
*39	6050-0042-020	J/P6902B (Output Buffer-Tracking Gen)	J/P50004 (Tracking Gen)
*40	6050-0051-250	J/P36007 (2nd LO)	J/P6901B (Output Buffer-Tracking Gen)
*41	6050-0040-500	J/P25002 (Analyzer Log Amp)	J/P62004 (Quasi-Peak Det)

\# COAX NOT USED IF QUASI-PEAK MODULE IS INSTALLED
* COAX USED IF OPTION IS INSTALLED
** COAX ROUTED DEPENDING ON INSTALLED OPTIONS

	SIGNAL	LEVEL
	12.5 MHz	TTL
	5 MHz	TTL
	800 kHz	TTL
	800 kHz	TTL
	100.7 to 160.7 MHz	-19 dBm
	Demod Audio	--
	0 to 1000 MHz	-60 to 0 dBm
	10.7 MHz	0 dBm REF
	10.7 MHz	0 dBm REF
	189.3 MHz	-20 dBm
	0 to 1000 MHz	-30 dBm
	189.3 MHz	Input @ J41003
	1100.7 to 1160.7 MHz	+5 dBm
	100 MHz	-30 dBm
	1350 to 2350 MHz	+5 dBm
	1350 to 2350 MHz	+5 dBm
	1100.7 to 1160.7 MHz	+5 dBm
	1100.7 to 1160.7 MHz	+5 dBm
	Video	0 to 0.8 V

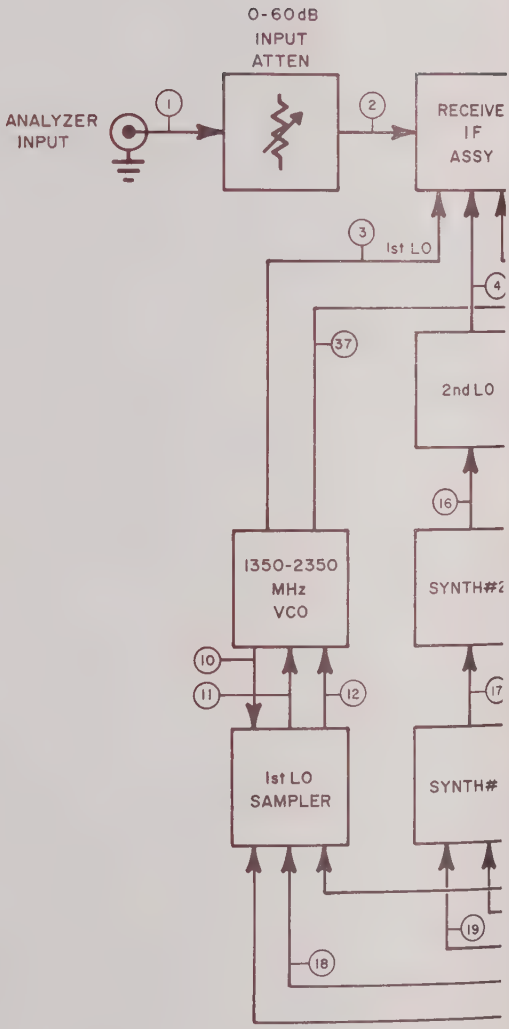
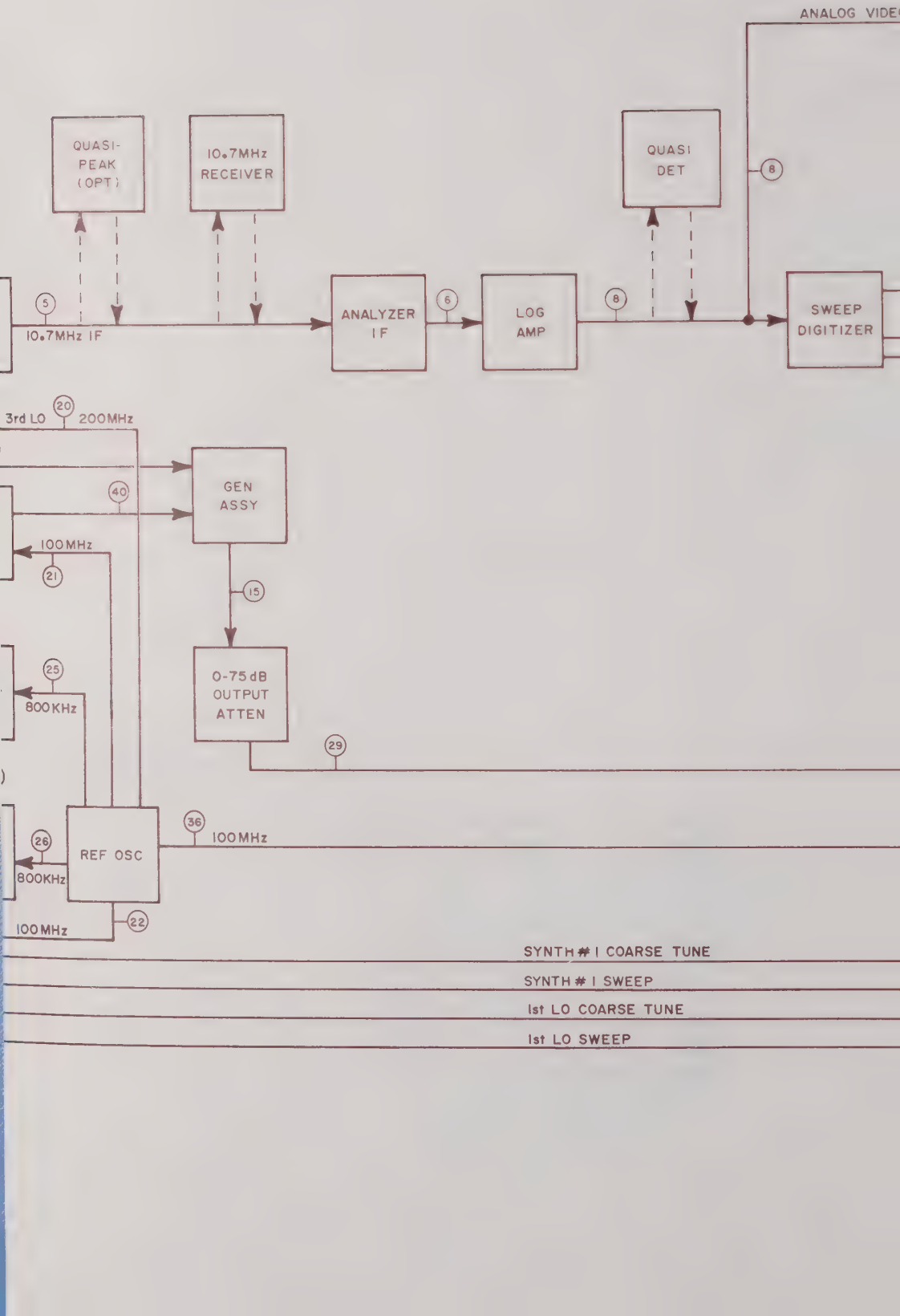


TABLE 5-1 A-7550 COAX RUNNING LIST


ANALOG VIDE
QUASI-
PEAK
(OPT)
10.7MHz
RECEIVER
QUASI
DET
8
5
10.7MHz IF
ANALYZER
IF
6
LOG
AMP
8
SWEEP
DIGITIZER
3rd LO
20
200MHz
40
GEN
ASSY
100MHz
21
15
25
800KHz
0-75dB
OUTPUT
ATTEN
29
36
100MHz
26
REF OSC
800KHz
100MHz
22
SYNTH # 1 COARSE TUNE
SYNTH # 1 SWEEP
1st LO COARSE TUNE
1st LO SWEEP

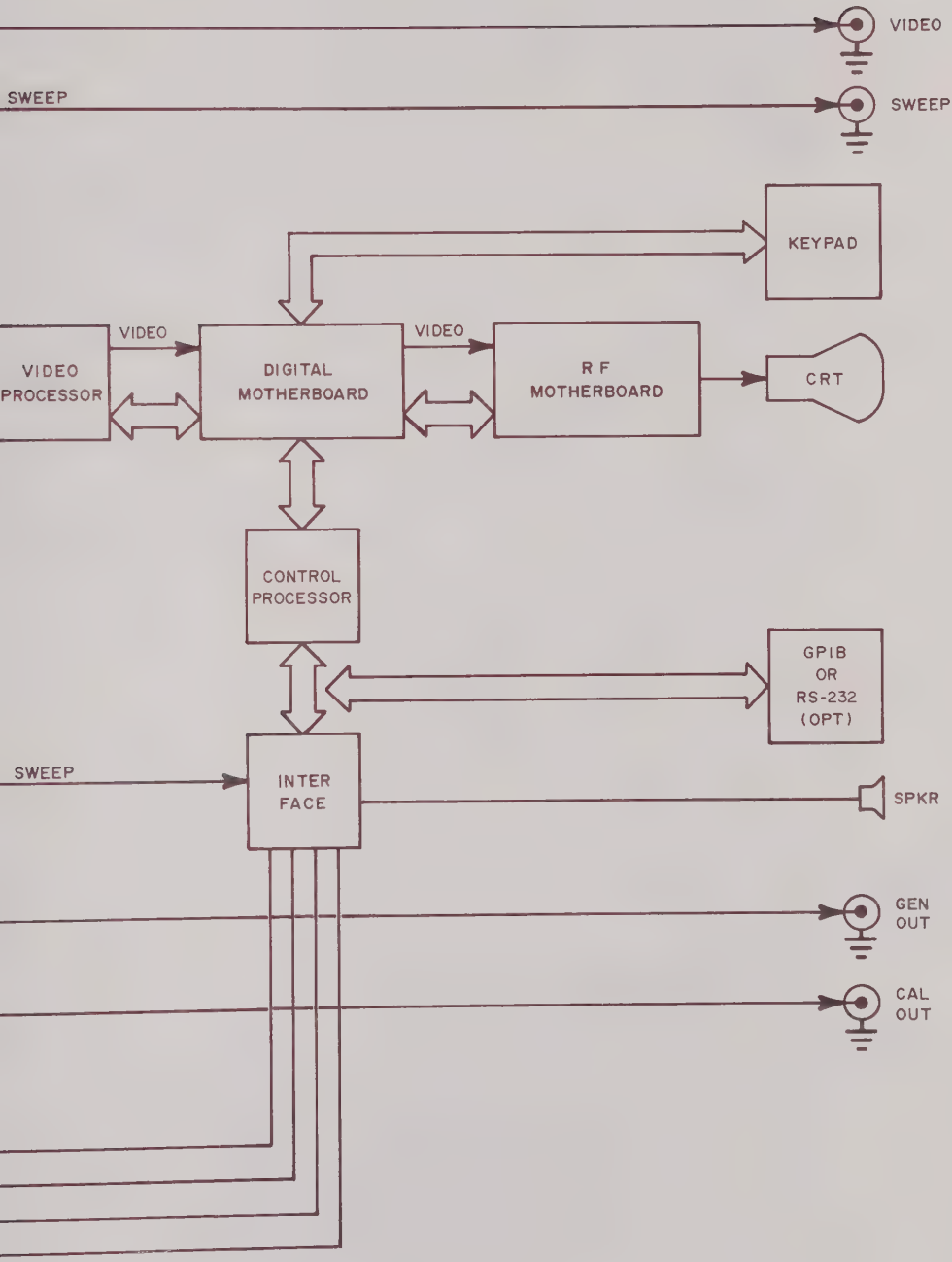
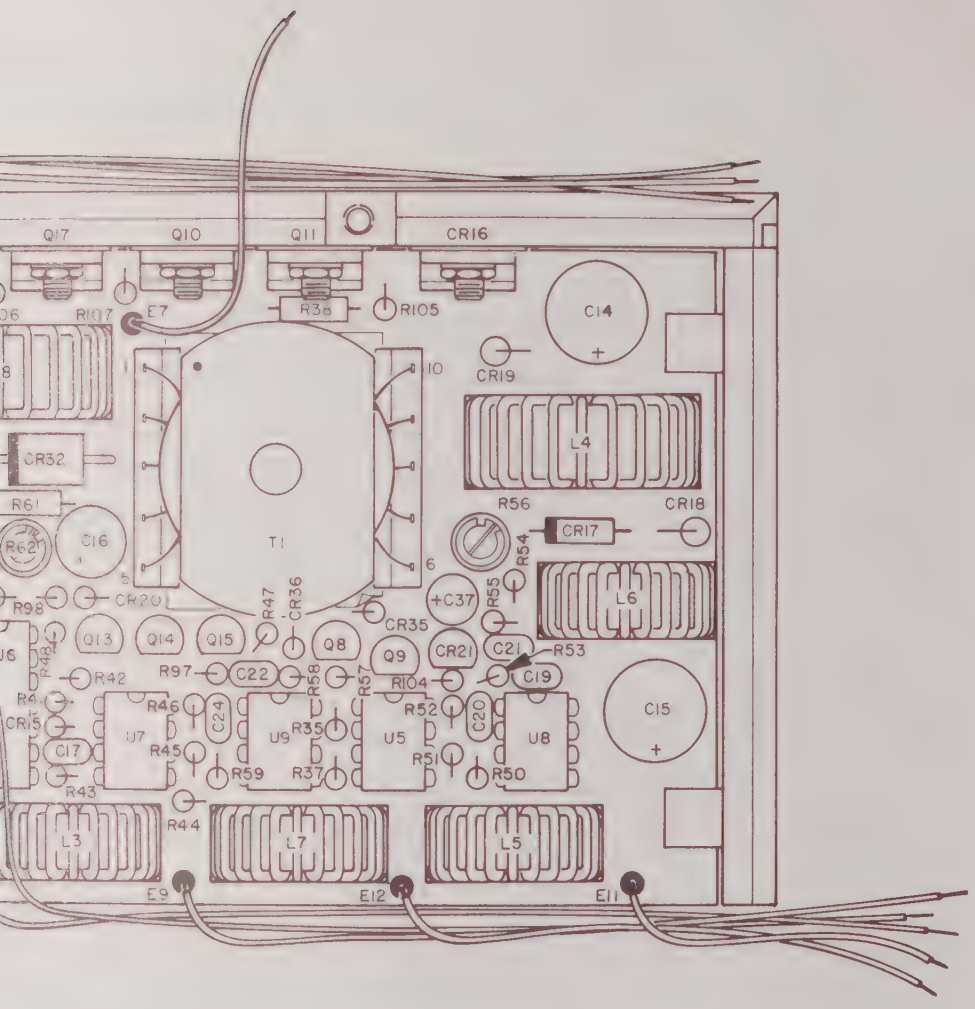
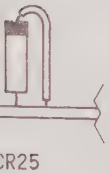


Figure 5-1 A-7550 Interconnect w/Block Diagram and Coax Running List (Sheet 2 of 2) (0000-5310-001-D)



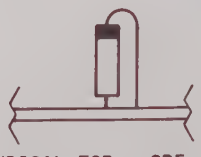


CR25

DETAIL **F**

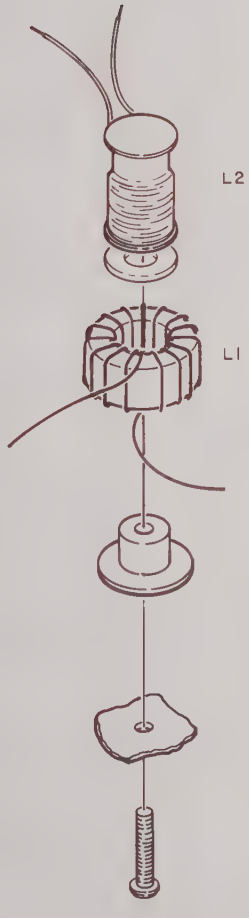
TYPICAL FOR: CR1, CR2, CR3, CR4, CR6, CR7, CR8, CR11, CR12, CR14, CR15, CR18, CR20, CR34, CR35, CR37

DETAIL **G**



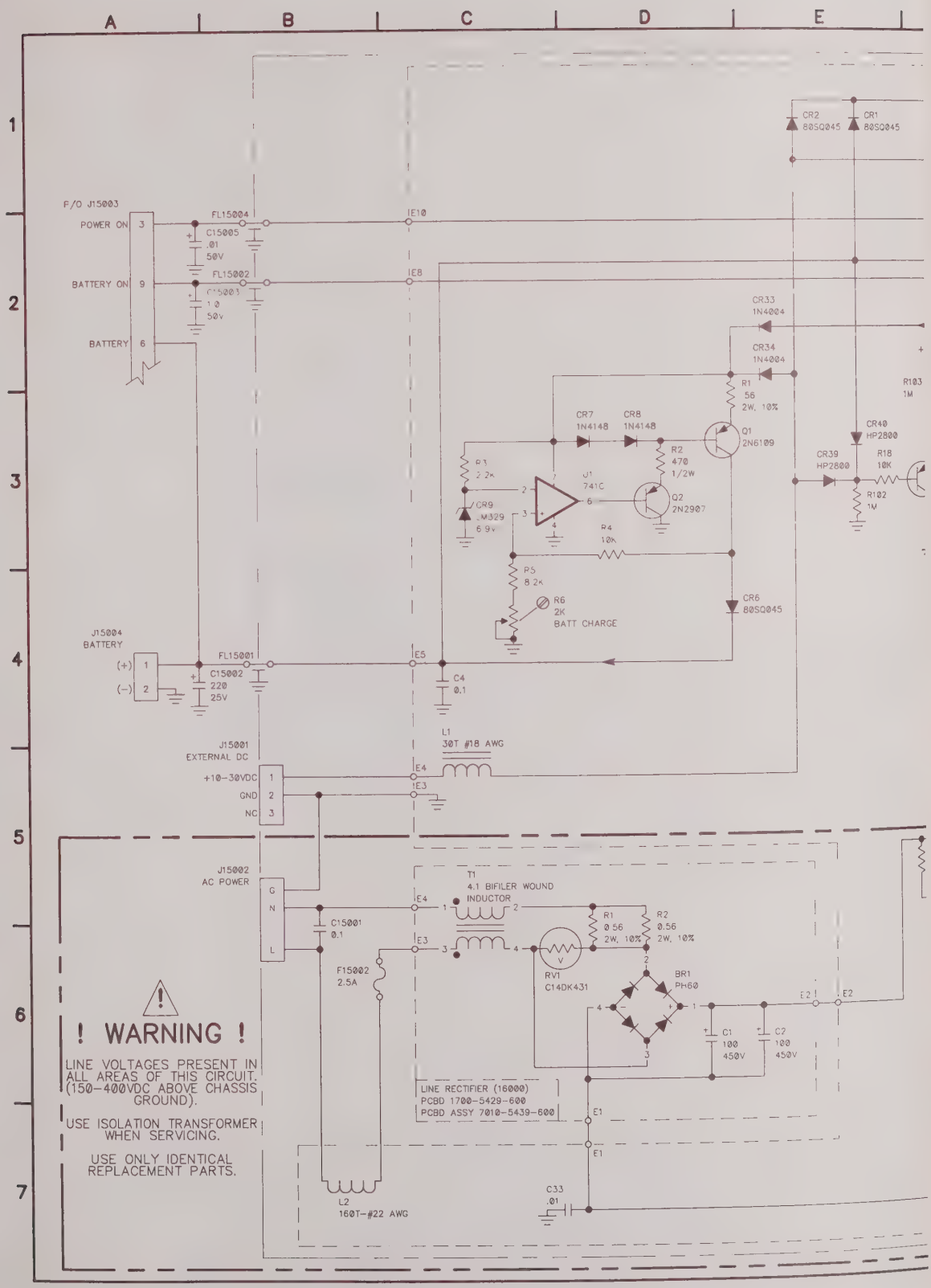
TYPICAL FOR: CR5, CR10, CR13, CR19, CR22, CR36, CR38, CR39, CR40

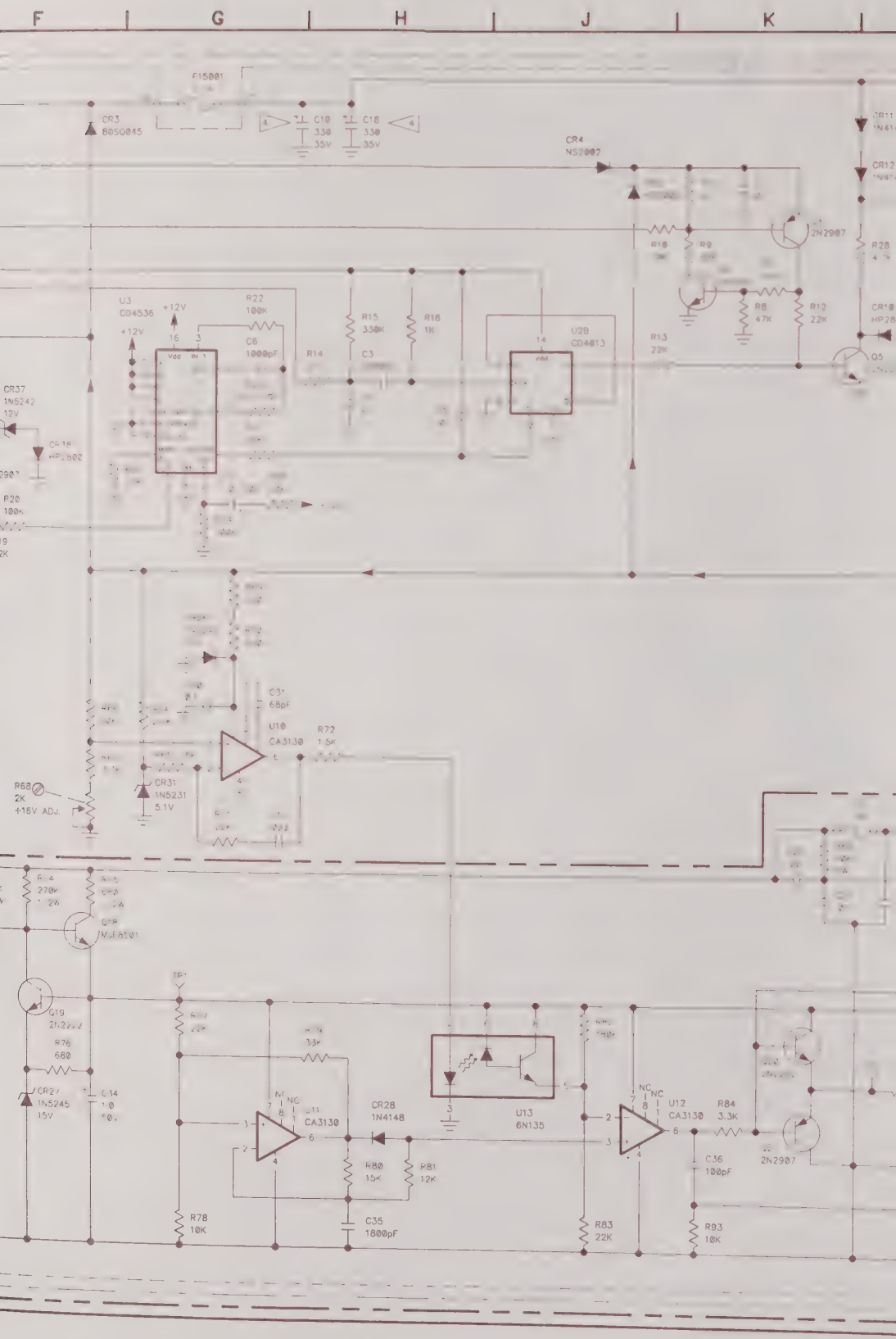
DETAIL **H**

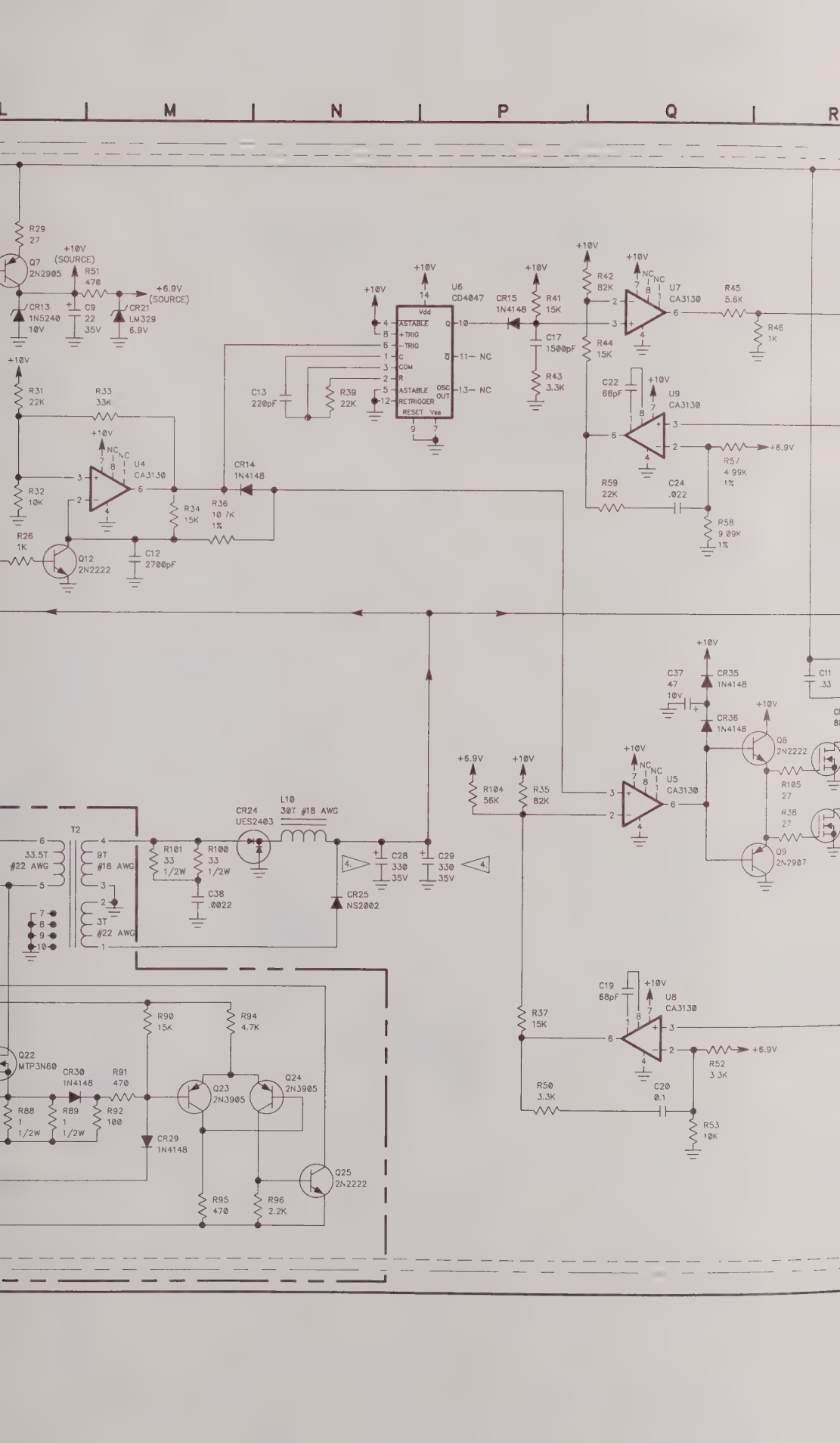


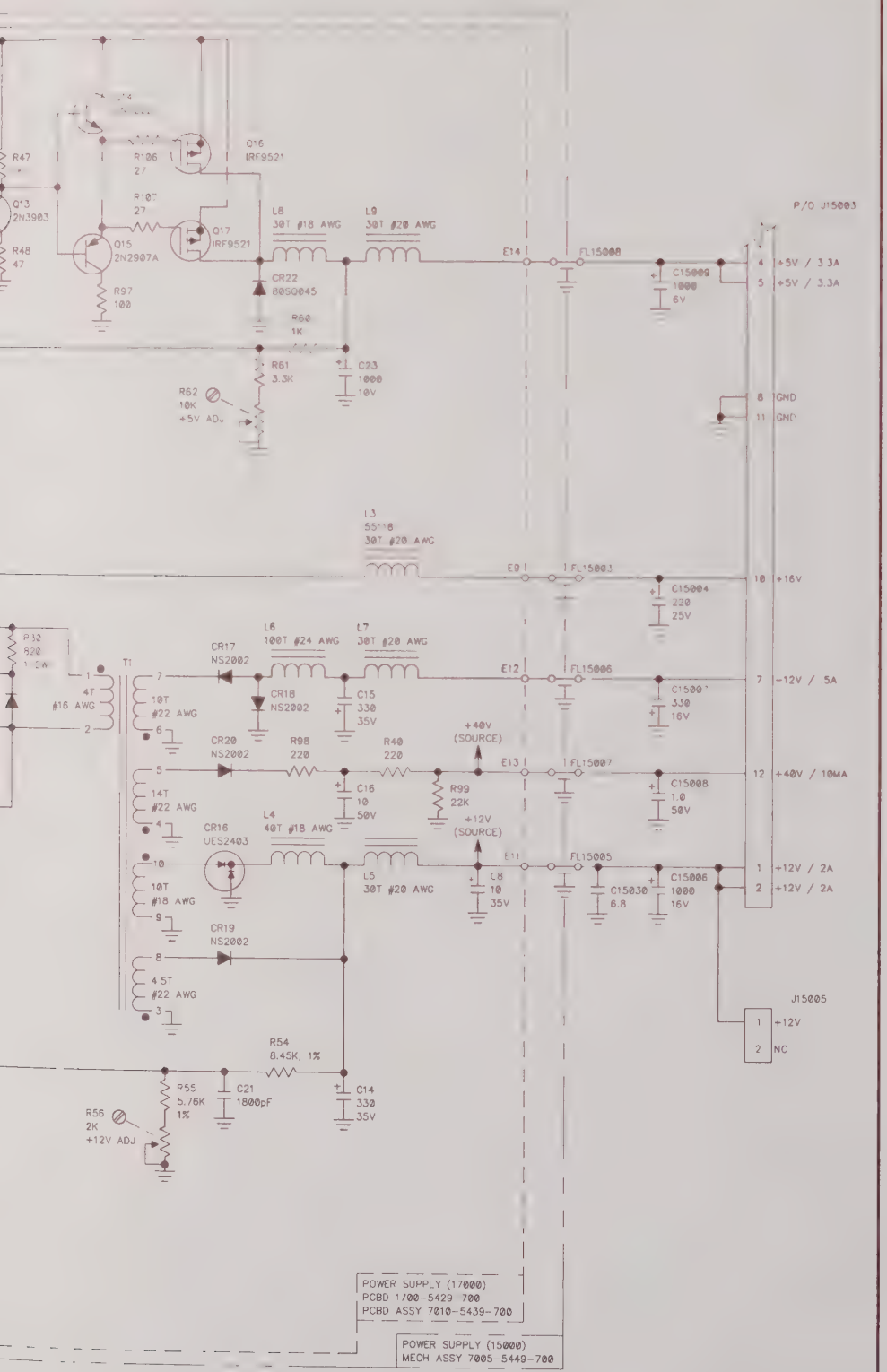
DETAIL **J**

Figure 5-2 A-7550 Power Supply Assembly (Sheet 1 of 2) (0000-5419-700-A5)


A
B
C
D
E
1
2
3
4
5
6
7
CR2
80SQ045
CR1
80SQ045
F/O J15003
POWER ON
3
BATTERY ON
9
BATTERY
6
FL15004
C15005
.01
50V
FL15002
C15003
1.0
50V
E10
E8
CR33
1N4004
CR34
1N4004
R1
56
2W, 10%
R103
1M
CR7
1N4148
CR8
1N4148
Q1
2N6109
R2
470
1/2W
CR40
HP2800
CR39
HP2800
R18
10K
R102
1M
R3
2.2K
U1
741C
CR9
LM329
6.9V
Q2
2N2907
R4
10K
R5
8.2K
R6
2K
BATT CHARGE
CR6
80SQ045
J15004
BATTERY
(+)
1
(-)
2
FL15001
C15002
220
25V
E5
C4
0.1
L1
30T #18 AWG
J15001
EXTERNAL DC
+10-30VDC
1
GND
2
NC
3
E4
E3
J15002
AC POWER
G
N
L
T1
4:1 BIFILER WOUND
INDUCTOR
C15001
0.1
F15002
2.5A
R1
0.56
2W, 10%
R2
0.56
2W, 10%
RV1
C14DK431
BR1
PH60
C1
100
450V
C2
100
450V
E2
LINE RECTIFIER (16000)
PCBD 1700-5429-600
PCBD ASSY 7010-5439-600
E1
L2
160T-#22 AWG
C33
.01
! WARNING !
LINE VOLTAGES PRESENT IN ALL AREAS OF THIS CIRCUIT. (150-400VDC ABOVE CHASSIS GROUND).
USE ISOLATION TRANSFORMER WHEN SERVICING.
USE ONLY IDENTICAL REPLACEMENT PARTS.


F
G
H
J
K
F15001
CR3
80SQ045
C10
330
35V
C18
330
35V
CR4
NS2002
2N2907
R10
R9
R8
47K
R12
22K
R13
22K
R28
CR10
HP28
Q5
U3
CD4536
+12V
R22
100K
C6
1000pF
R14
R15
330K
R16
1K
C3
U2B
CD4013
CR37
1N5242
12V
R20
100K
C31
68pF
U10
CA3130
R72
1.5K
R68
2K
+16V ADJ.
CR31
1N5231
5.1V
Q19
2N2222
R76
680
CR27
1N5245
15V
C34
TP1
R78
10K
CA3130
CR28
1N4148
R80
15K
R81
12K
C35
1800pF
U13
6N135
U12
CA3130
R84
3.3K
C36
100pF
R83
22K
R93
10K
2N2907


L
M
N
P
Q
R
R29
27
Q7
2N2905
+10V
(SOURCE)
R51
470
+6.9V
(SOURCE)
CR13
1N5240
10V
C9
22
35V
CR21
LM329
6.9V
+10V
R31
22K
R33
33K
U4
CA3130
R32
10K
R34
15K
R36
10.7K
1%
CR14
1N4148
R26
1K
Q12
2N2222
C12
2700pF
U6
CD4047
Vdd
ASTABLE
+TRIG
-TRIG
C
COM
R
ASTABLE
RETRIGGER
RESET
Vss
OSC OUT
NC
C13
220pF
R39
22K
CR15
1N4148
R41
15K
C17
1500pF
R43
3.3K
R42
82K
R44
15K
U7
CA3130
R45
5.6K
R46
1K
C22
68pF
U9
CA3130
R57
4.99K
1%
+6.9V
R59
22K
C24
.022
R58
9.09K
1%
T2
33.5T
#22 AWG
9T
#18 AWG
3T
#22 AWG
R101
33
1/2W
R100
33
1/2W
C38
.0022
CR24
UES2403
L10
30T #18 AWG
CR25
NS2002
C28
330
35V
C29
330
35V
R104
56K
R35
82K
U5
CA3130
C37
47
10V
CR35
1N4148
CR36
1N4148
Q8
2N2222
R105
27
R38
27
Q9
2N2907
C11
.33
R37
15K
C19
68pF
U8
CA3130
R52
3.3K
R50
3.3K
C20
0.1
R53
10K
Q22
MTP3N60
CR30
1N4148
R91
470
R88
1
1/2W
R89
1
1/2W
R92
100
R90
15K
R94
4.7K
Q23
2N3905
Q24
2N3905
CR29
1N4148
Q25
2N2222
R95
470
R96
2.2K


R47
Q13
2N3903
R48
47
R106
27
Q16
IRF9521
R107
27
Q15
2N2907A
Q17
IRF9521
R97
100
L8
30T #18 AWG
L9
30T #20 AWG
CR22
80S0045
R60
1K
R61
3.3K
C23
1000
10V
R62
10K
+5V ADJ
E14
FL15008
C15009
1000
6V
P/O J15003
4 +5V / 3.3A
5 +5V / 3.3A
8 GND
11 GND
L3
30T #20 AWG
E9
FL15003
C15004
220
25V
10 +16V
L6
100T #24 AWG
L7
30T #20 AWG
CR17
NS2002
CR18
NS2002
C15
330
35V
E12
FL15006
C15007
330
16V
7 -12V / .5A
T1
4T
#16 AWG
10T
#22 AWG
14T
#22 AWG
10T
#18 AWG
4.5T
#22 AWG
CR20
NS2002
R98
220
R40
220
+40V
(SOURCE)
C16
10
50V
R99
22K
E13
FL15007
C15008
1.0
50V
12 +40V / 10MA
L4
40T #18 AWG
CR16
UES2403
L5
30T #20 AWG
+12V
(SOURCE)
C8
10
35V
E11
FL15005
C15030
6.8
C15006
1000
16V
1 +12V / 2A
2 +12V / 2A
CR19
NS2002
J15005
1 +12V
2 NC
R54
8.45K, 1%
R55
5.76K
1%
C21
1800pF
C14
330
35V
R56
2K
+12V ADJ
POWER SUPPLY (17000)
PCBD 1700-5429-700
PCBD ASSY 7010-5439-700
POWER SUPPLY (15000)
MECH ASSY 7005-5449-700

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS USE THE FOLLOWING SERIES:

   A. LINE RECTIFIER PC BD ASSY - 16000
   B. POWER SUPPLY PC BD ASSY - 17000
   C. POWER SUPPLY MECH ASSY - 15000

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

4. C10, C18, C28 AND C29 ARE INSTALLED AT THE MECH ASSY LEVEL.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

Figure 5-2 A-7550 Power Supply Assembly (Sheet 2 of 2) (0000-5419-700-A5)

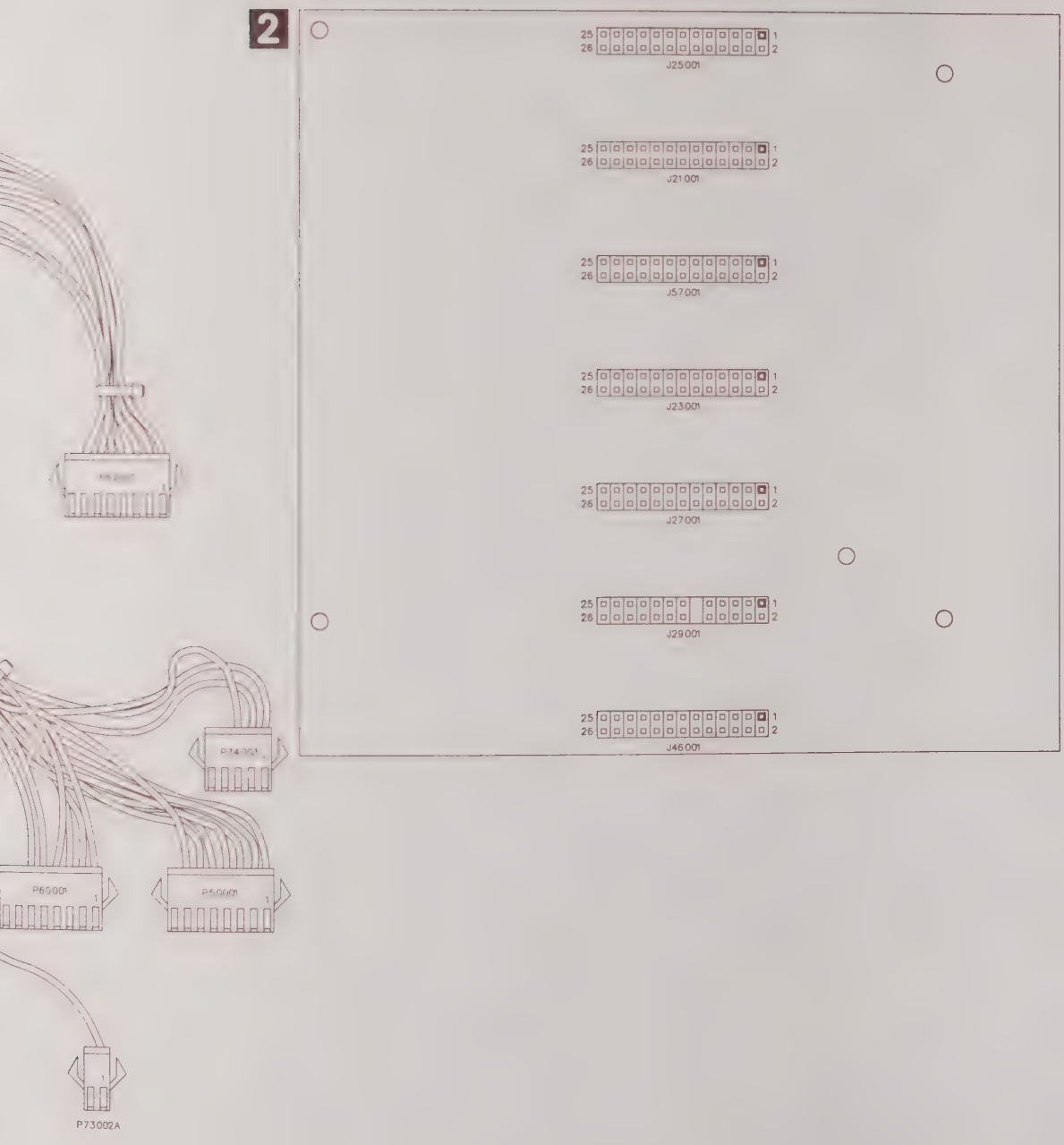
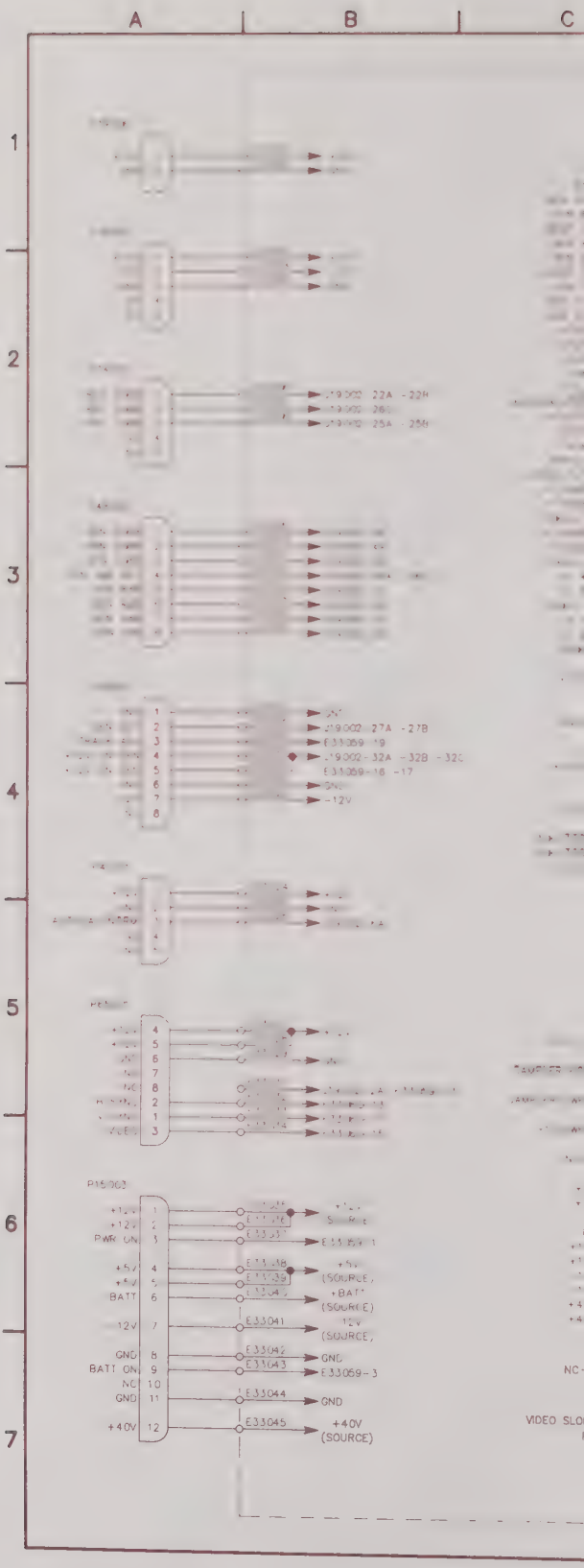
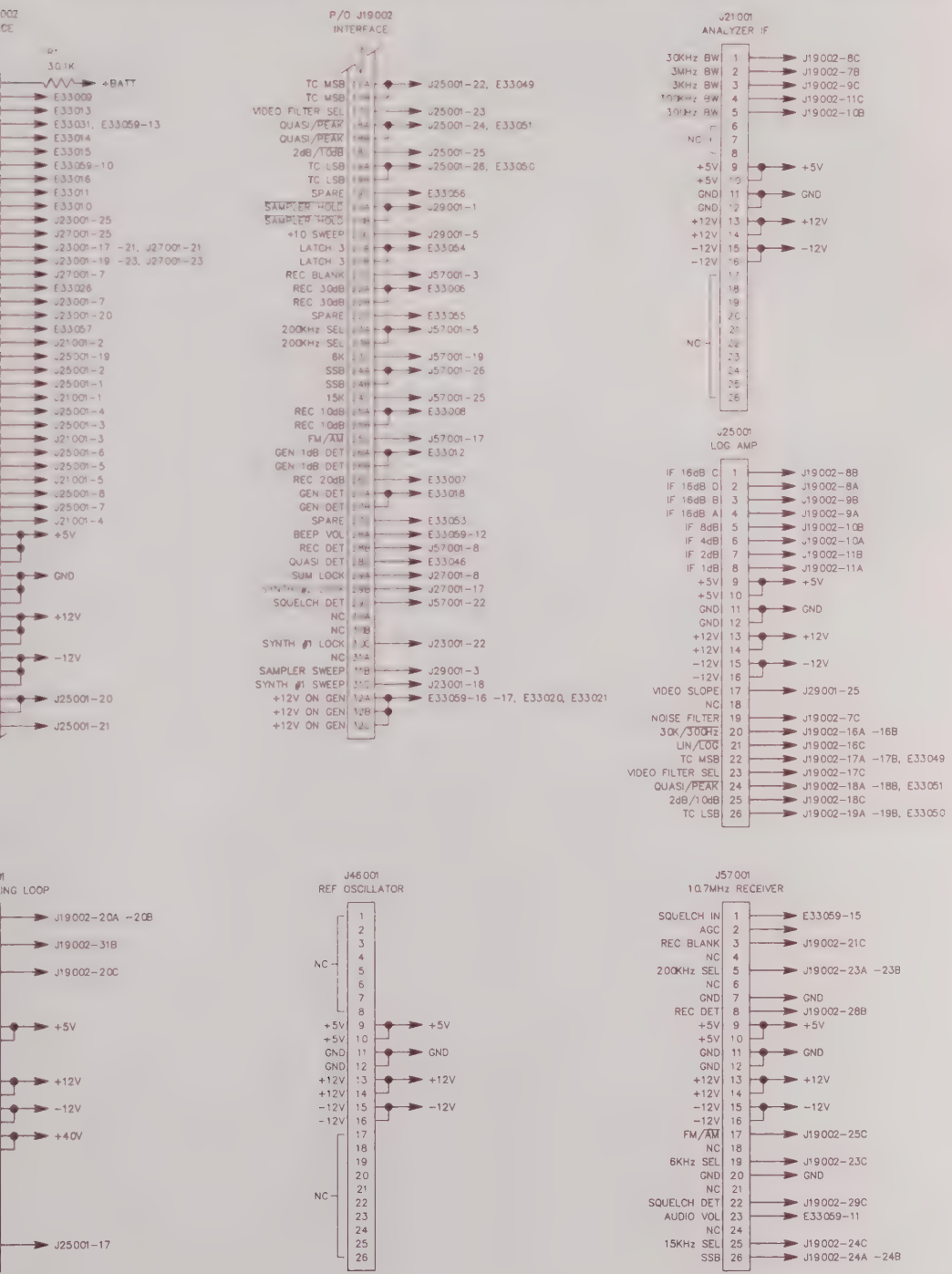
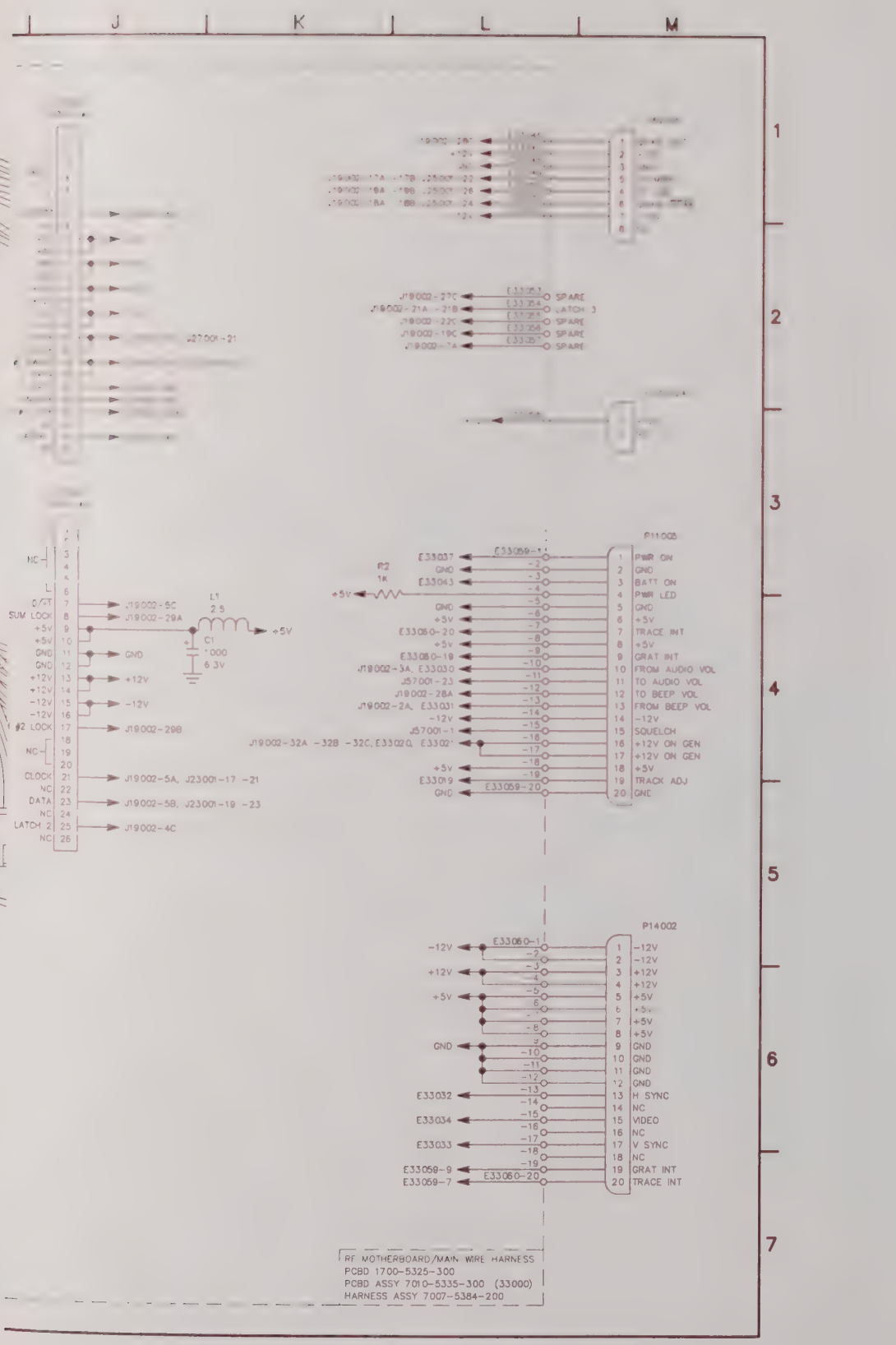


Figure 5-3 RF Motherboard with Wire Harness Assembly (Sheet 1 of 2) (0000-5315-300-C2)


A
B
C
1
2
3
4
5
6
7
-12V
+12V
PWR ON
+5V
+5V
BATT
12V
GND
BATT ON
NC
GND
+40V
E33041
E33042
E33043
E33044
E33045
GND
+40V
(SOURCE)
GND
VIDEO SLO

D E F G H


P/O J19002
INTERFACE
J21001
ANALYZER IF
J25001
LOG AMP
J46001
REF OSCILLATOR
J57001
10.7MHz RECEIVER
+BATT
TC MSB
TC LSB
VIDEO FILTER SEL
QUASI/PEAK
2dB/10dB
SPARE
SAMPLER HOLD
+10 SWEEP
LATCH 3
REC BLANK
REC 30dB
200KHz SEL
6K
SSB
15K
REC 10dB
FM/AM
GEN 1dB DET
REC 20dB
GEN DET
BEEP VOL
REC DET
QUASI DET
SUM LOCK
SQUELCH DET
SYNTH #1 LOCK
SAMPLER SWEEP
SYNTH #1 SWEEP
+12V ON GEN
NC
+5V
GND
+12V
-12V
+40V
30KHz BW
3MHz BW
3KHz BW
300Hz BW
AGC
AUDIO VOL
6KHz SEL
15KHz SEL
IF 16dB C
IF 16dB D
IF 16dB B
IF 16dB A
IF 8dB
IF 4dB
IF 2dB
IF 1dB
NOISE FILTER
30K/300Hz
LIN/LOG


J
K
L
M
1
2
3
4
5
6
7
J19002-27C
SPARE
J19002-21A, -21B
LATCH 3
J19002-22C
SPARE
J19002-19C
SPARE
J19002-17A
SPARE
J27001-21
P11002
PWR ON
GND
BATT ON
PWR LED
GND
+5V
TRACE INT
+5V
GRAT INT
FROM AUDIO VOL
TO AUDIO VOL
TO BEEP VOL
FROM BEEP VOL
-12V
SQUELCH
+12V ON GEN
+12V ON GEN
+5V
TRACK ADJ
GND
E33037
GND
E33043
R2
1K
+5V
GND
+5V
E33060-20
+5V
E33060-19
J19002-3A, E33030
J57001-23
J19002-28A
J19002-2A, E33031
-12V
J57001-1
J19002-32A -32B -32C, E33020, E33021
+5V
E33019
GND
E33059-20
NC
D/GT
SUM LOCK
+5V
GND
GND
+12V
+12V
-12V
-12V
#2 LOCK
NC
CLOCK
NC
DATA
NC
LATCH 2
NC
J19002-5C
J19002-29A
L1
2.5
C1
1000
6.3V
+5V
GND
+12V
-12V
J19002-29B
J19002-5A, J23001-17 -21
J19002-5B, J23001-19 -23
J19002-4C
P14002
-12V
-12V
+12V
+12V
+5V
+5V
+5V
+5V
GND
GND
GND
GND
E33032
H SYNC
NC
E33034
VIDEO
NC
E33033
V SYNC
NC
E33059-9
GRAT INT
E33059-7
TRACE INT
E33060-1
E33060-20
RF MOTHERBOARD/MAIN WIRE HARNESS
PCBD 1700-5325-300
PCBD ASSY 7010-5335-300 (33000)
HARNESS ASSY 7007-5384-200

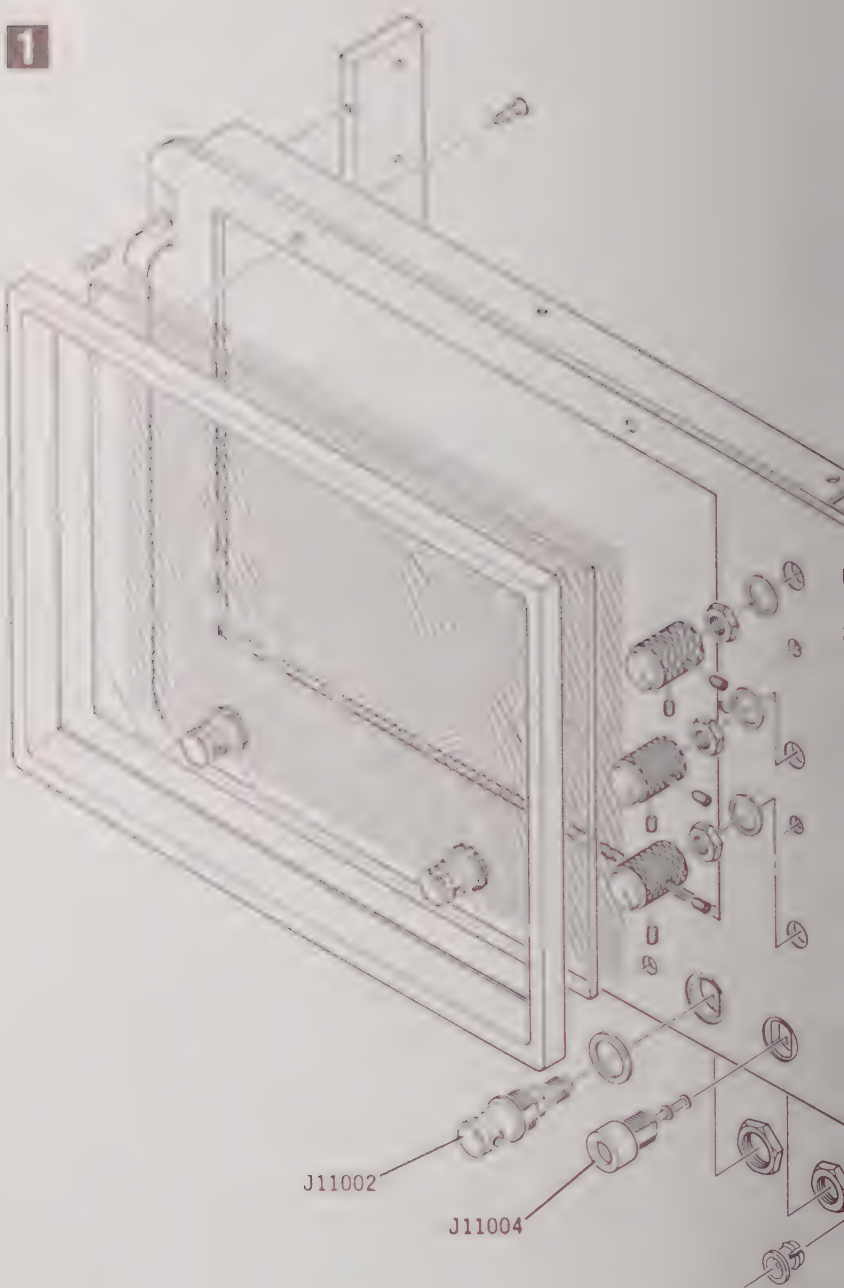
NOTES (UNLESS OTHERWISE STATED):

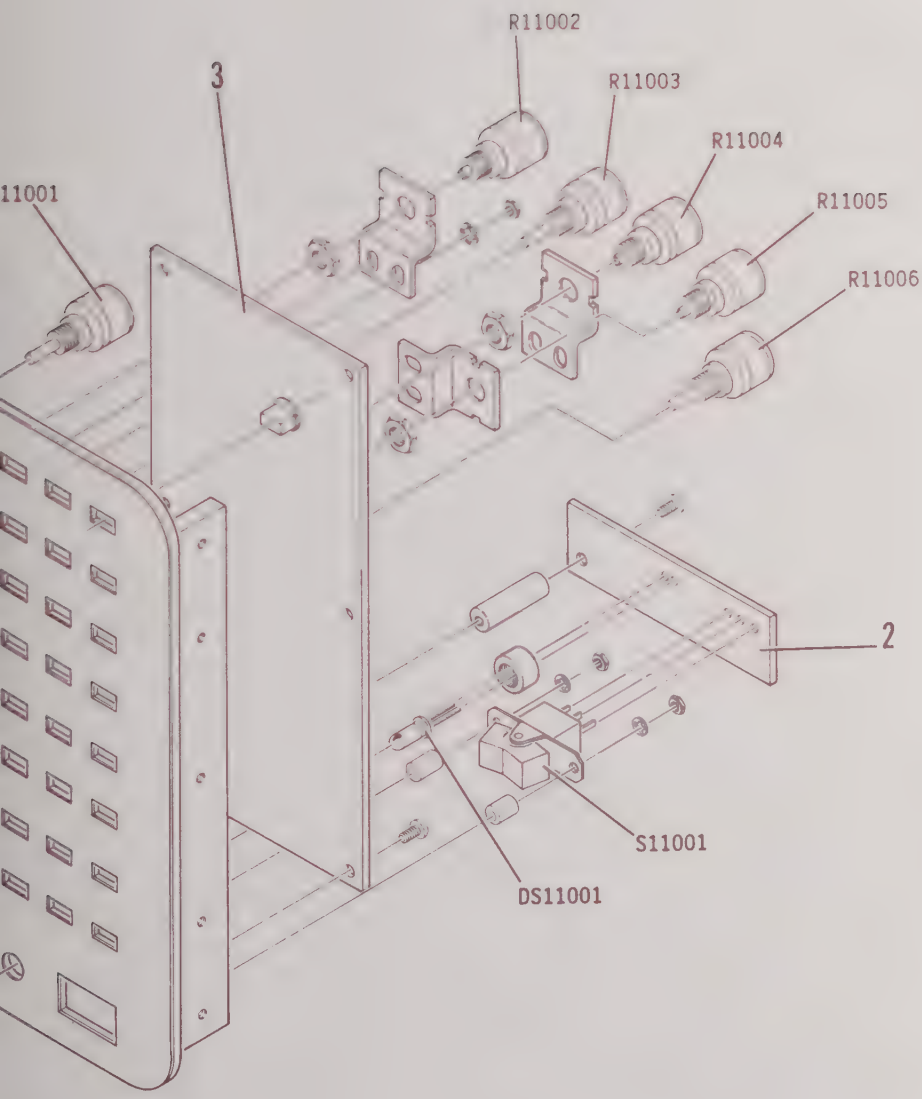
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 33000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

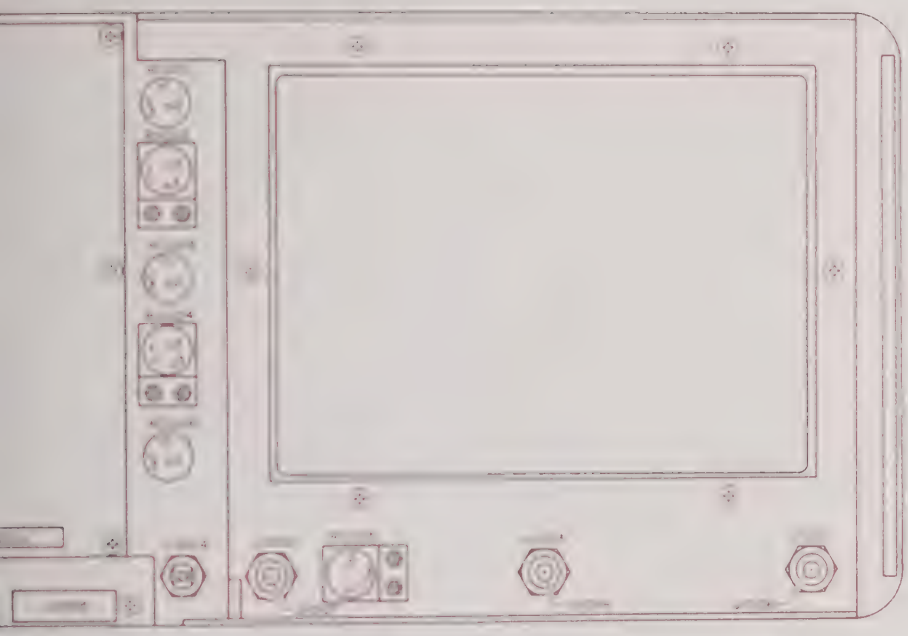
Figure 5-3 RF Motherboard with Wire Harness Assembly (Sheet 2 of 2) (0000-5315-300-C2)

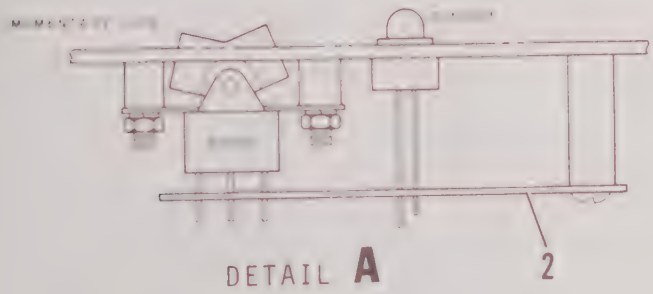

1
J11002
J11004

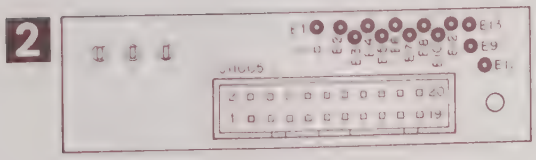

R11002
3
R11003
R11004
11001
R11005
R11006
2
S11001
DS11001

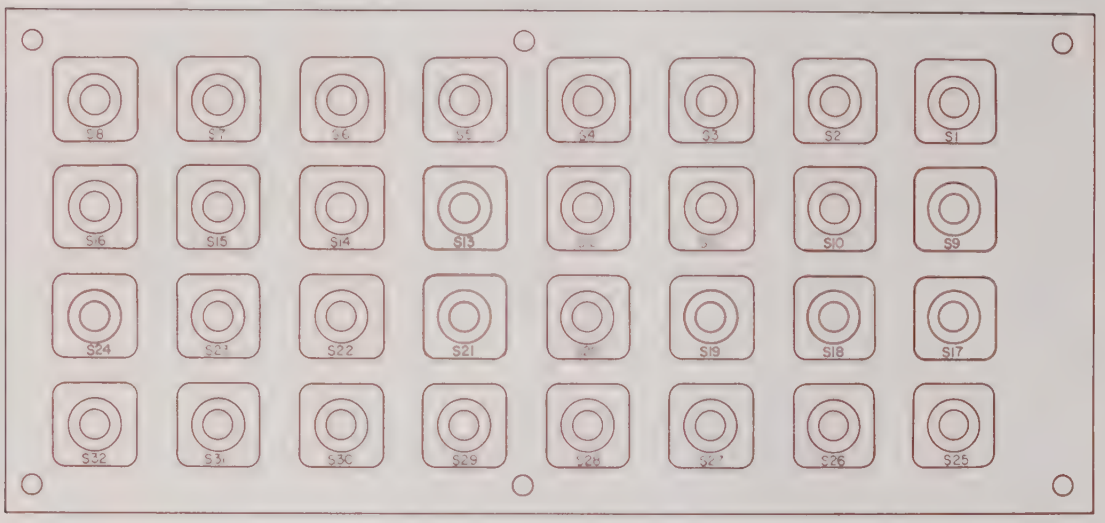
KEY

1. Front Panel Assy (7005-5342-800-F)
2. Front Panel Interface PC Bd Assy (1700-5325-400)
3. Keyboard PC Bd Assy (7010-5331-200-B1)

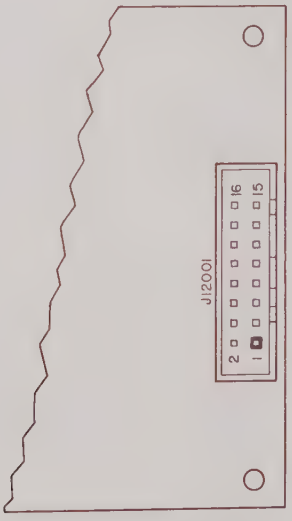



DETAIL A
2


2

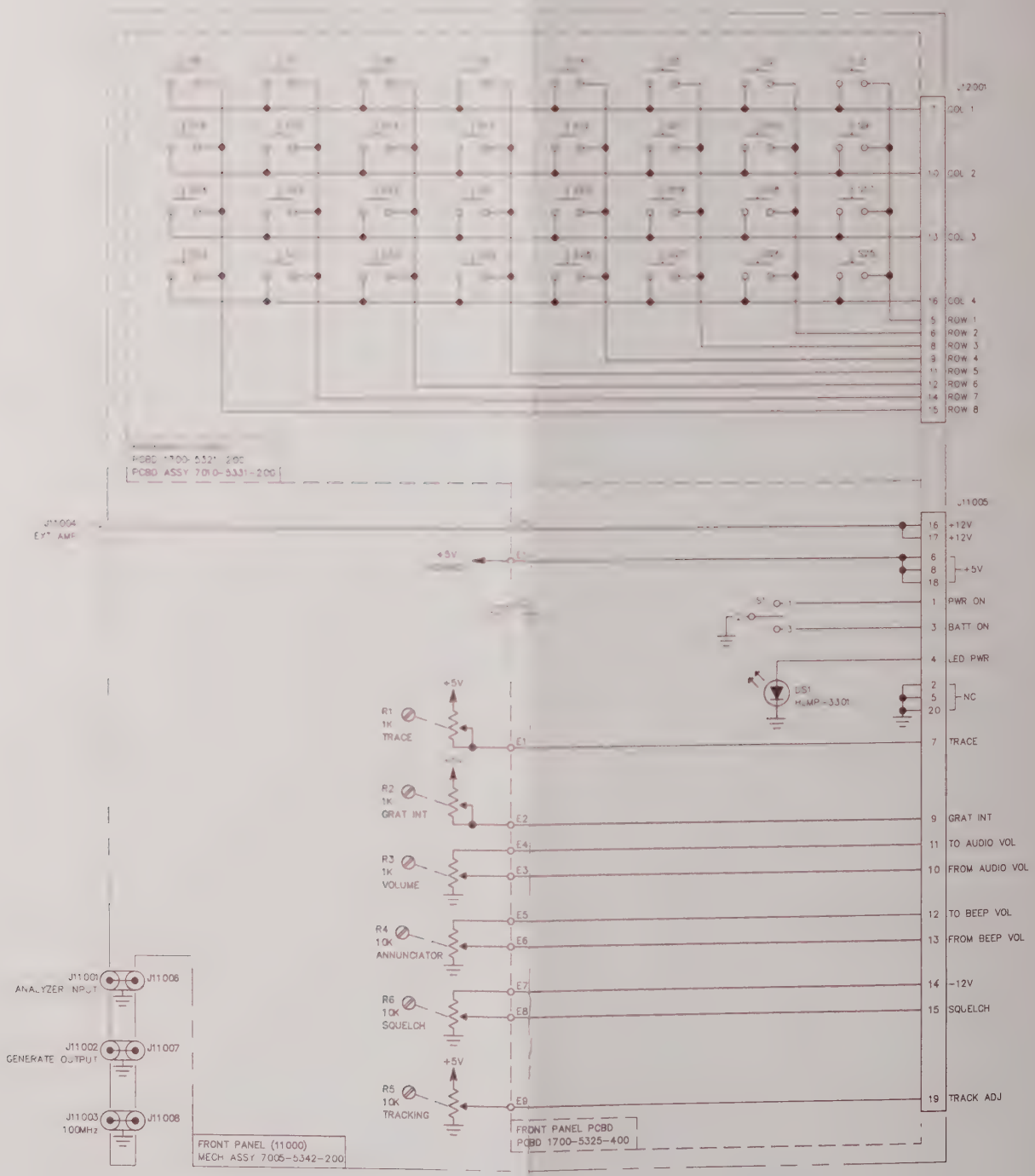


Top View



Bottom View

Figure 5-4 Front Panel & Keyboard Assembly
(Sheet 1 of 2)
(0000-5312-200-C & 0000-5311-200-B1)


J12001
COL 1
COL 2
COL 3
COL 4
ROW 1
ROW 2
ROW 3
ROW 4
ROW 5
ROW 6
ROW 7
ROW 8
PCBD 1700-5321-200
PCBD ASSY 7010-5331-200
J11004
EXT AMP
J11005
+12V
+12V
+5V
PWR ON
BATT ON
LED PWR
DS1
HLMP-3301
NC
TRACE
GRAT INT
TO AUDIO VOL
FROM AUDIO VOL
TO BEEP VOL
FROM BEEP VOL
-12V
SQUELCH
TRACK ADJ
R1
1K
TRACE
R2
1K
GRAT INT
R3
1K
VOLUME
R4
10K
ANNUNCIATOR
R6
10K
SQUELCH
R5
10K
TRACKING
+5V
J11001
ANALYZER INPUT
J11006
J11002
GENERATE OUTPUT
J11007
J11003
100MHz
J11008
FRONT PANEL (11000)
MECH ASSY 7005-5342-200
FRONT PANEL PCBD
PCBD 1700-5325-400

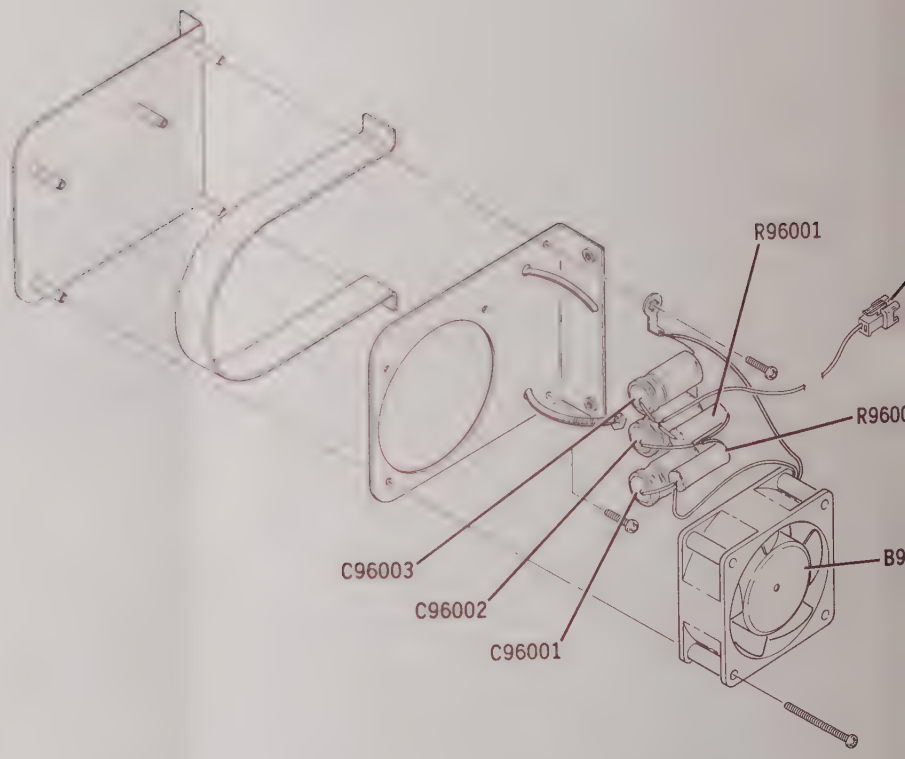
NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

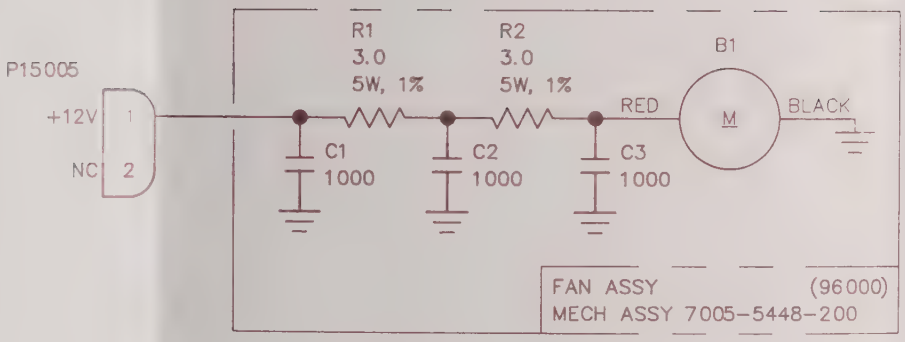
   A. KEYBOARD PCB ASSY - 12000
   B. FRONT PANEL PCB ASSY - 11000

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

Figure 5-4 Front Panel and Keyboard Assembly (Sheet 2 of 2) (0000-5312-200-C/0000-5311-200-B1)



MECH ASSY - FAN (7005-5448-200-E)


P15005
+12V
1
NC
2
R1
3.0
5W, 1%
R2
3.0
5W, 1%
B1
RED
M
BLACK
C1
1000
C2
1000
C3
1000
FAN ASSY
(96000)
MECH ASSY 7005-5448-200

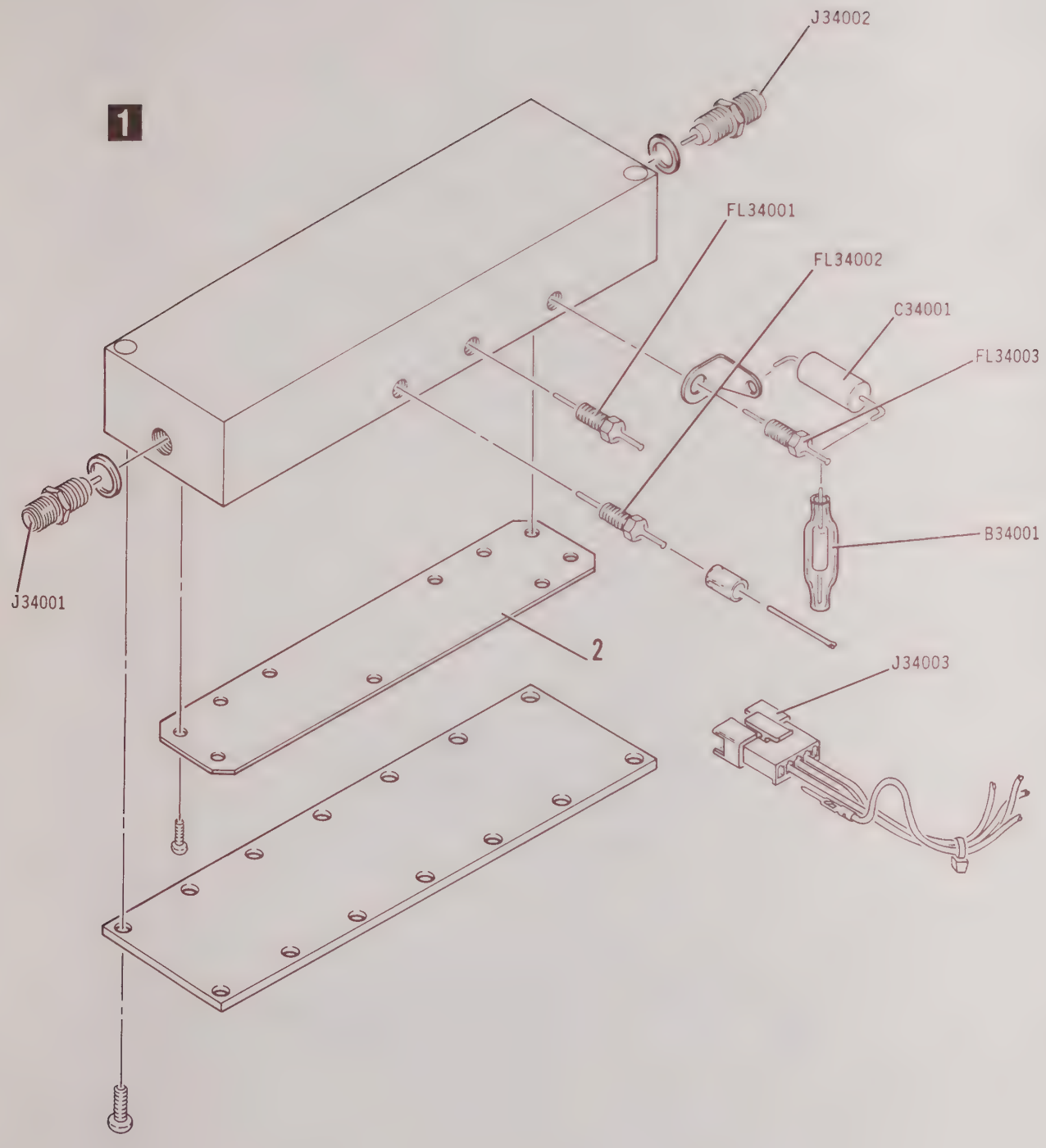
NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES 96000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

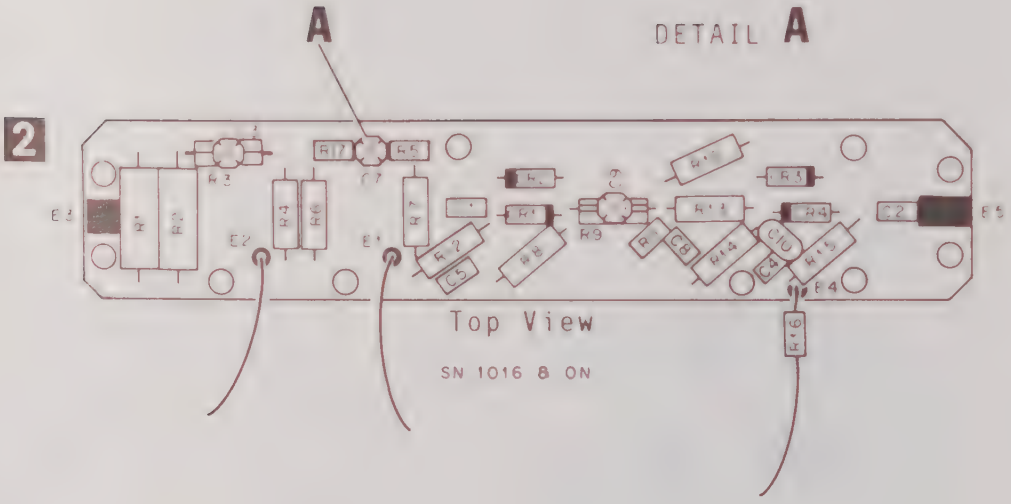
Figure 5-5 Fan Assembly (0000-5418-200-A)
Fan Assembly (7005-5448-200-E)

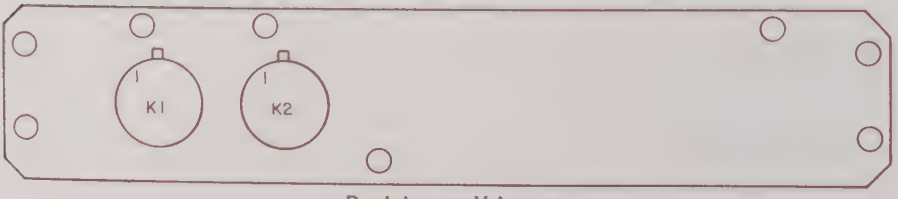

1
J34002
FL34001
FL34002
C34001
FL34003
B34001
J34001
2
J34003

KEY

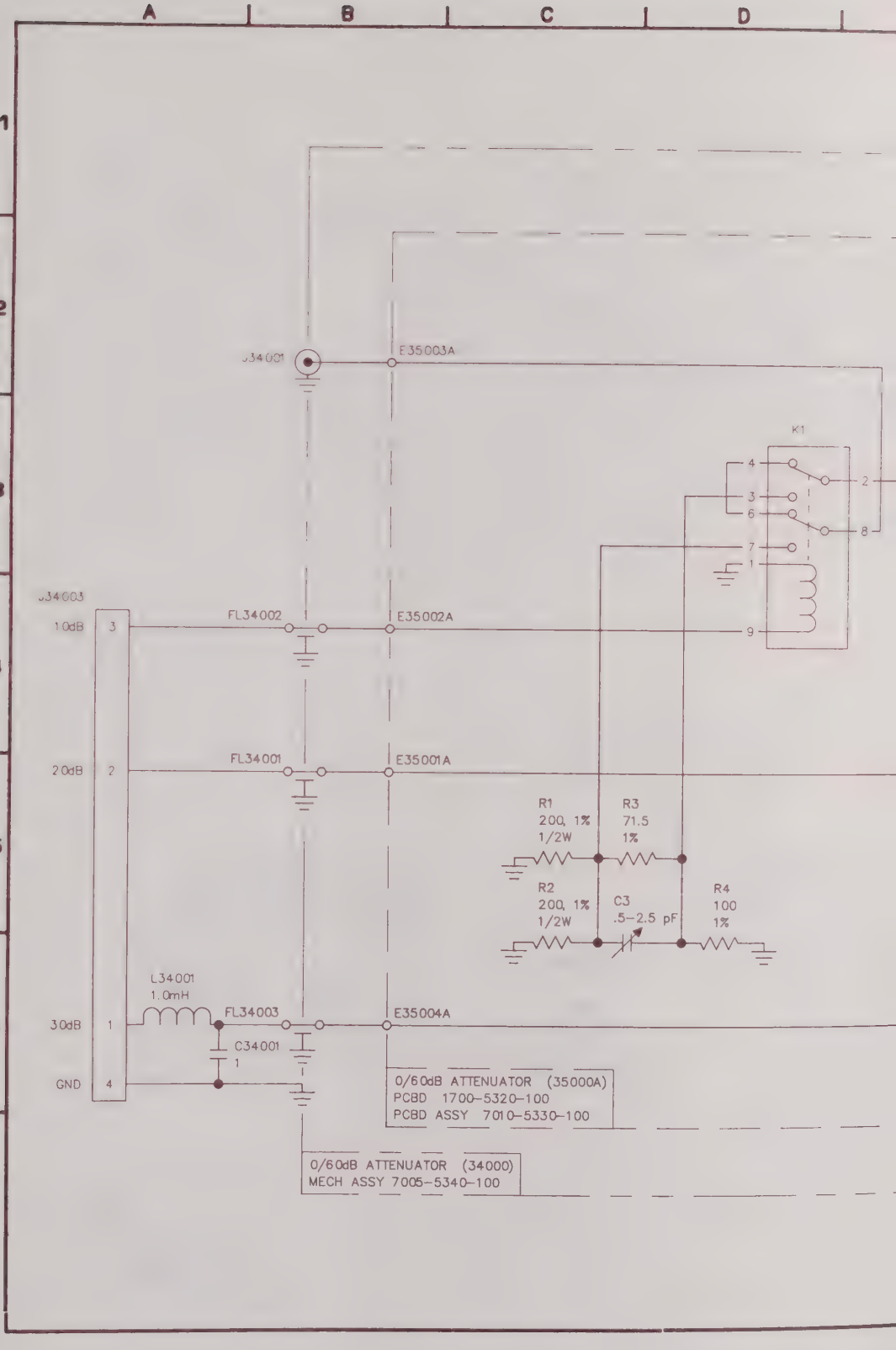
1. 0-60 dB Attenuator Assy (7005-5340-100-H)
2. 0-60 dB Attenuator PC Bd Assy (7010-5330-100-C4)

DETAIL A

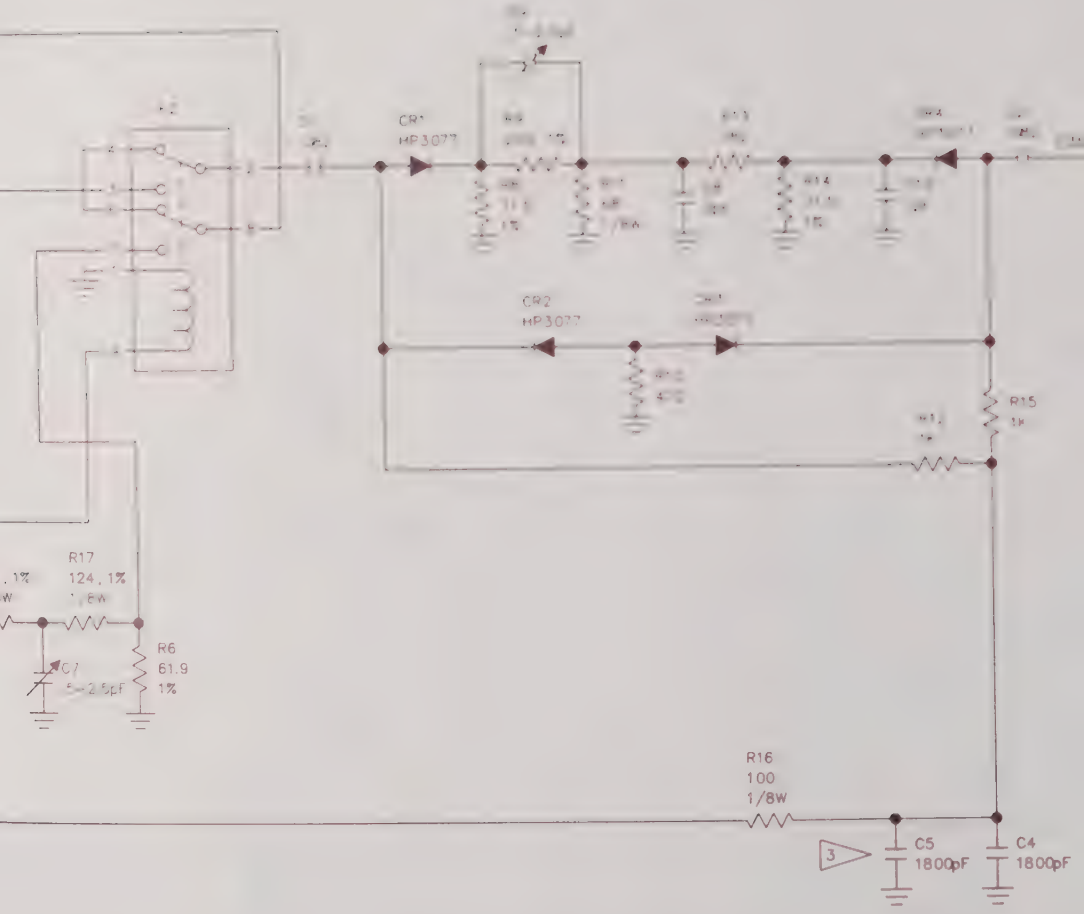


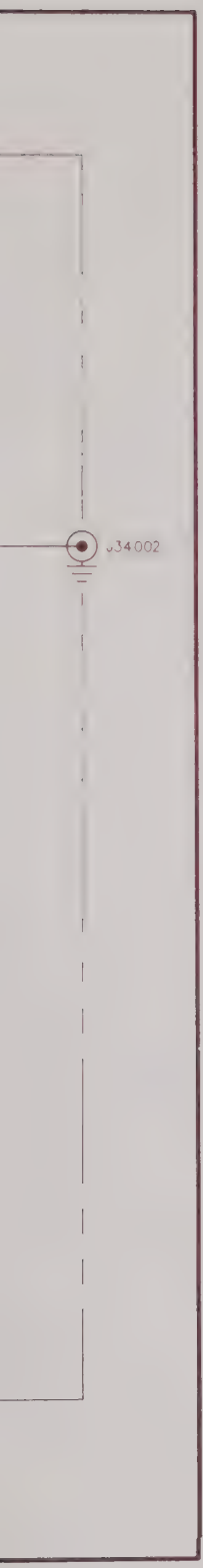


Bottom View


A
B
C
D
1
2
3
4
5
6
7
J34001
E35003A
K1
4
3
6
7
1
2
8
9
J34003
10dB
3
FL34002
E35002A
20dB
2
FL34001
E35001A
R1
200, 1%
1/2W
R3
71.5
1%
R2
200, 1%
1/2W
C3
.5-2.5 pF
R4
100
1%
L34001
1.0mH
30dB
1
FL34003
E35004A
C34001
1
GND
4
0/60dB ATTENUATOR (35000A)
PCBD 1700-5320-100
PCBD ASSY 7010-5330-100
0/60dB ATTENUATOR (34000)
MECH ASSY 7005-5340-100

F G H J


CR1
HP3077
CR2
HP3077
R15
1K
R17
124, 1%
R6
61.9
1%
C7
R16
100
1/8W
C5
1800pF
C4
1800pF
3



NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

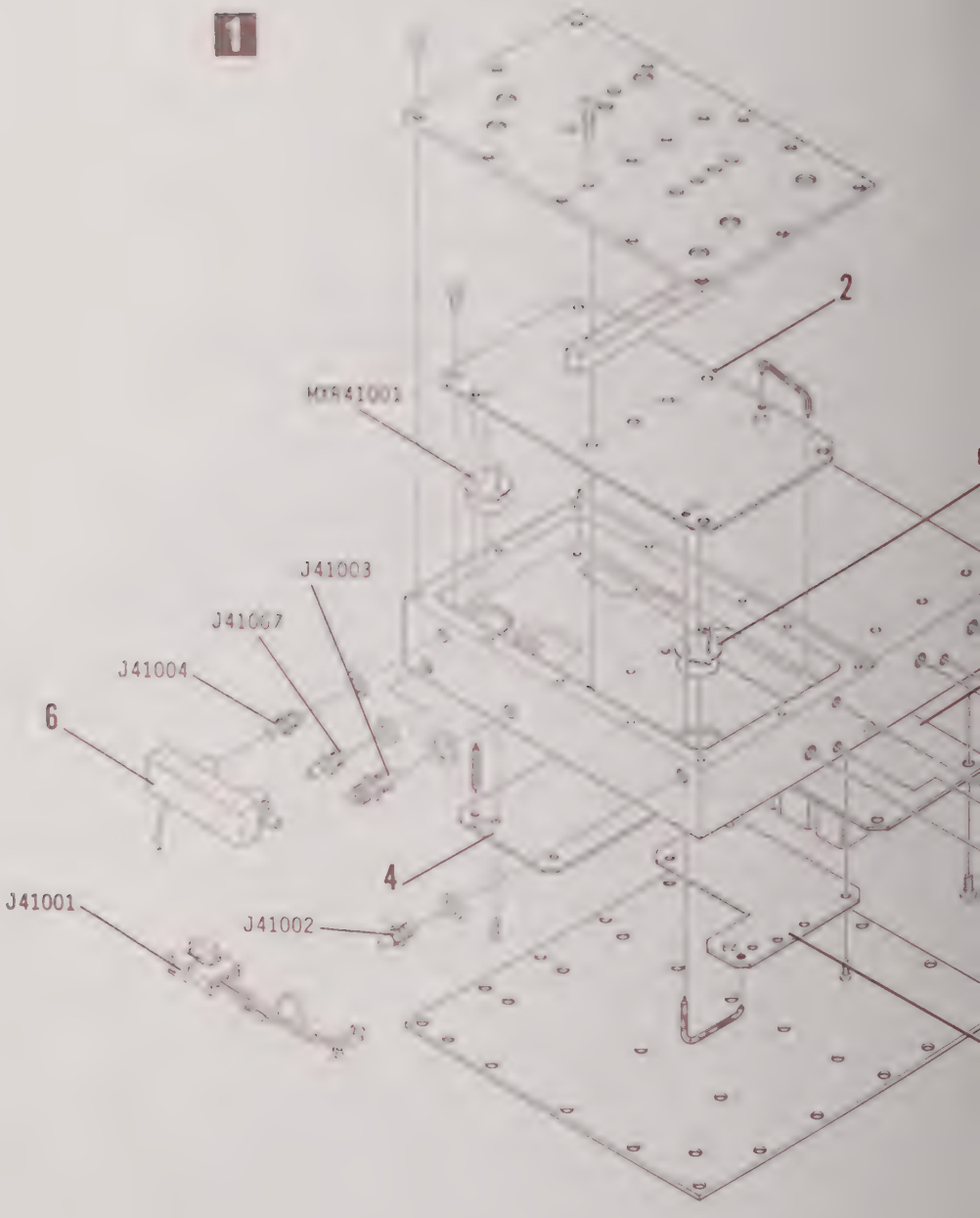
   A. MECH ASSY - 34000
   B. PC BD ASSY - 35000 (A)

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. C35005 IS INSTALLED AT MODULE LEVEL TO PREVENT BREAKAGE.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

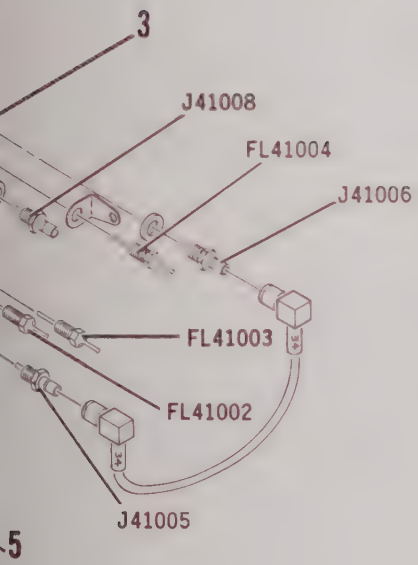
igure 5-6 0-60 dB Attenuator Assembly (0000-5310-201-M)


1
2
J41003
J41007
J41004
6
4
J41001
J41002

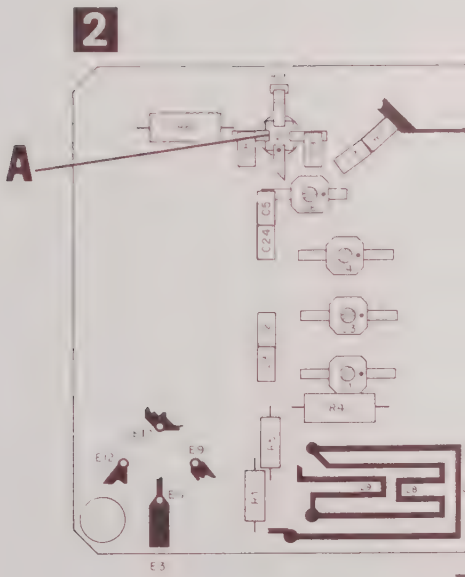
KEY

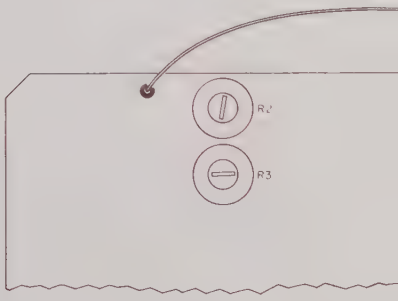
1. Recei
2. 1300
   (7010
3. 189.3
   (7010
4. 1000
   (Stri
5. Auto
6. Buffe
   (7010

002



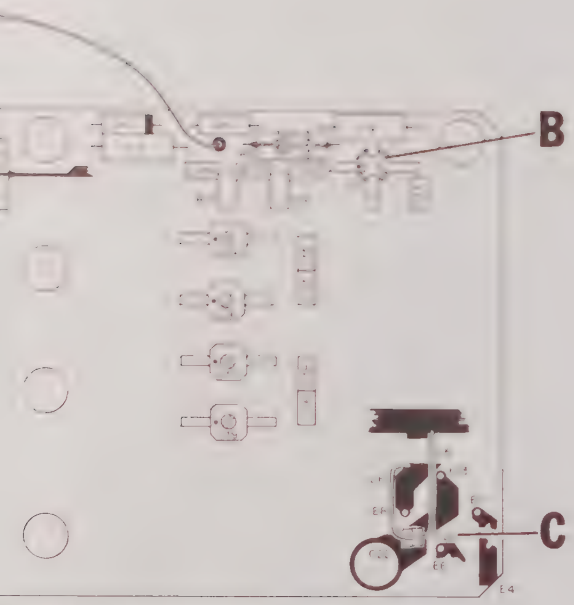
5



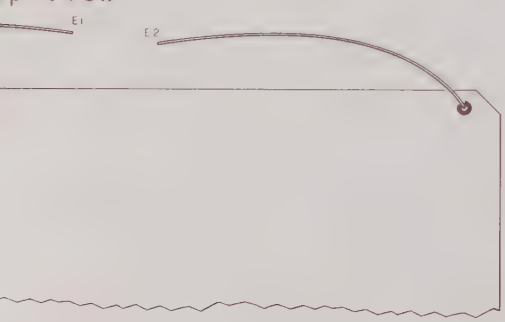


Bo

ve IF Assy (7005-5348-200-D)
MHz Receive IF PC Bd Assy
-5338-200-C7)
MHz Bandpass Filter PC Bd Assy
-5332-801-C5)
MHz Low-pass Filter PC Bd Assy
oline) (1700-5327-200-D2)
Cal PC Bd Assy (7010-5332-400-E4)
r Amp PC Bd Assy
-5335-501-C3)

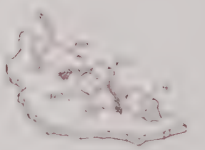


op View

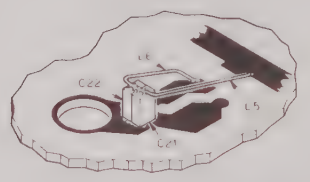


tom View

DETAIL **A**

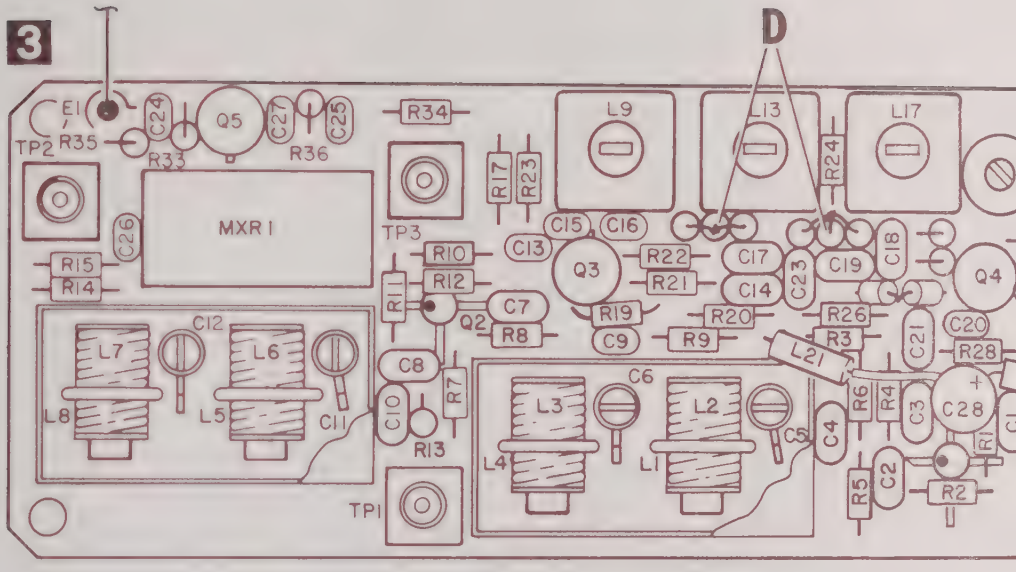


DETAIL **B**

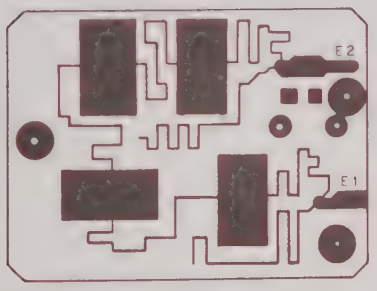


DETAIL **C**

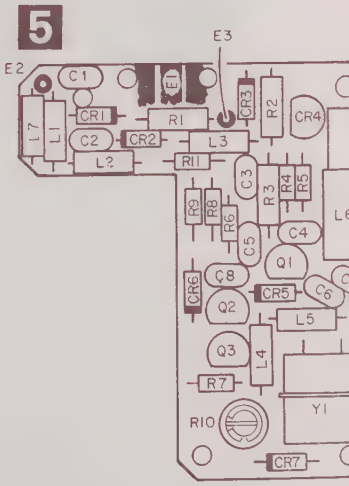
3

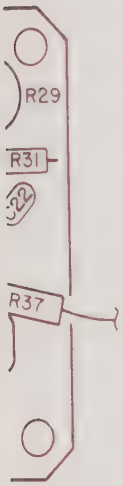

D
E1
TP2
R35
C24
Q5
C27
C25
R33
R36
R34
L9
L13
L17
R24
R17
R23
MXR1
C26
TP3
C15
C16
C13
R10
R22
C17
C18
R15
R14
R12
R11
Q3
R21
C14
C23
C19
Q4
C7
Q2
R8
R19
R20
R26
C12
L7
L6
C9
R9
R3
C21
C20
L21
R28
C8
R7
C6
L3
L2
R6
R4
C3
C28
L8
L5
C11
C10
R13
C5
C4
R1
L4
L1
R5
C2
R2
TP1

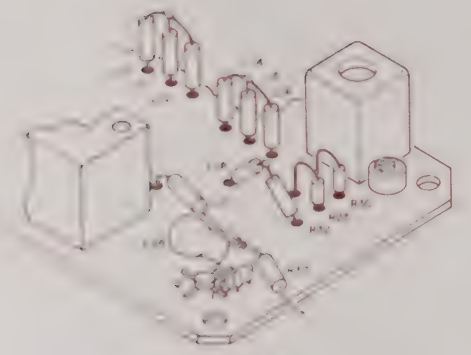
4


E2
E1

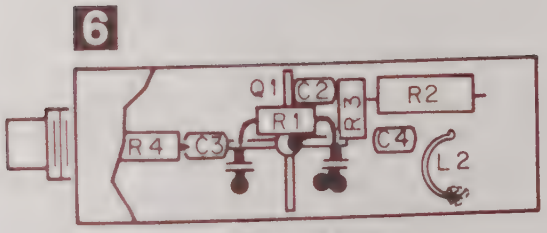
5


E3
E2
C1
E1
CR3
R2
CR4
L7
L1
CR1
R1
C2
CR2
L3
L2
R11
C3
R3
R4
R5
R9
R8
R6
C5
C4
Q1
CR6
C8
CR5
C6
Q2
L5
Q3
L4
R7
Y1
R10
CR7

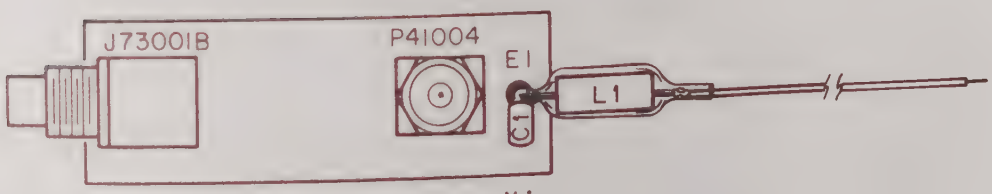




DETAIL **D**

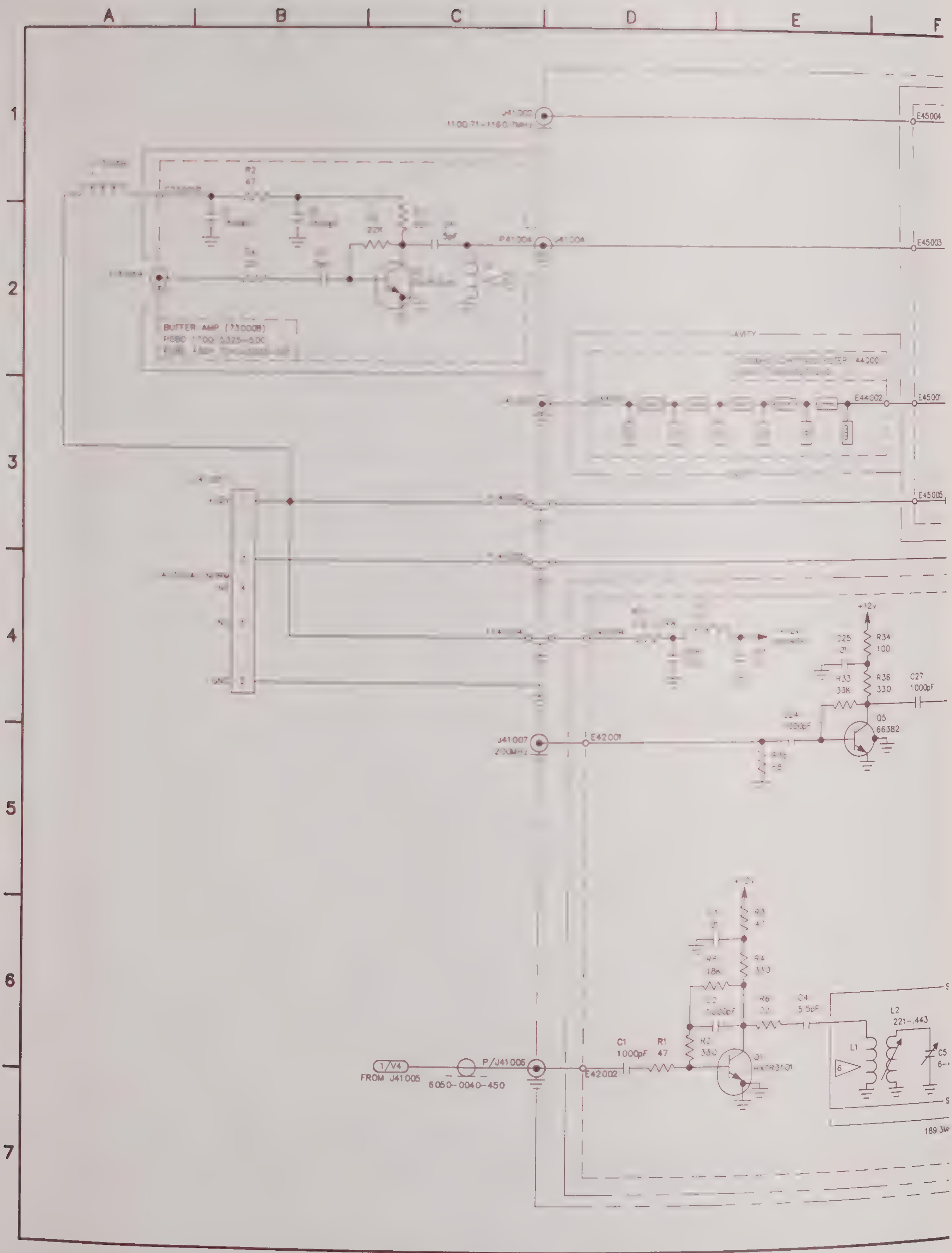


Top View

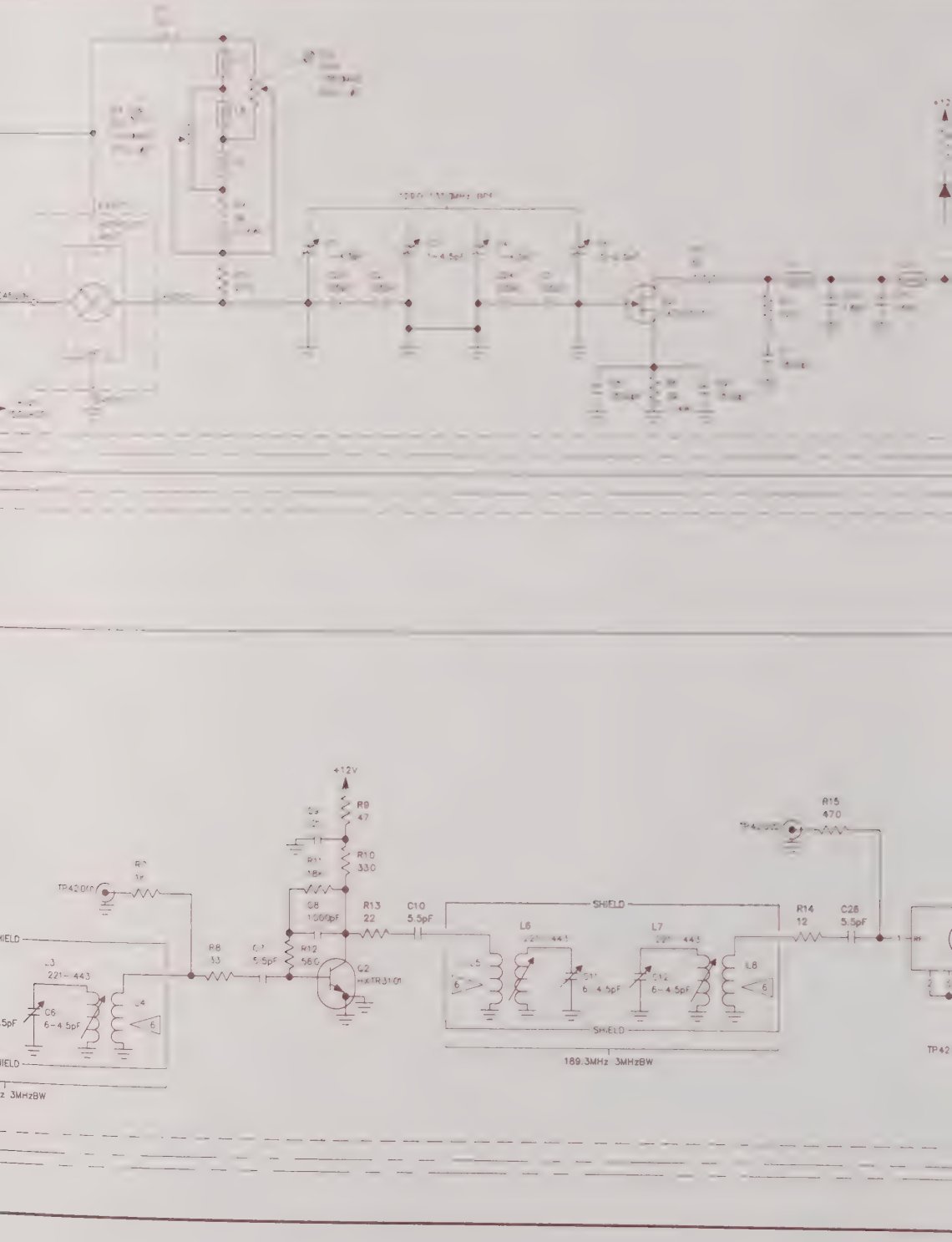


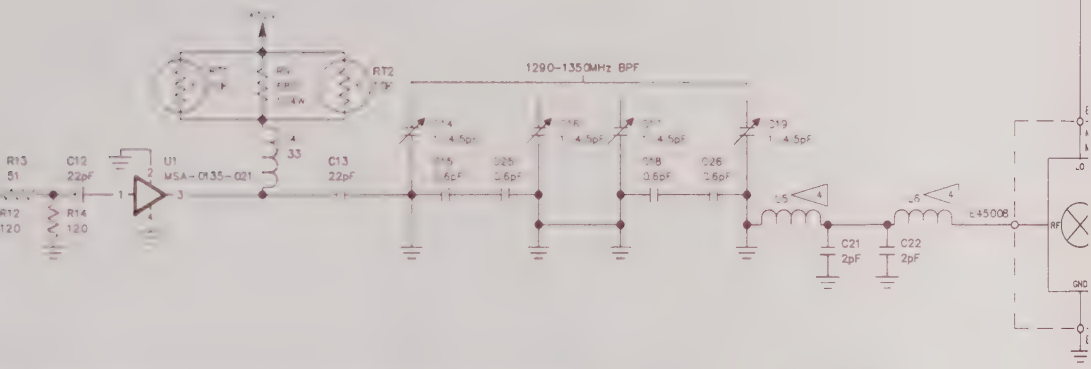
Bottom View

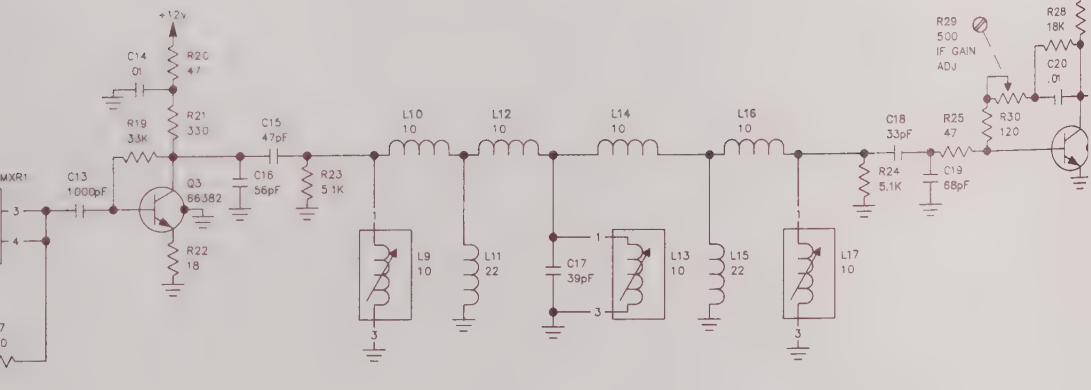
Figure 5-7 Receive IF Assembly (Sheet 1 of 2)
(0000-5318-200-L)

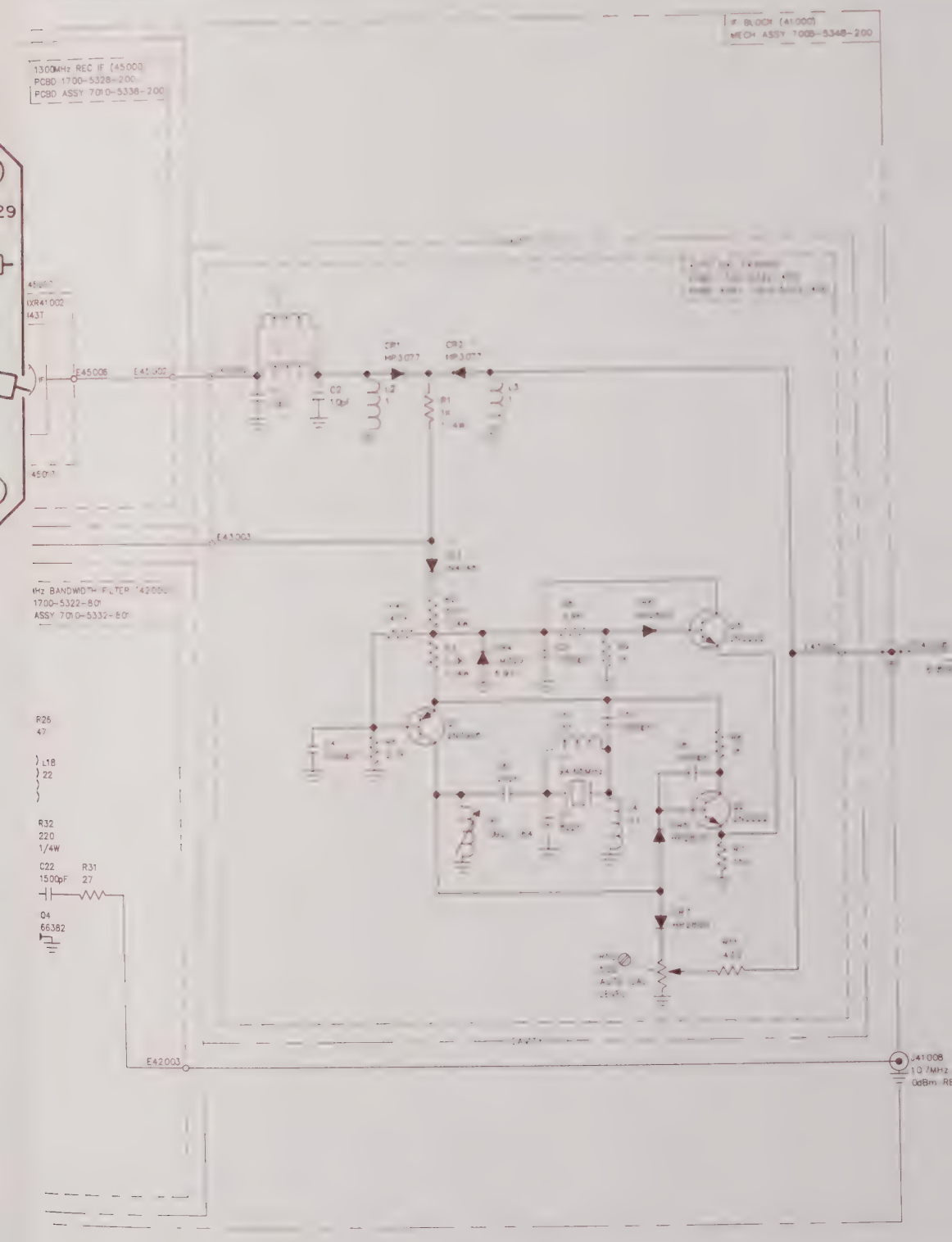


A
B
C
D
E
F
1
2
3
4
5
6
7
J41002
E45004
R2
47
22K
P41004
J41004
E45003
BUFFER AMP (73000B)
E44002
E45001
E45005
+12v
C25
.01
R34
100
R33
33K
R36
330
C27
1000pF
Q5
66382
J41007
200MHz
E42001
18K
R4
330
1000pF
R6
22
C4
5.5pF
L2
221-443
L1
C5
C1
1000pF
R1
47
R2
330
1/V4
FROM J41005
P/J41006
6050-0040-450
E42002


G
H
J
K
L
+12V
R9
47
R10
330
R13
22
C10
5.5pF
R12
560
Q2
HXTR3101
R8
33
C8
1000pF
TP42001
L3
221-443
C6
6-4.5pF
L4
SHIELD
L6
L7
L8
C11
6-4.5pF
C12
6-4.5pF
R14
12
C26
5.5pF
R15
470
189.3MHz 3MHzBW
3MHzBW


RT2
1290-1350MHz BPF
R13
51
C12
22pF
U1
MSA-0135-021
R12
120
R14
120
33
C13
22pF
C21
2pF
C22
2pF
RF
GND


+12v
C14
01
R20
47
R21
330
R19
33K
C15
47pF
C16
56pF
R23
5.1K
C13
1000pF
Q3
66382
R22
18
L10
10
L12
10
L14
10
L16
10
L9
10
L11
22
C17
39pF
L13
10
L15
22
L17
10
C18
33pF
R24
5.1K
R25
47
C19
68pF
R29
500
IF GAIN
ADJ
R30
120
R28
18K
C20
.01
C21
01


S
T
U
V
W
IF BLOCK (41000)
MECH ASSY 7008-5348-200
1300MHz REC IF (45000
PCBD 1700-5328-200
PCBD ASSY 7010-5338-200
E45006
E43003
E42003
CR1
HP3077
CR2
HP3077
C2
10pF
L2
1
R1
1K
L3
1
R26
47
L18
22
R32
220
1/4W
C22
1500pF
R31
27
Q4
66382
J41008
10.7MHz
0dBm

X

(1/A7)
TO J41006

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. 7005-5348-200 (MECH) - 41000
   B. 7010-5332-801 (189.3 MHz BANDWIDTH FILTER) - 42000
   C. 7010-5332-400 (AUTO CAL) - 43000
   D. 1700-5327-200 (1000 MHz LOWPASS FILTER) - 44000
   E. 7010-5338-200 (1300 MHz RECEIVE IF) - 45000
   F. 7010-5335-501 (BUFFER AMP) - 73000B

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (µF).

4. L4505 & L4506 ARE MADE OF A .9" LENGTH OF 22 GA. BUS WIRE.

5. L73002B IS MADE OF A .5" LOOP OF 22 GA. BUS WIRE.

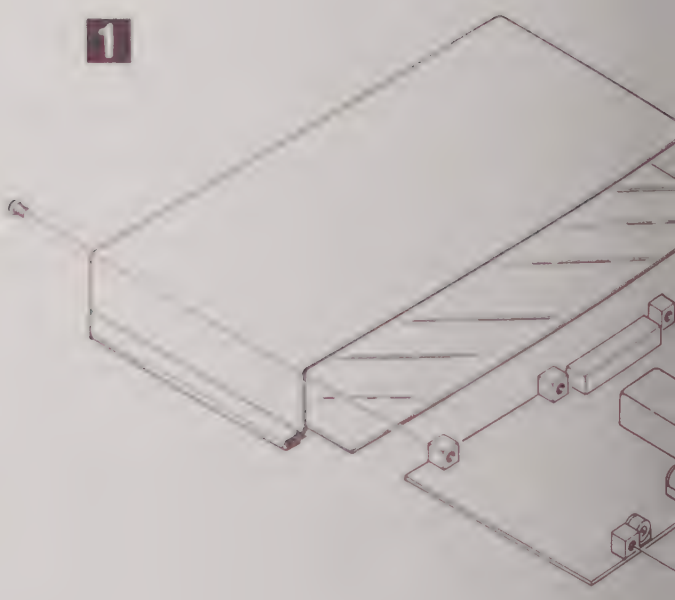
6. L42001, L42004, L42005 & L42008 ARE MADE OF 26 GA. BUS WIRE WITH SLEEVING.

7. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (µH).

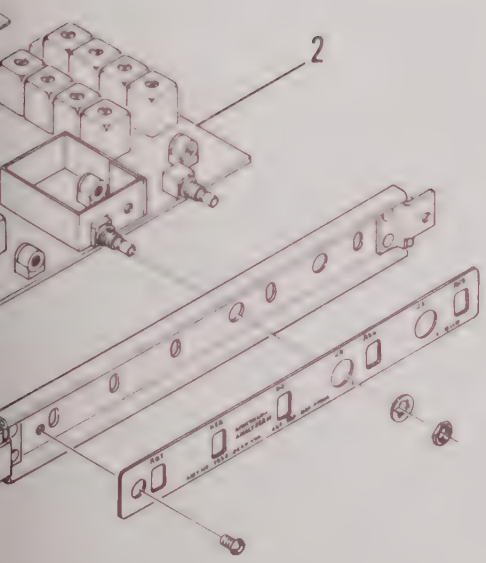
Figure 5-7 Receive IF Assembly (Sheet 2 of 2) (0000-5318-200-L)

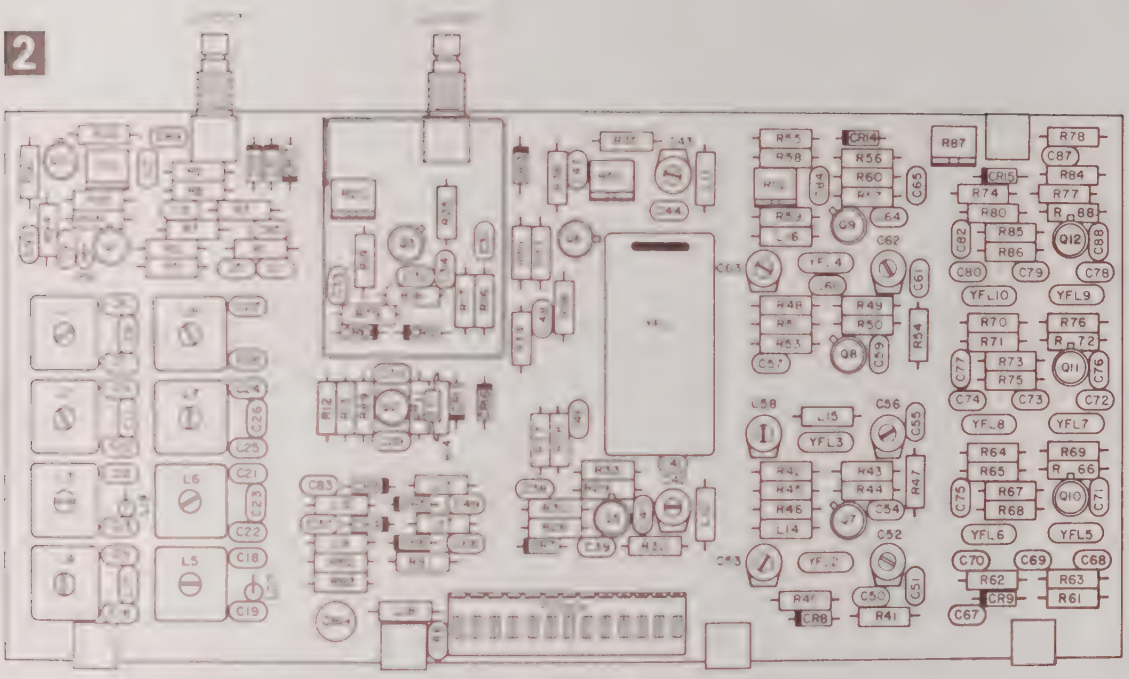
KEY:

1. Analyzer IF Assy (70
2. Analyzer IF PC Bd As
   (7010-5339-400-B)



5349-400-A)





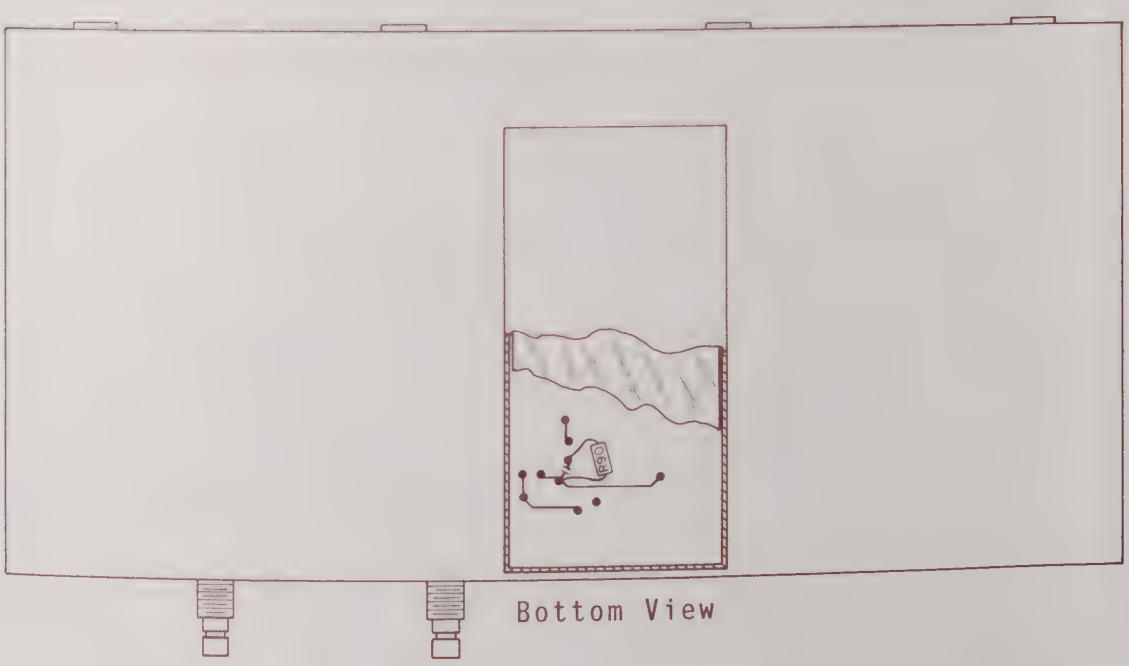
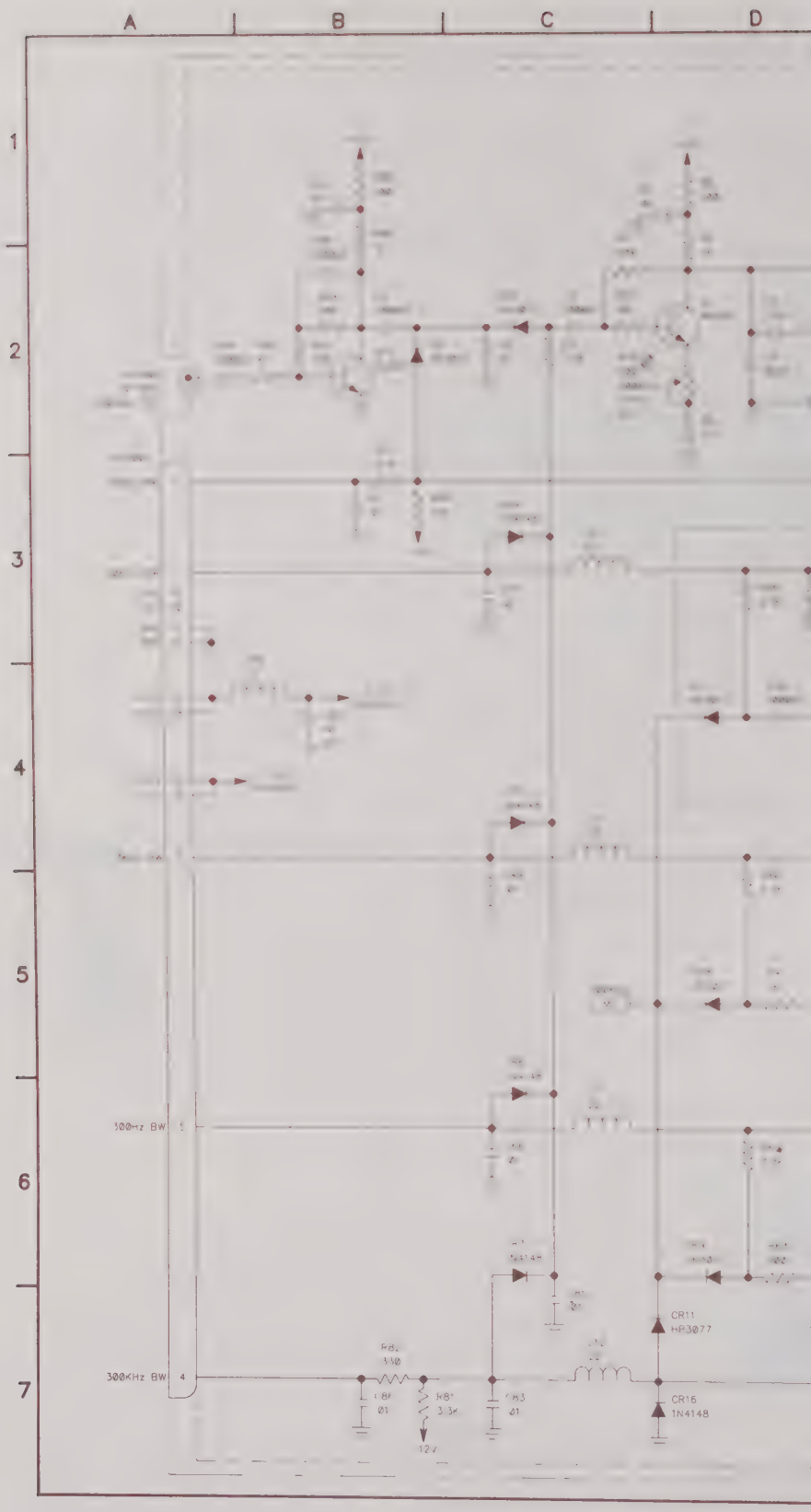
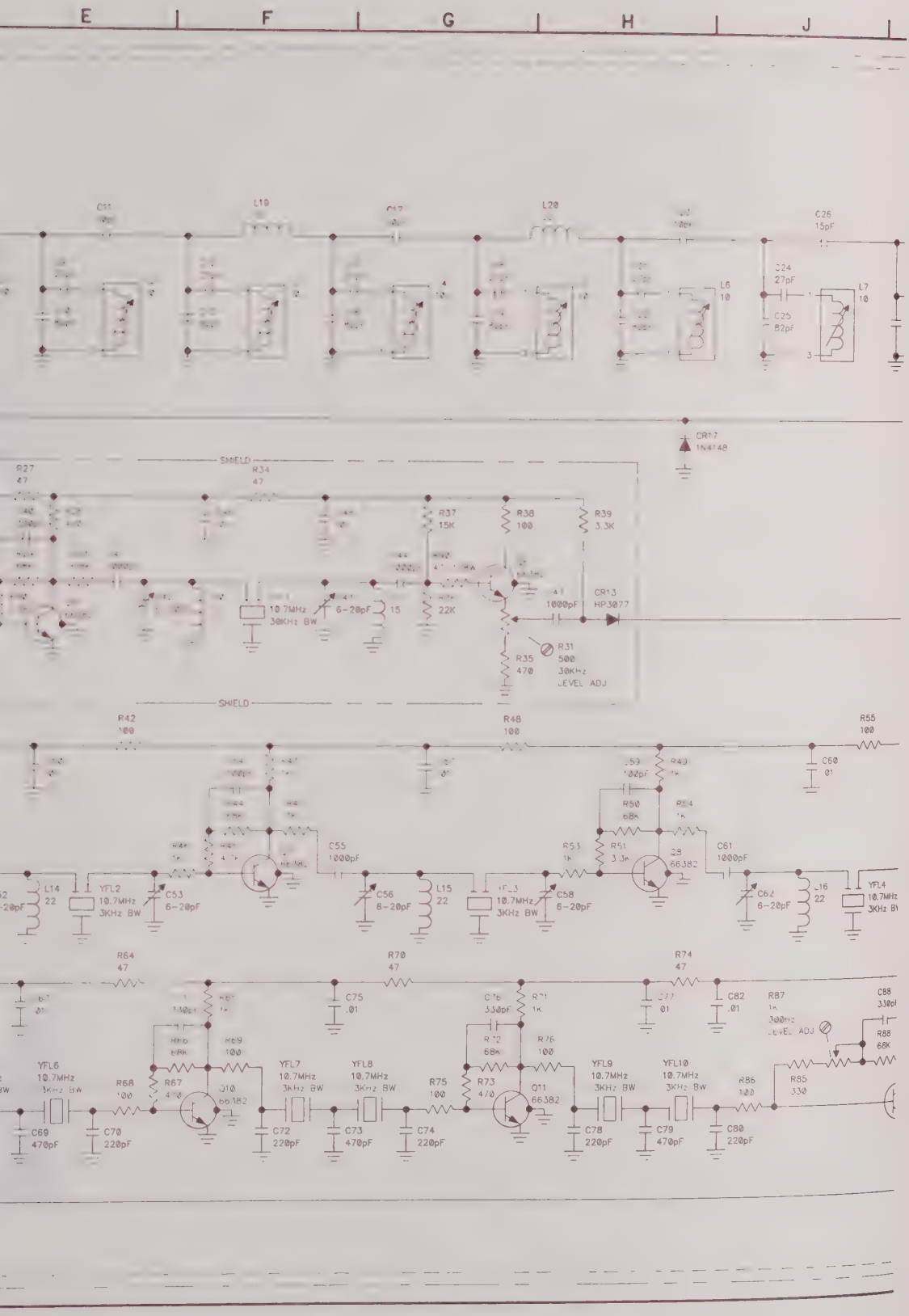
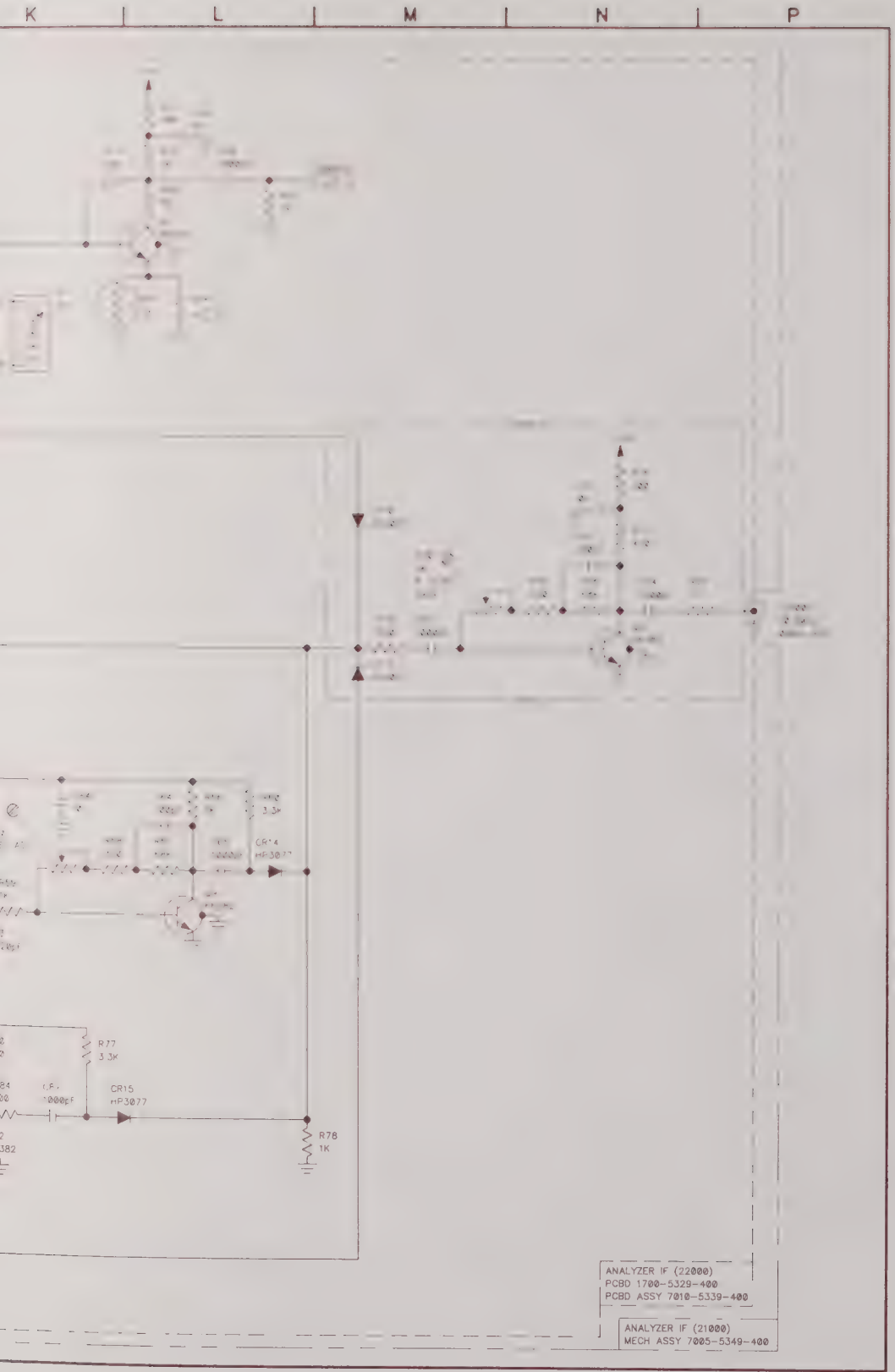


Figure 5-8 Analyzer IF Assembly (Sheet 1 of 2)
(0000-5319-100-B3)


A
B
C
D
1
2
3
4
5
6
7
300Hz BW
300KHz BW
CR11
HP3077
CR16
1N4148
12V


E
F
G
H
J
C11
L19
C17
L20
C26
15pF
C24
27pF
C25
82pF
L6
10
L7
10
CR17
1N4148
SHIELD
R27
47
R34
47
R37
15K
R38
100
R39
3.3K
10.7MHz
30KHz BW
6-20pF
15
22K
1000pF
CR13
HP3077
R35
470
R31
500
30KHz
LEVEL ADJ
SHIELD
R42
100
R48
100
R55
100
C60
01
R50
68K
R51
3.3K
Q8
66382
C61
1000pF
C55
1000pF
L14
22
YFL2
10.7MHz
3KHz BW
C53
6-20pF
C56
6-20pF
L15
22
10.7MHz
3KHz BW
C58
6-20pF
C62
6-20pF
L16
22
YFL4
10.7MHz
3KHz BW
R64
47
R70
47
R74
47
C75
.01
C82
.01
R87
1K
300Hz
LEVEL ADJ
C88
330pF
R88
68K
YFL6
10.7MHz
3KHz BW
R68
100
R67
470
Q10
66382
YFL7
10.7MHz
3KHz BW
YFL8
10.7MHz
3KHz BW
R75
100
R73
470
Q11
66382
YFL9
10.7MHz
3KHz BW
YFL10
10.7MHz
3KHz BW
R86
100
R85
330
C69
470pF
C70
220pF
C72
220pF
C73
470pF
C74
220pF
C78
220pF
C79
470pF
C80
220pF


K
L
M
N
P
R77
3.3K
CR15
HP3077
R78
1K
ANALYZER IF (22000)
PCBD 1700-5329-400
PCBD ASSY 7010-5339-400
ANALYZER IF (21000)
MECH ASSY 7005-5349-400

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 21000
   B. PC BD ASSY - 22000

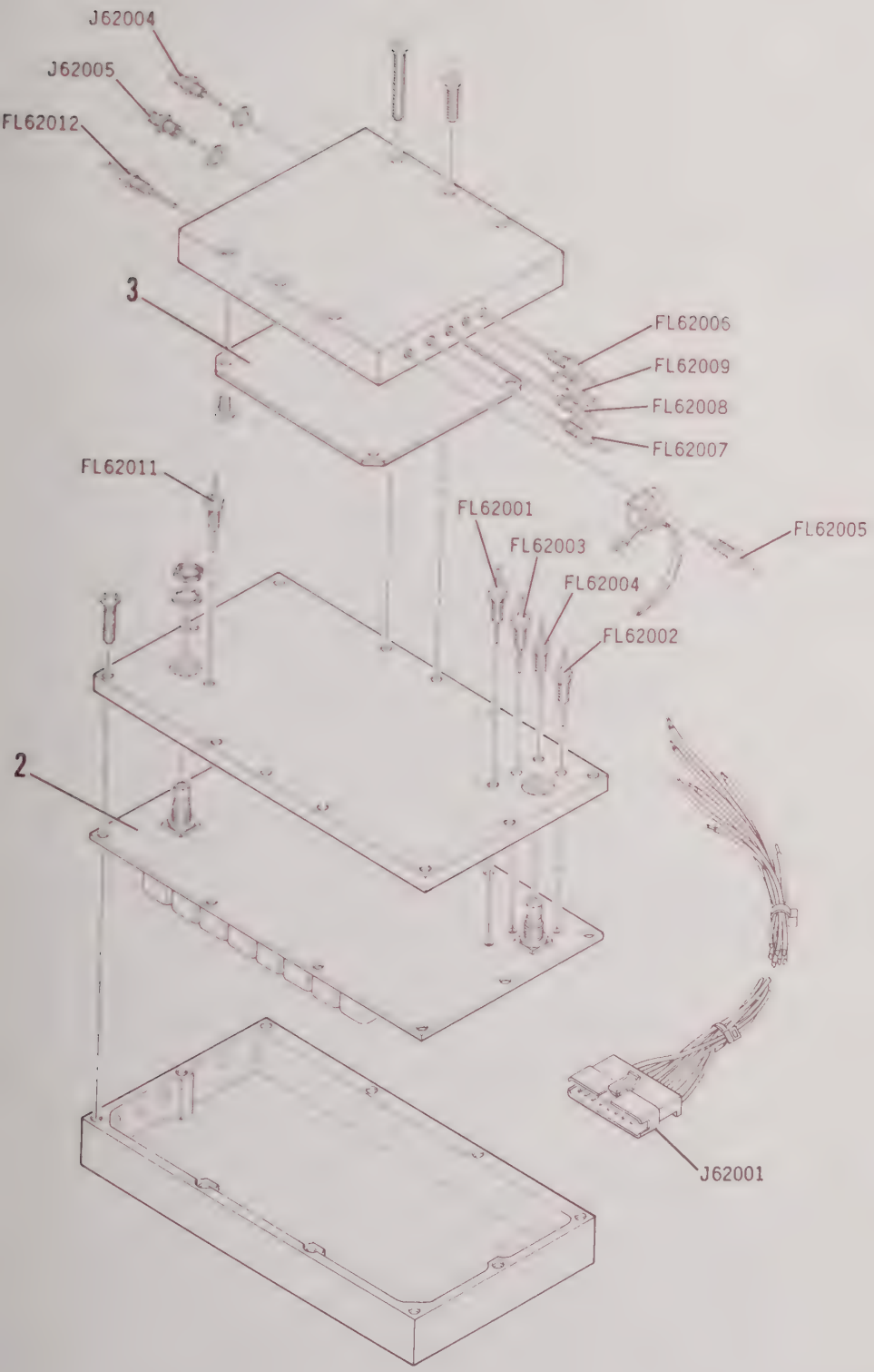
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. R22014 IS SELECT AT TEST (S.A.T.) NOMINAL VALUE = 120Ω; RANGE = 68-120Ω.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

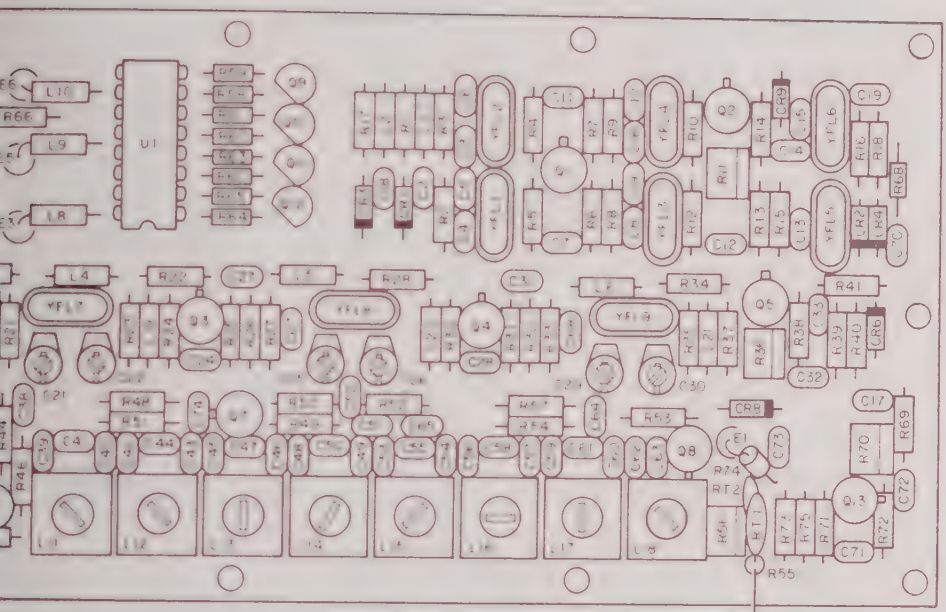
Figure 5-8 Analyzer IF Assembly (Sheet 2 of 2) (0000-5319-100-B3)


J62004
J62005
FL62012
3
FL62006
FL62009
FL62008
FL62007
FL62011
FL62001
FL62003
FL62004
FL62002
FL62005
2
J62001

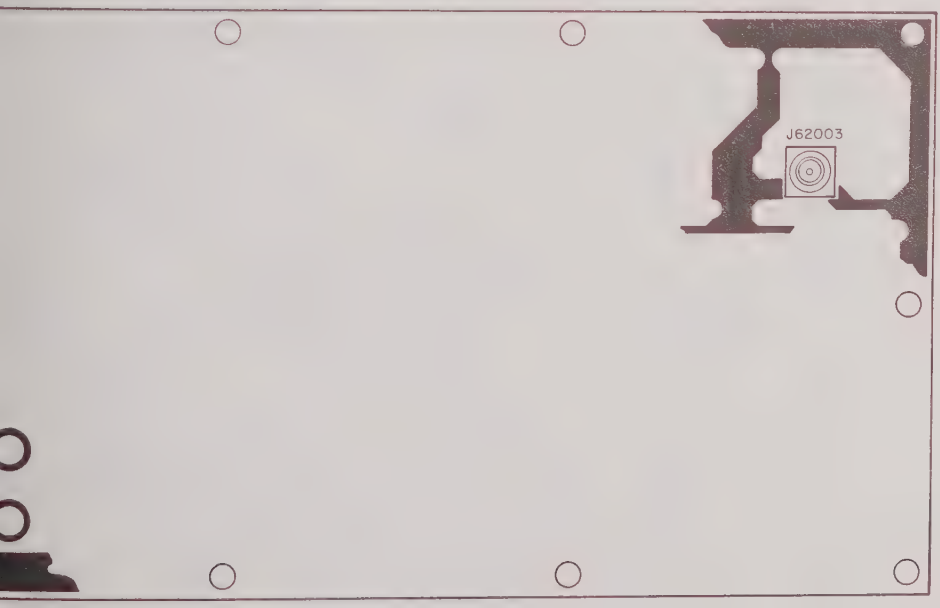
KEY:

1. Quasi-peak Assy (7005-5348-000-D)
2. Quasi-peak Filter PC Bd Assy (7010-5338-000-C2)
3. Quasi-peak Detector PC Bd Assy (7010-5338-300-D2)

DETAIL **A**



Top View



Bottom View

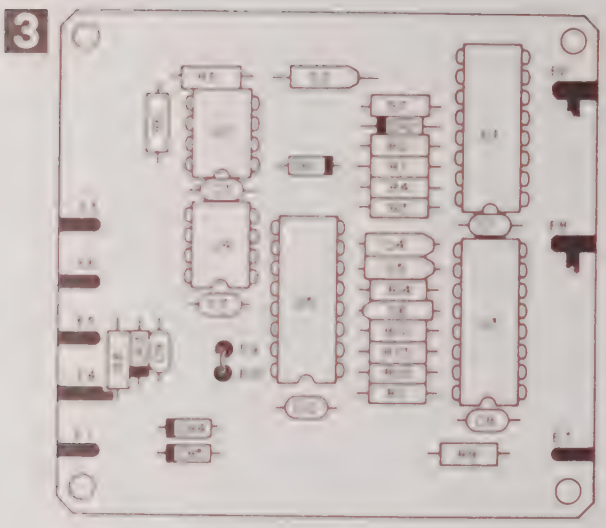
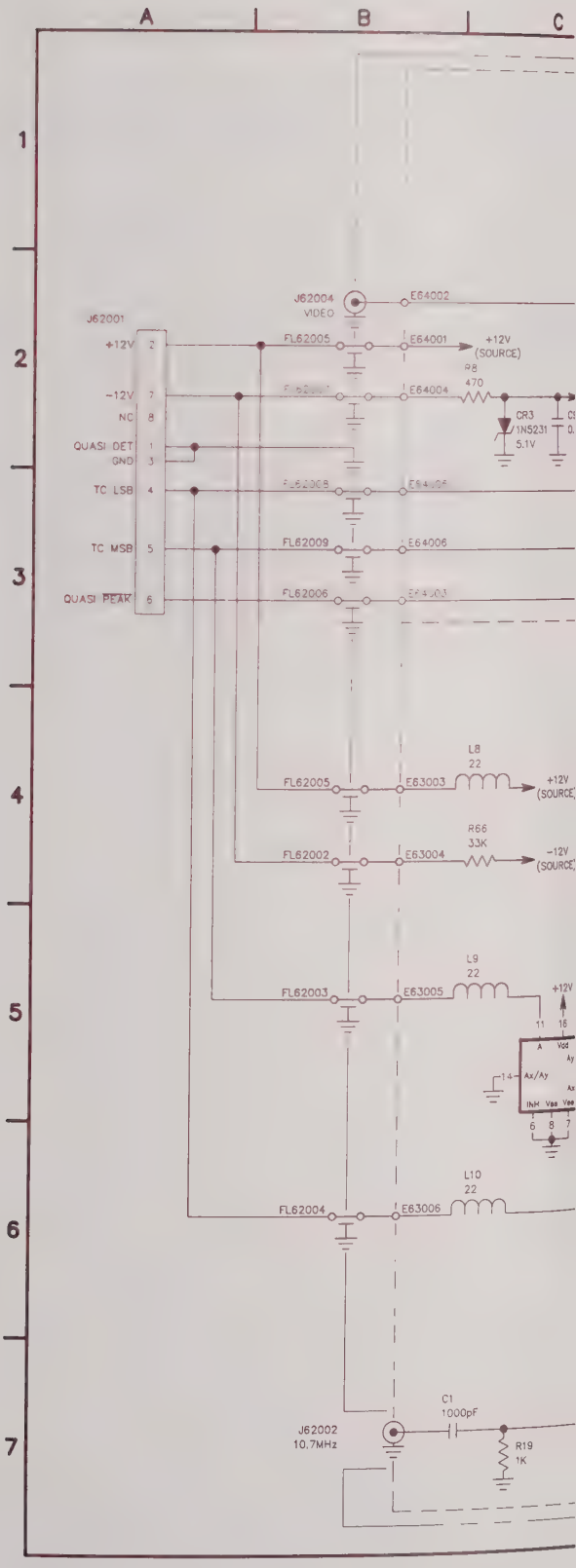
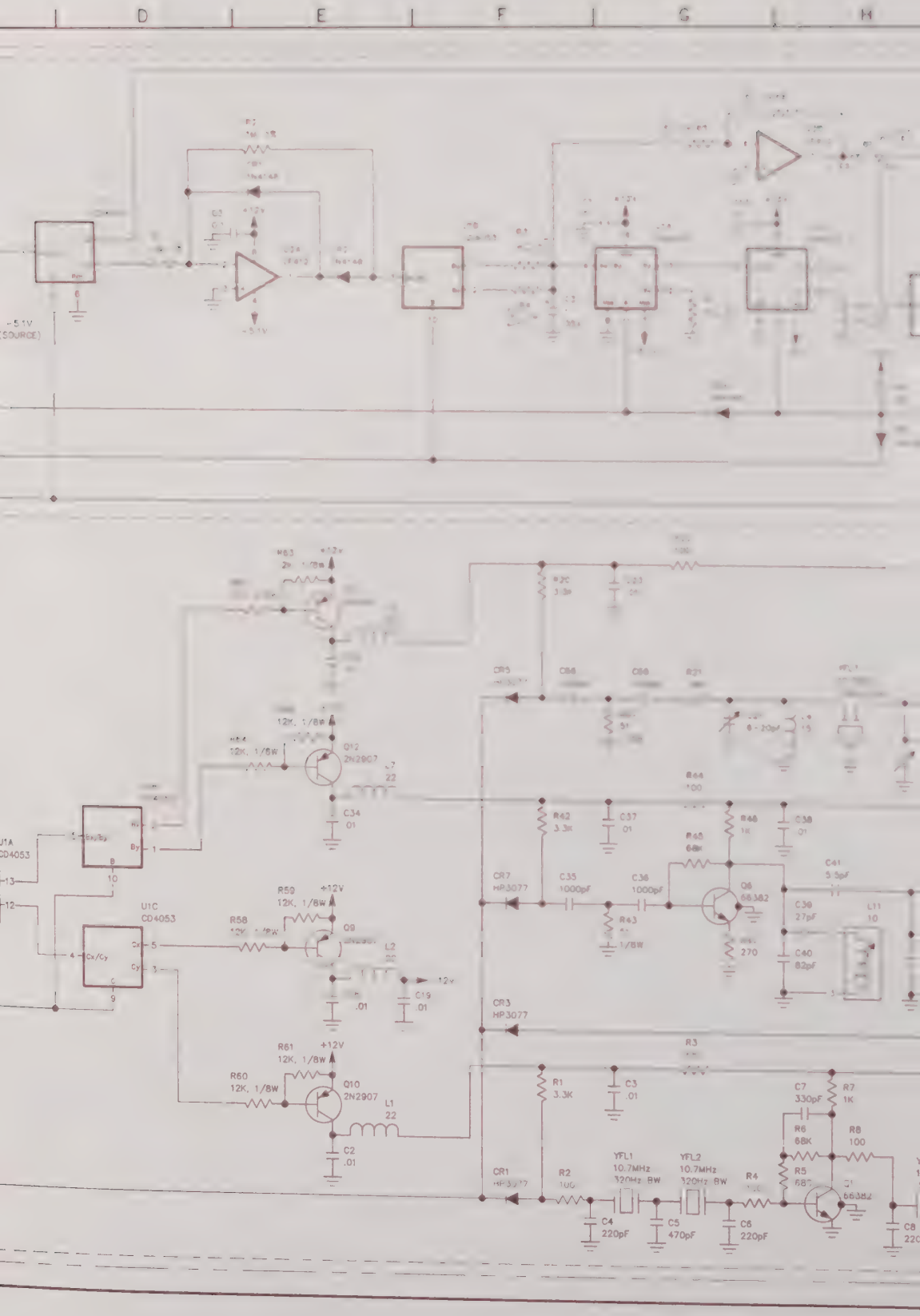
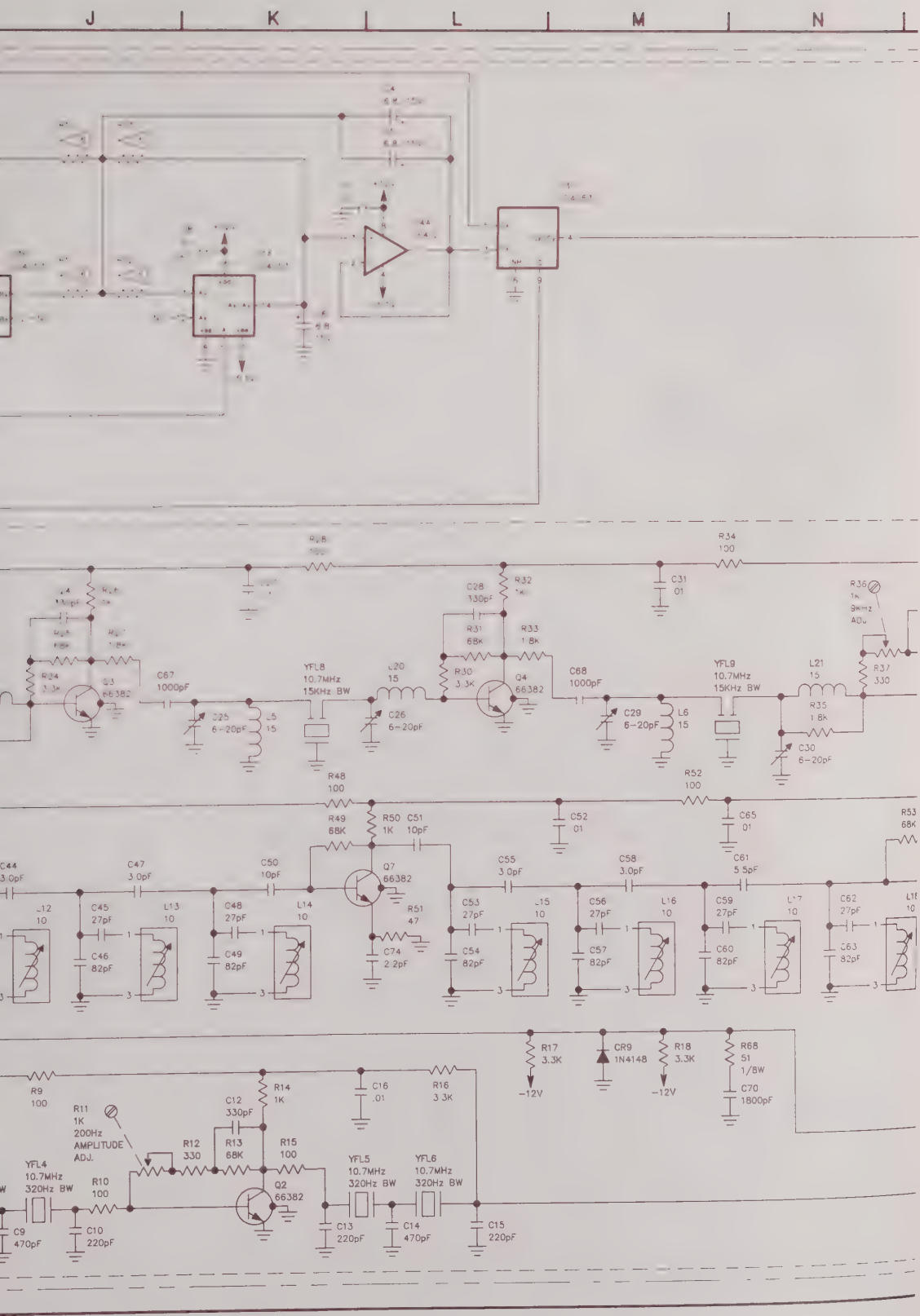


Figure 5-9 Quasi-peak Assembly (Sheet 1 of 2)
(0000-5318-000-F)


A
B
C
1
2
3
4
5
6
7
J62004
VIDEO
E64002
J62001
+12V
2
FL62005
E64001
+12V
(SOURCE)
-12V
7
E64004
R8
470
NC
8
CR3
1N5231
5.1V
QUASI DET
1
GND
3
TC LSB
4
TC MSB
5
FL62009
E64006
QUASI PEAK
6
FL62006
L8
22
E63003
+12V
(SOURCE)
R66
33K
FL62002
E63004
-12V
(SOURCE)
L9
22
FL62003
E63005
+12V
11
16
A
Vdd
Ay
14
Ax/Ay
Ax
INH
Vss
Vee
6
8
7
L10
22
FL62004
E63006
C1
1000pF
J62002
10.7MHz
R19
1K


D
E
F
G
H
-5.1V
(SOURCE)
+12v
-5.1V
R63
2K 1/8W
12K, 1/8W
R64
12K, 1/8W
Q12
2N2907
L7
22
C34
.01
U1A
CD4053
U1C
CD4053
R59
12K, 1/8W
+12V
R58
12K, 1/8W
Q9
2N2907
L2
.01
C19
.01
12v
R61
12K, 1/8W
+12V
R60
12K, 1/8W
Q10
2N2907
L1
22
C2
.01
R42
3.3K
C37
.01
R44
100
R46
1K
R45
68K
C38
.01
C41
3.9pF
CR7
HP3077
C35
1000pF
C36
1000pF
Q8
68382
C39
27pF
L11
10
R43
1/8W
270
C40
82pF
CR3
HP3077
R3
R1
3.3K
C3
.01
C7
330pF
R7
1K
R6
68K
R8
100
R5
68K
Q1
68382
CR1
R2
100
YFL1
10.7MHz
120KHz BW
YFL2
10.7MHz
120Hz BW
R4
C4
220pF
C5
470pF
C6
220pF
C8
220


J
K
L
M
N
R34
100
C31
.01
C28
330pF
R32
R31
68K
R33
1.8K
R30
3.3K
Q4
66382
C68
1000pF
YFL9
10.7MHz
15KHz BW
L21
15
R36
1K
3KHz
ADJ.
R37
330
R35
1.8K
C30
6-20pF
C29
6-20pF
L6
15
R24
3.3K
Q3
66382
C67
1000pF
C25
6-20pF
L5
15
YFL8
10.7MHz
15KHz BW
L20
15
C26
6-20pF
R48
100
R49
68K
R50
1K
C51
10pF
Q7
66382
R51
47
C74
2.2pF
R52
100
C52
.01
C65
.01
R53
68K
C44
3.0pF
C47
3.0pF
C50
10pF
C55
3.0pF
C58
3.0pF
C61
5.5pF
L12
10
C45
27pF
C46
82pF
L13
10
C48
27pF
C49
82pF
L14
10
C53
27pF
C54
82pF
L15
10
C56
27pF
C57
82pF
L16
10
C59
27pF
C60
82pF
L17
10
C62
27pF
C63
82pF
L18
10
R17
3.3K
-12V
CR9
1N4148
R18
3.3K
-12V
R68
51
1/8W
C70
1800pF
R9
100
R11
1K
200Hz
AMPLITUDE
ADJ.
R14
1K
C12
330pF
R12
330
R13
68K
R15
100
C16
.01
R16
3.3K
YFL4
10.7MHz
320Hz BW
R10
100
Q2
66382
YFL5
10.7MHz
320Hz BW
YFL6
10.7MHz
320Hz BW
C9
470pF
C10
220pF
C13
220pF
C14
470pF
C15
220pF

P
Q
R
S
1
2
3
4
5
6
7
C72
330pF
R73
470
R74
100
R70
2K
R56
200
120KHz ADJ
C17
1000pF
R69
330
Q13
6638Z
CR8
HP3077
RT1
100
RT2
100
CR4
HP3077
CR2
HP3077
R41
1K
QUASI PEAK FILTER (63000)
PCBD 1700-5328-000
PCBD ASSY 7010-5338-000
QUASI PEAK FILTER (62000)
MECH ASSY 7005-5348-000

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 62000
   B. FILTER PC BD ASSY - 63000
   C. DETECTOR PC BD ASSY - 64000

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (µF).

4. W1 IS INSTALLED AT TEST.

5. THE FOLLOWING RESISTORS ARE SELECTED AT TEST (S.A.T.):

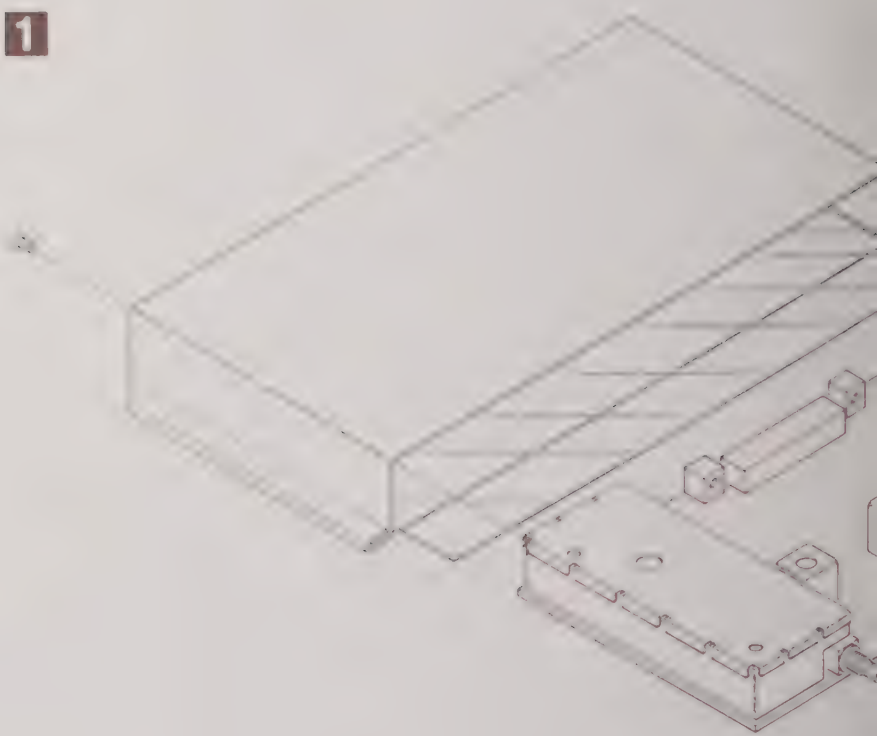
RESISTOR(S)	NOMINAL VALUE	RANGE
R3	909Ω	806Ω THRU 1K
R4	45.3K	40.2K THRU 49.9K
R5 & R6	1.24M	1M THRU 1.5M
R7	232K	200K THRU 274K
R10 & R13	16.2K	13K THRU 20K
R11 & R12	26.1K	20K THRU 43.2K
R14	4.7M	2.2M THRU 5.6M

6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (µH).

Figure 5-9 Quasi-peak Assembly (Sheet 2 of 2) (0000-5318-000-F)

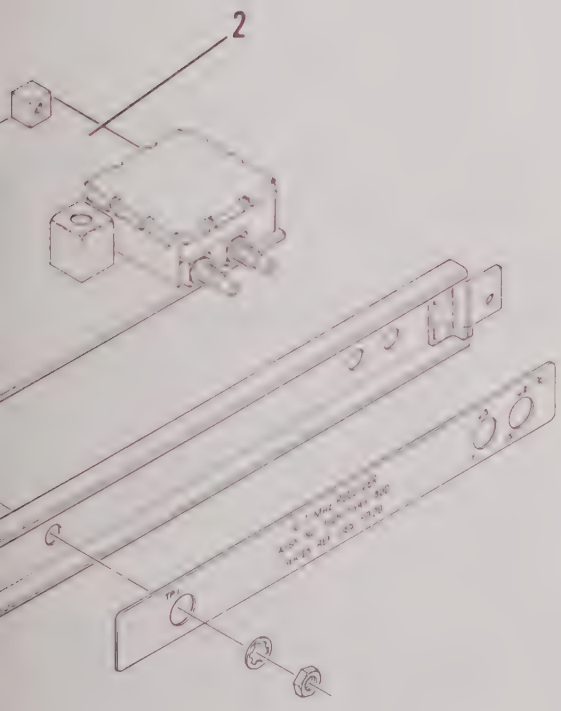
KEY:

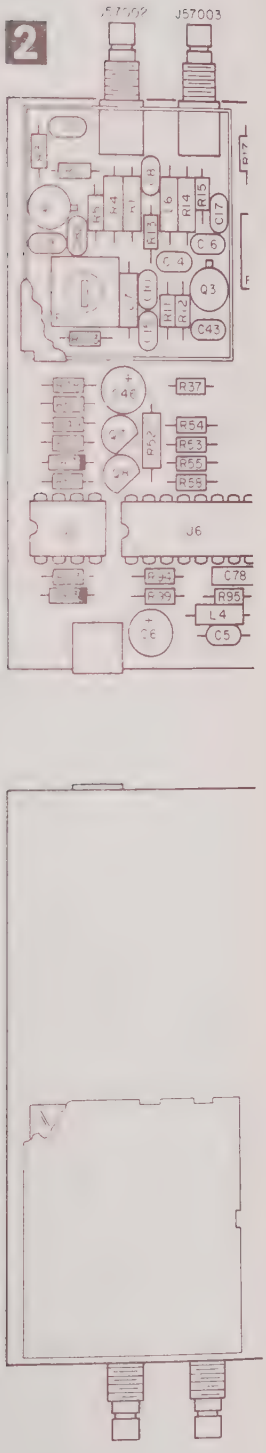
1. 10.7 MHz Receiver A
   (7005-5349-800-A)
2. 10.7 MHz Receiver B
   (7010-5339-800-D)

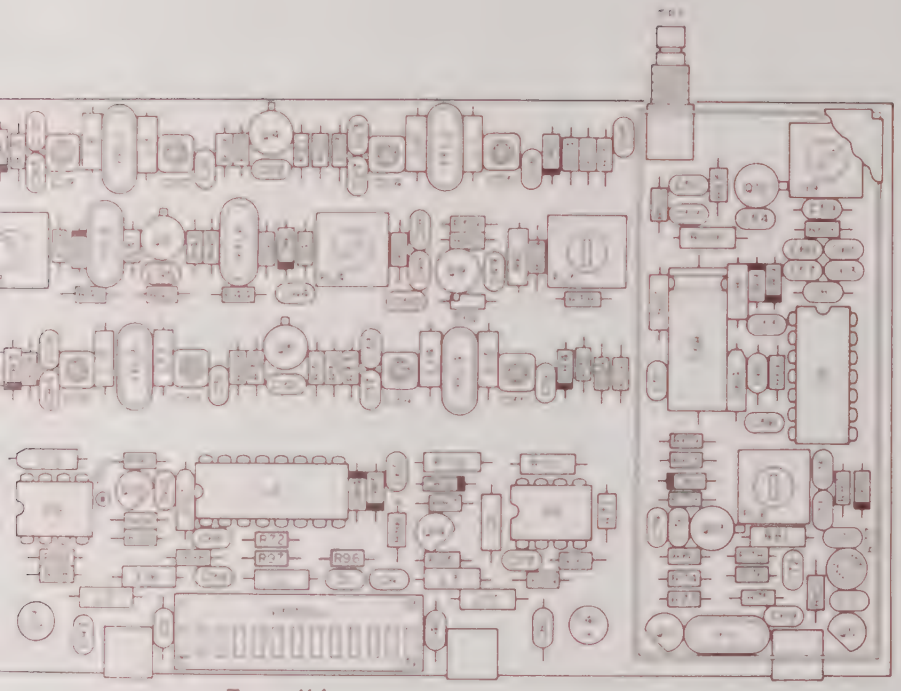


---

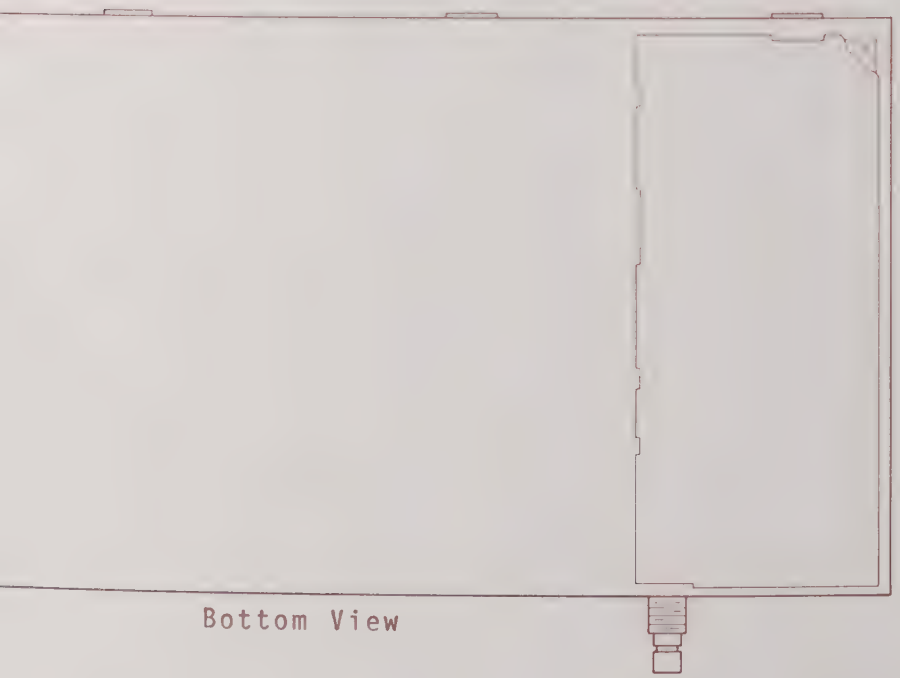
l Assy


2


2
J57003
R17
R14
R15
C17
C6
C4
Q3
C43
R37
R54
R53
R55
R56
J6
C78
R95
L4
C5

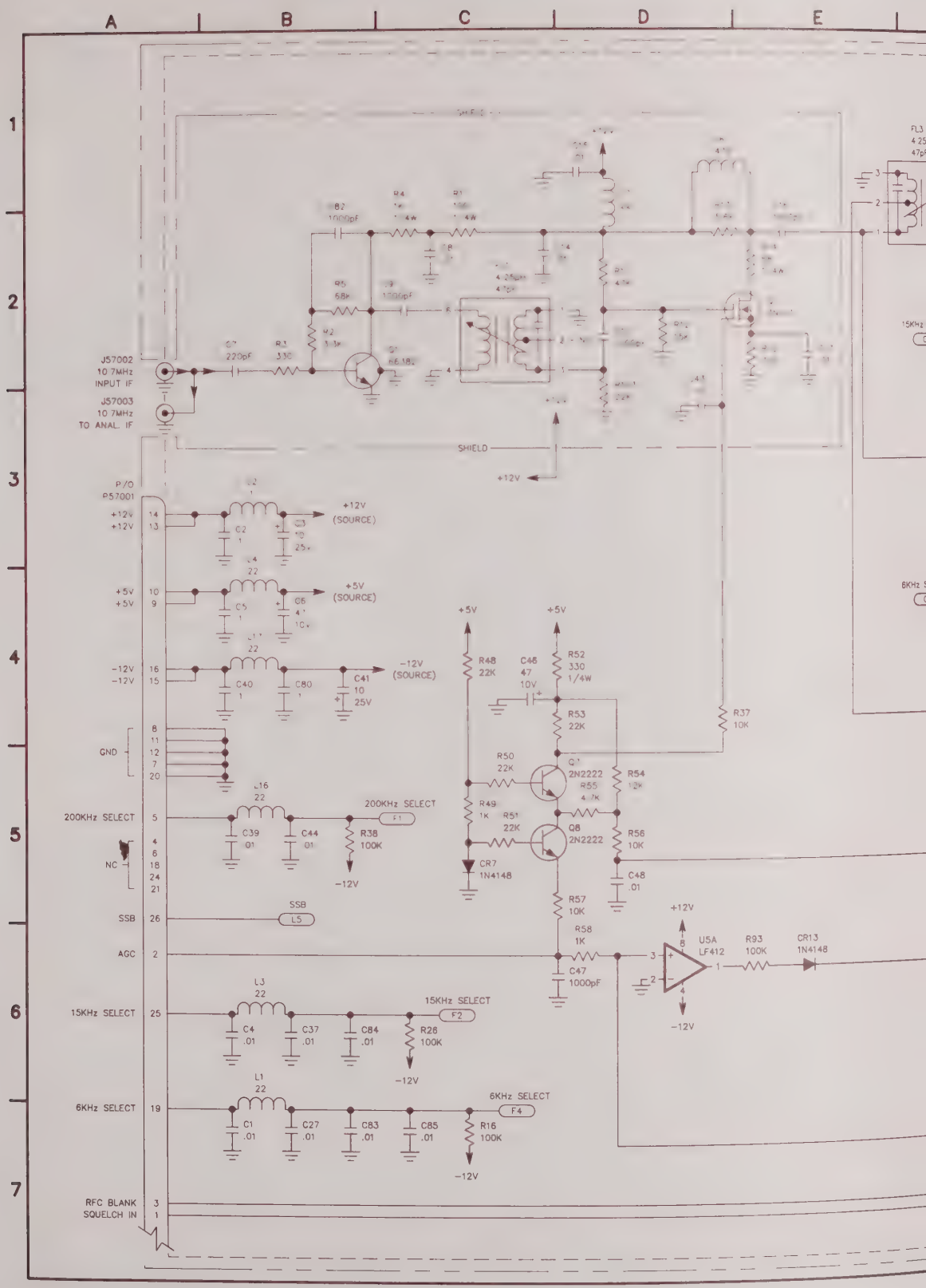


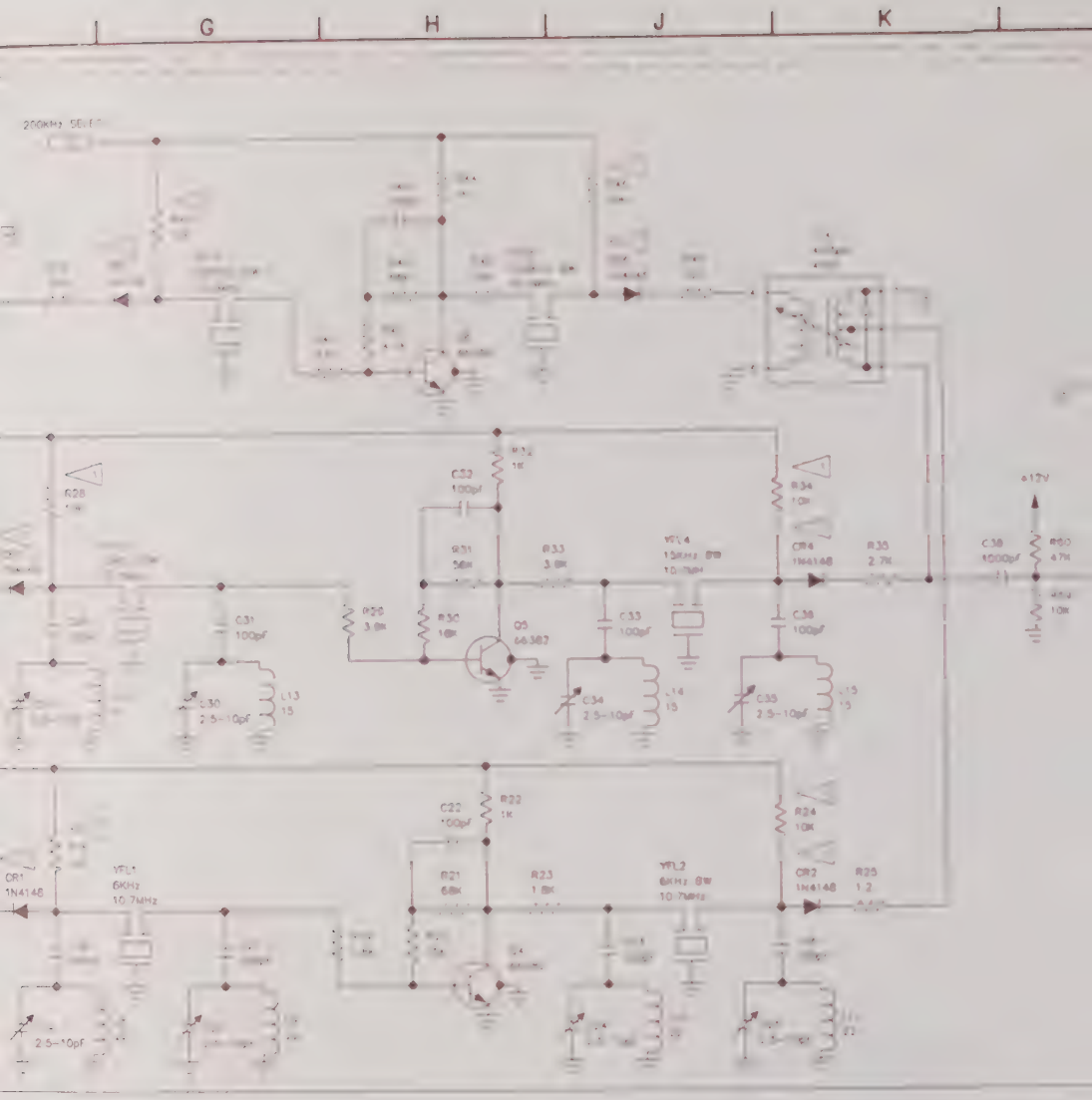
Top View

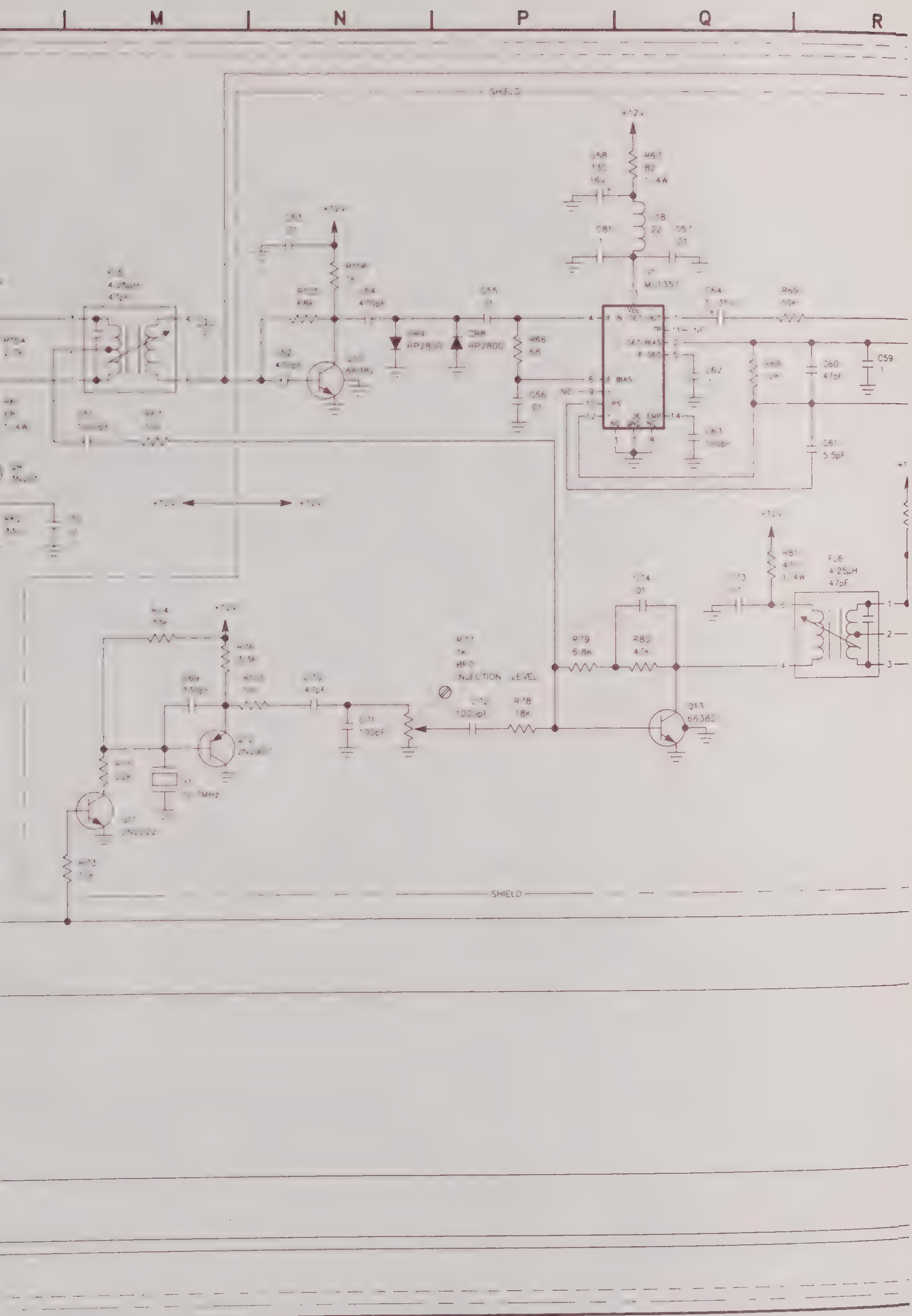


Bottom View

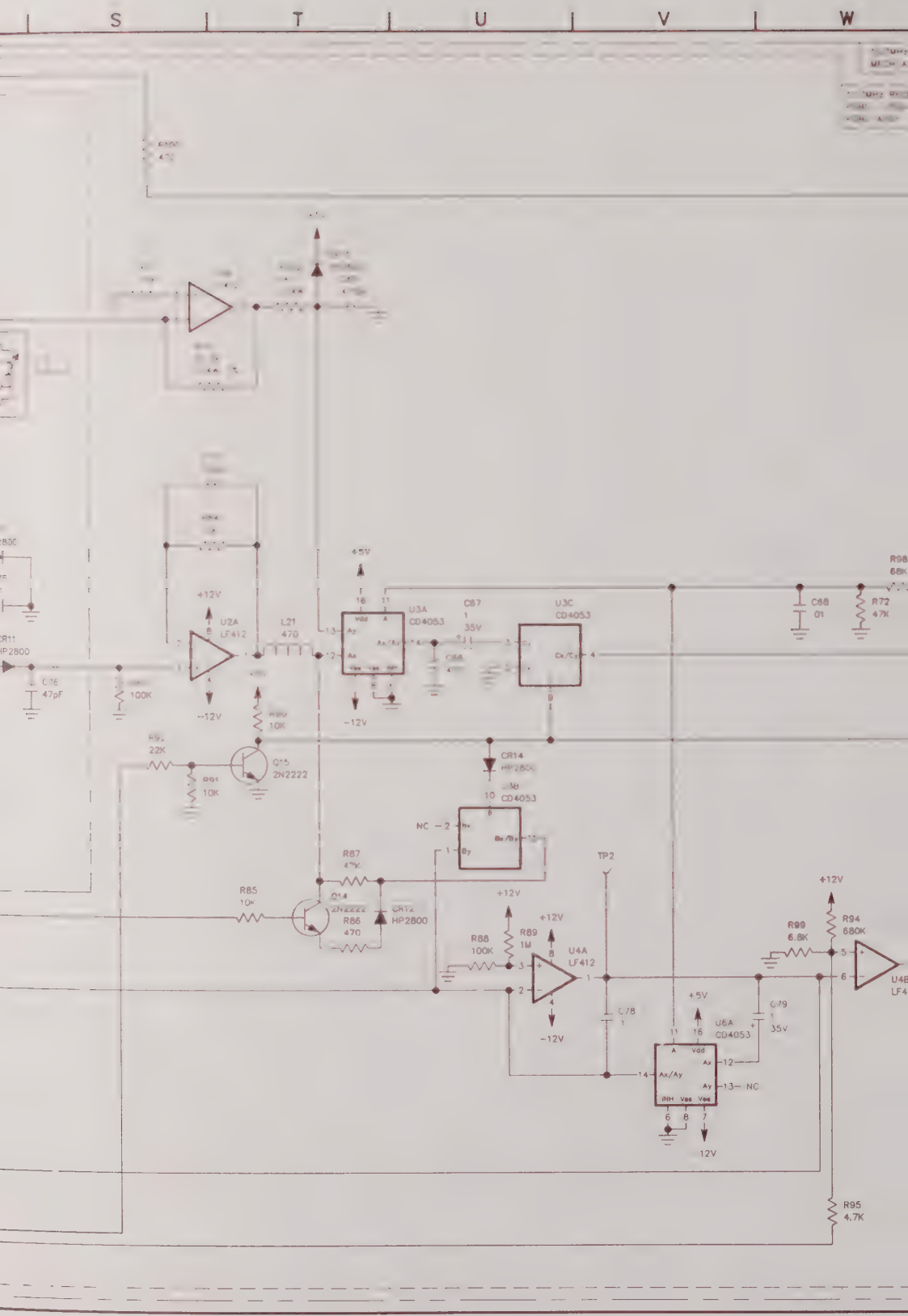
Figure 5-10 10.7 MHz (FM/AM/SSB) Receiver Assembly (Sheet 1 of 2) (0000-5319-800-D1)

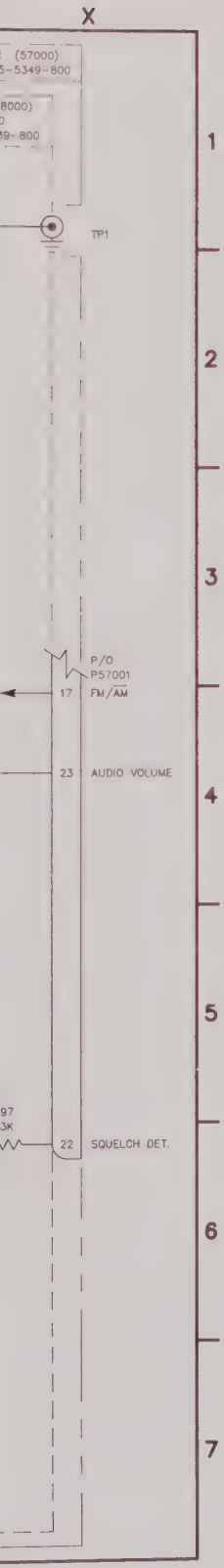

A
B
C
D
E
1
2
3
4
5
6
7
J57002
10.7MHz
INPUT IF
J57003
10.7MHz
TO ANAL. IF
SHIELD
+12V
P/O
P57001
+12V
+12V
+12V
(SOURCE)
+5V
+5V
+5V
(SOURCE)
-12V
-12V
-12V
(SOURCE)
GND
200KHz SELECT
NC
SSB
AGC
15KHz SELECT
6KHz SELECT
RFC BLANK
SQUELCH IN
200KHz SELECT
F1
SSB
L5
15KHz SELECT
F2
6KHz SELECT
F4
U5A
LF412
2N2222
1N4148


G
H
J
K
200KHz SELECT
R28
C32
100pF
R32
1K
R31
56K
R33
3.8K
R34
10K
CR4
1N4148
R35
2.7K
C38
1000pF
R60
47K
+12V
C31
100pF
R29
3.8K
R30
16K
Q5
66382
C33
100pF
C36
100pF
C30
2.5-10pF
L13
15
C34
2.5-10pF
L14
15
C35
2.5-10pF
L15
15
C22
100pF
R22
1K
R24
10K
CR1
1N4148
YFL1
6KHz
10.7MHz
R21
68K
R23
1.8K
YFL2
6KHz BW
10.7MHz
CR2
1N4148
R25
1.2
2.5-10pF



M
N
P
Q
R
SHIELD
+12V
R67
82
1/4W
L8
22
C58
C81
C51
.01
C64
R69
10K
Vcc
DET BIAS
BIAS
PS
NC
C62
C60
47pF
C59
C56
.01
R66
68
C55
.01
CR8
HP2800
HP2800
C63
C61
5.5pF
FL6
4.25μH
47pF
C74
.01
R79
6.8K
R83
47K
Q13
66382
R78
18K
INJECTION LEVEL
100pF
47pF
100pF
SHIELD


S
T
U
V
W
+5V
+12V
U2A
LF412
L21
470
U3A
CD4053
C87
1
35V
U3C
CD4053
C68
01
R72
47K
R98
68K
CR11
HP2800
C76
47pF
100K
-12V
R90
10K
R92
22K
Q15
2N2222
R91
10K
CR14
HP2800
U3B
CD4053
NC
R87
47K
R85
10K
Q14
2N2222
R86
470
CR12
HP2800
TP2
R88
100K
R89
1M
U4A
LF412
C78
1
U6A
CD4053
C79
1
35V
R99
6.8K
R94
680K
R95
4.7K



NOTES (UNLESS OTHERWISE STATED):

1. THRU SER. NO. 2450:
   CR1, CR2, CR3, CR4, CR5, CR6 WERE MA47047; R18, R24, R28, R34, R40, R46 WERE 18K, 1/8W.

2. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 57000.
   B. PC BD ASSY - 58000.

3. ALL RESISTORS ARE 1/8W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

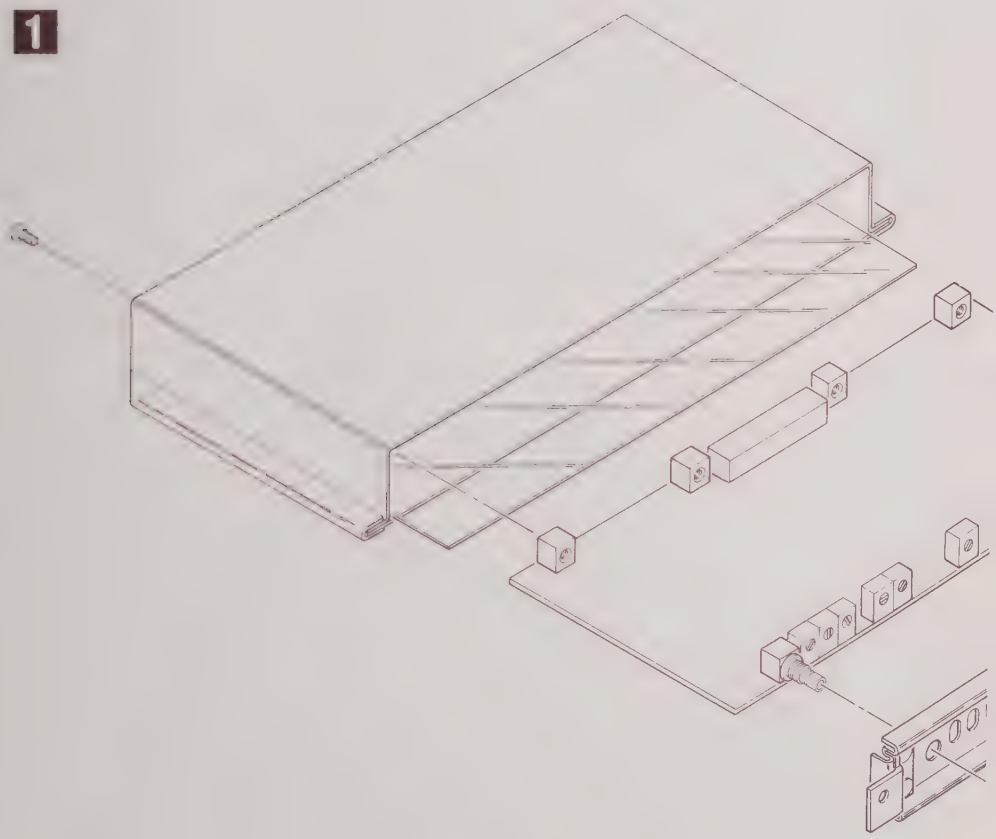
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

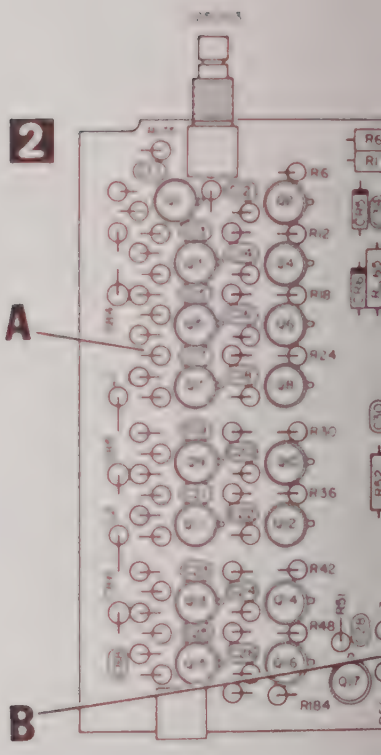
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

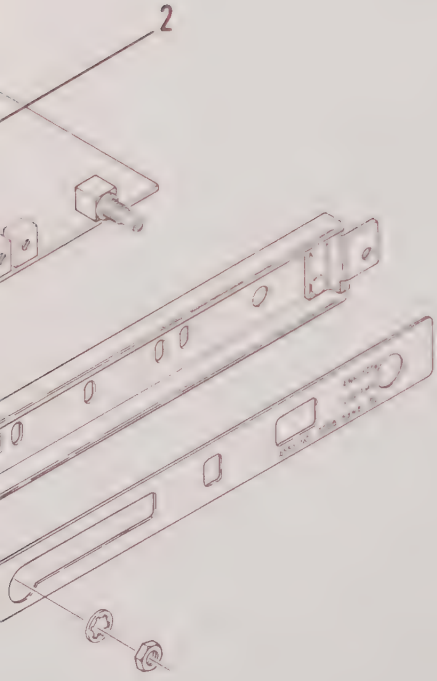
Figure 5-10 10.7 MHz (FM/AM/SSB) Receiver Assembly (Sheet 2 of 2) (0000-5319-800-D1)

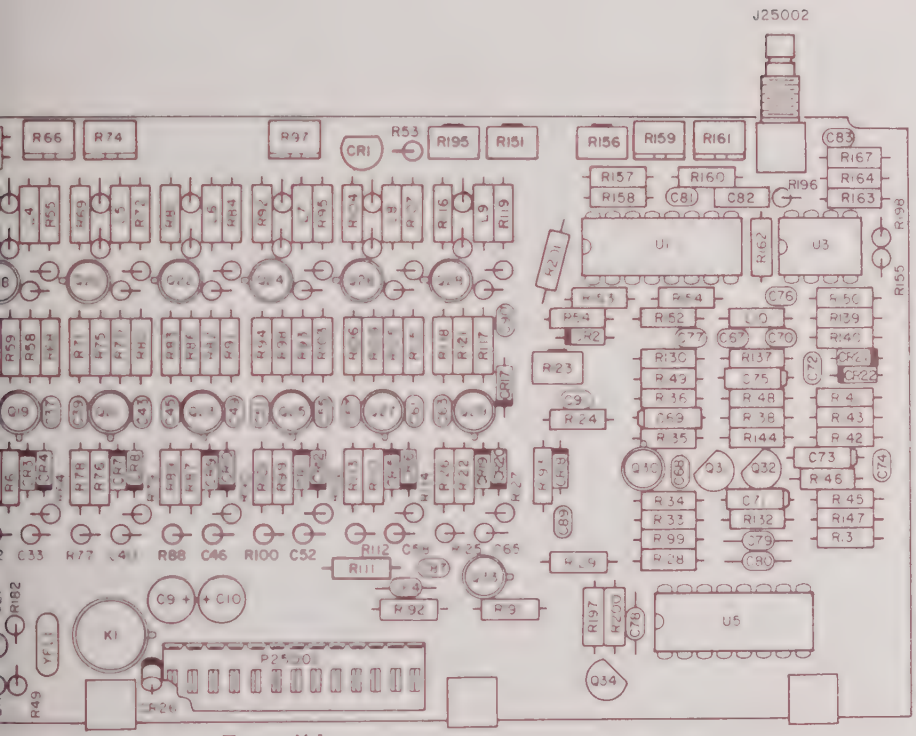
KEY:

1. Analyzer Log Amp Assy (7005-5348-100-A)
2. Analyzer Log Amp PC Bd Assy (7010-5338-100-D3)

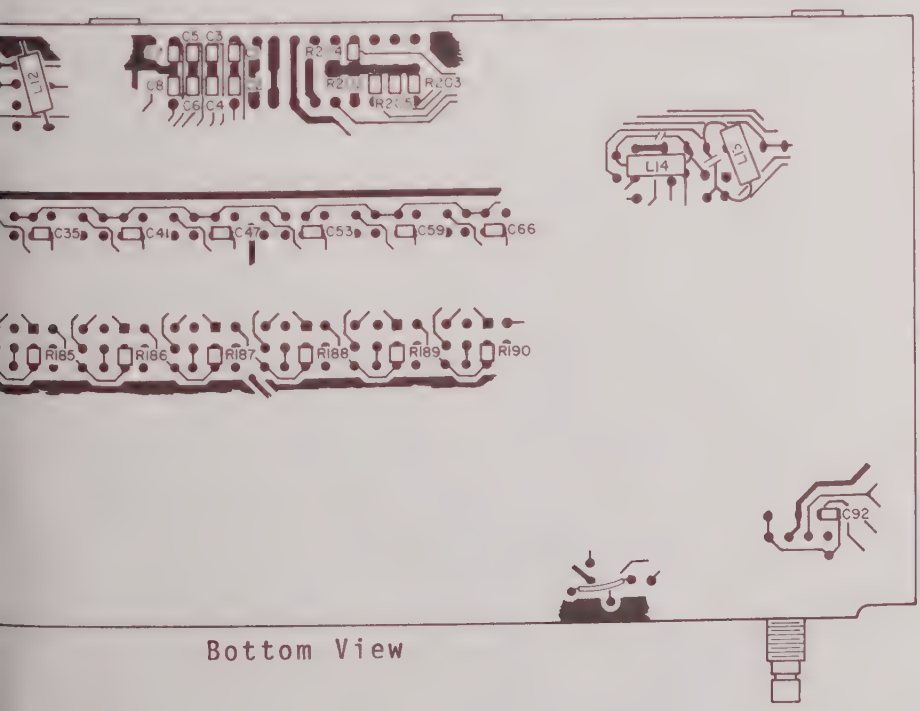



2
A
B
R6
R12
R18
R24
R30
R36
R42
R48
R184

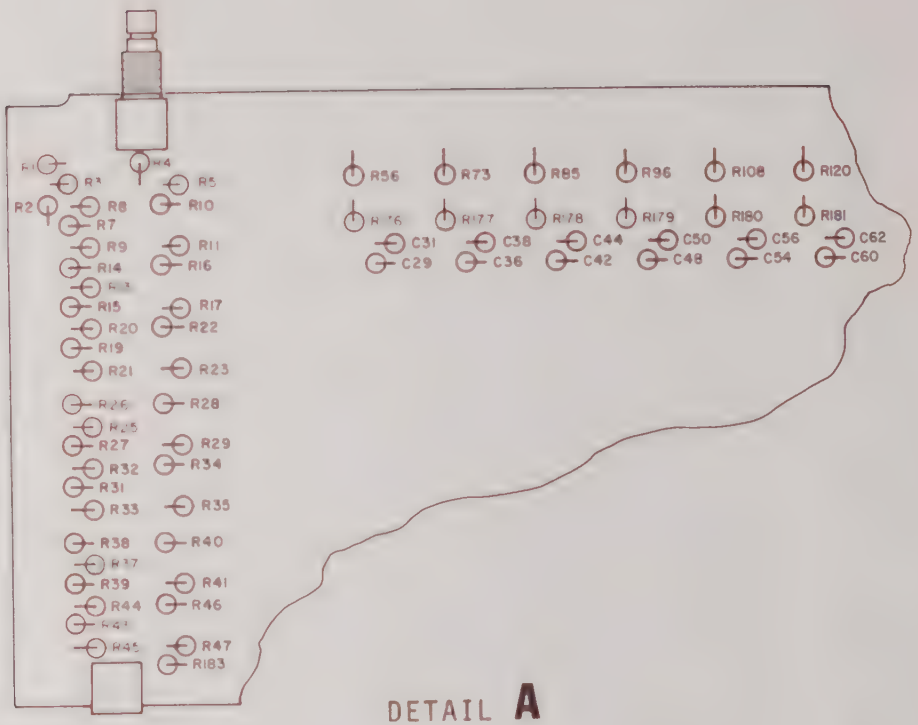

2



Top View



Bottom View

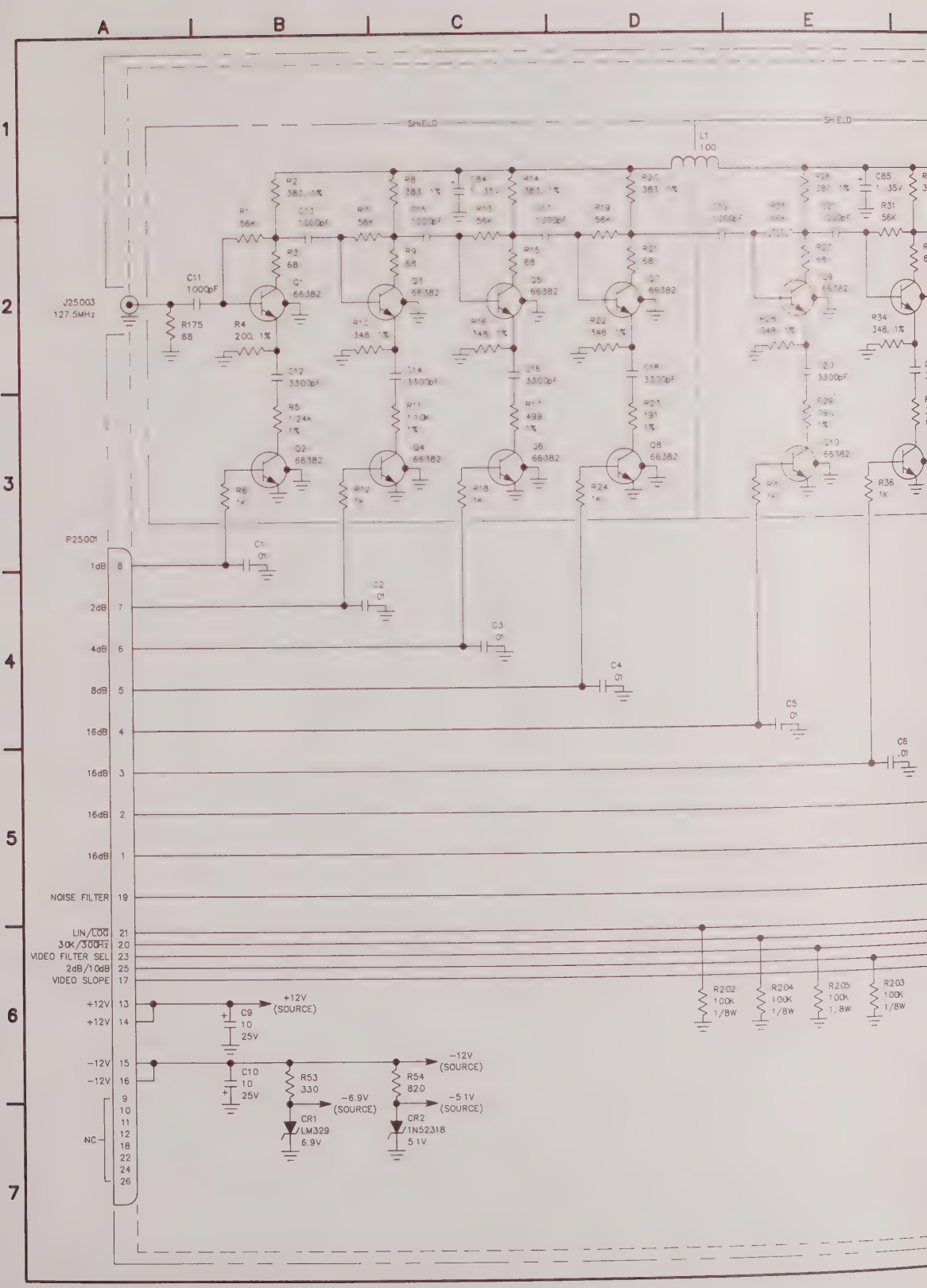


DETAIL **A**

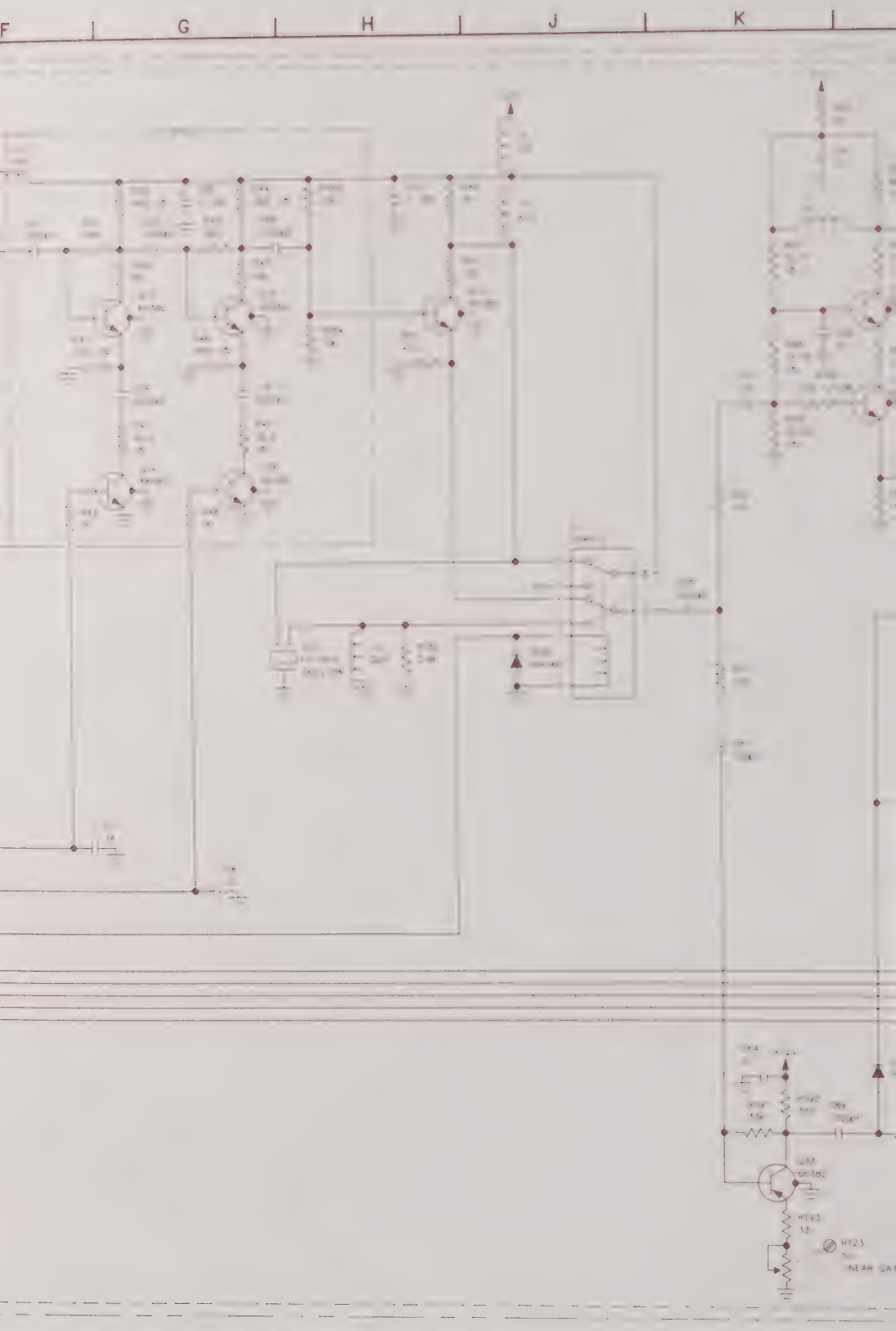
DETAIL **B**

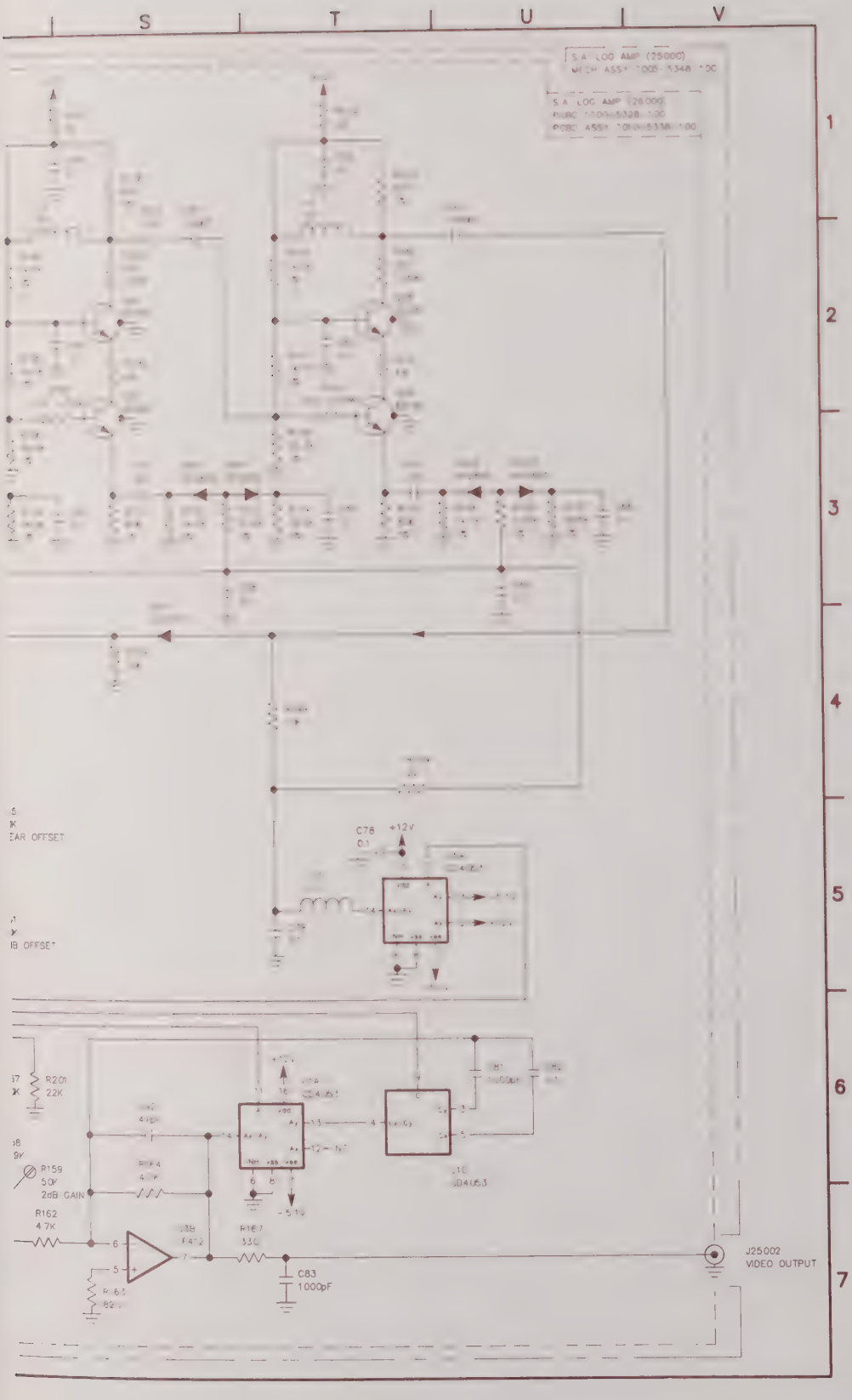
NOTE: DETAIL TYPICAL FOR C27, C84, C85, C86.

Figure 5-11 Analyzer Log Amp Assembly (Sheet 1 of 2) (0000-5319-100-B3)



A
B
C
D
E
1
2
3
4
5
6
7
SHIELD
SHIELD
L1
100
J25003
127.5MHz
C11
1000pF
R175
68
R4
200, 1%
R3
68
R5
1.24K
1%
R6
1K
Q1
66382
Q2
66382
Q3
66382
Q4
66382
Q5
66382
Q6
66382
Q7
66382
Q8
66382
R9
68
R10
348, 1%
R11
1.10K
1%
R12
1K
R14
383, 1%
R15
68
R16
348, 1%
R17
499
1%
R18
1K
R19
56K
R20
383, 1%
R21
68
R22
348, 1%
R23
191
1%
R24
1K
C85
1.35V
R31
56K
R34
348, 1%
R36
1K
P25001
1dB 8
2dB 7
4dB 6
8dB 5
16dB 4
16dB 3
16dB 2
16dB 1
NOISE FILTER 19
LIN/LOG 21
30K/300Hz 20
VIDEO FILTER SEL 23
2dB/10dB 25
VIDEO SLOPE 17
+12V 13
+12V 14
-12V 15
-12V 16
NC
9
10
11
12
18
22
24
26
C1
.01
C2
.01
C3
.01
C4
.01
C5
.01
C6
.01
C9
10
25V
+12V
(SOURCE)
C10
10
25V
R53
330
-6.9V
(SOURCE)
CR1
LM329
6.9V
R54
820
-12V
(SOURCE)
-5.1V
(SOURCE)
CR2
1N52318
5.1V
R202
100K
1/8W
R204
100K
1/8W
R205
100K
1/8W
R203
100K
1/8W


F
G
H
J
K
R123
NEAR GA


S
T
U
V
1
2
3
4
5
6
7
S.A. LOG AMP (25000)
C78
0.1
+12V
R201
22K
R159
50K
2dB GAIN
R162
4.7K
R164
330
C83
1000pF
-5.1V
J25002
VIDEO OUTPUT

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 25000.
   B. PC BD ASSY - 26000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

4. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

Figure 5-11 Analyzer Log Amp Assembly (Sheet 2 of 2) (0000-5318-100-B3)

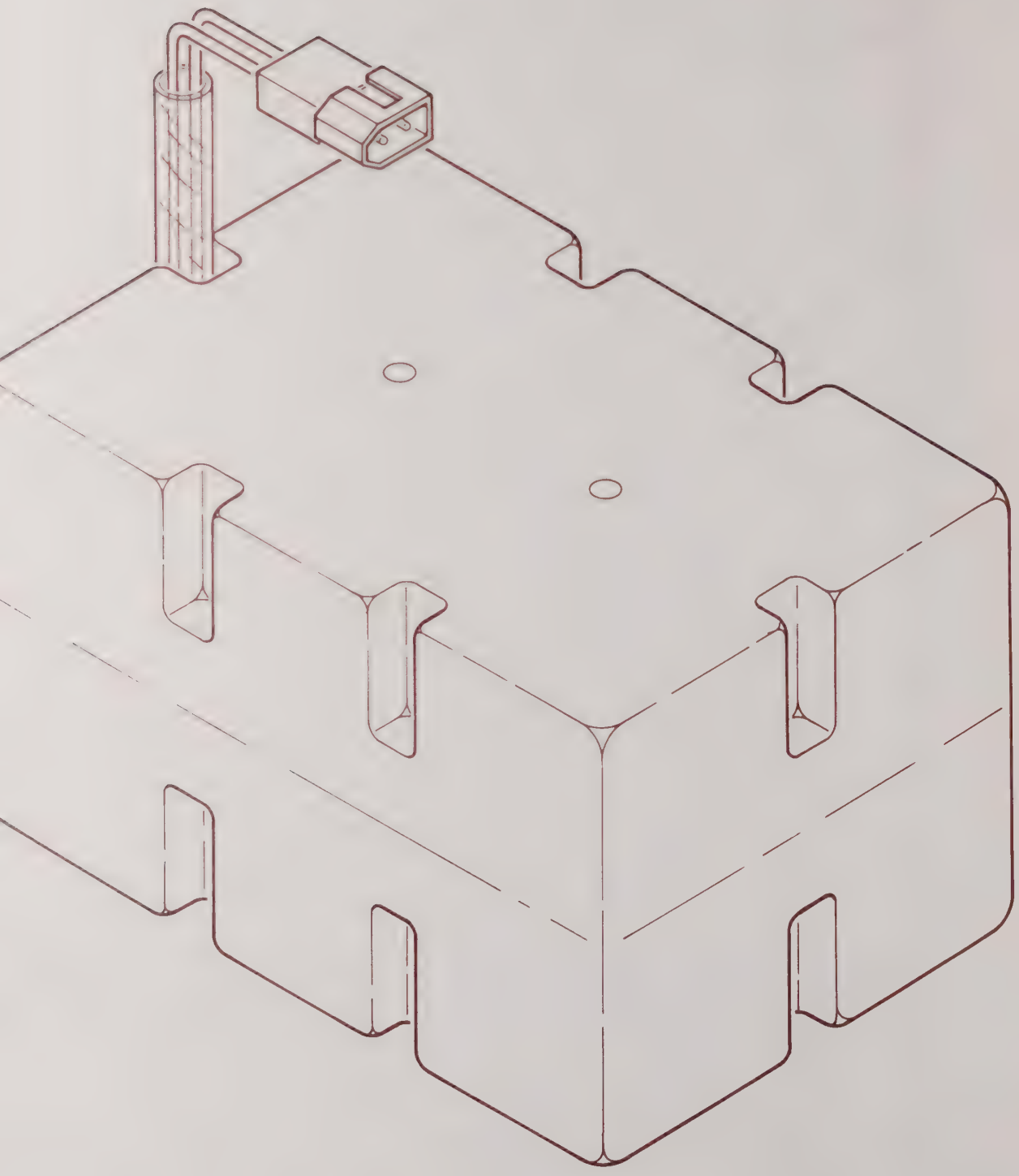
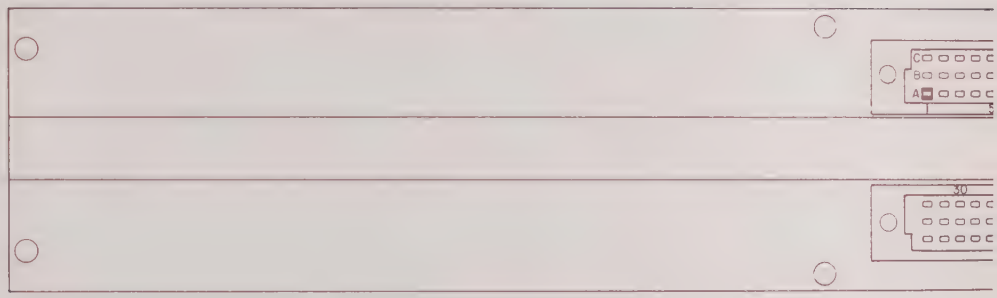
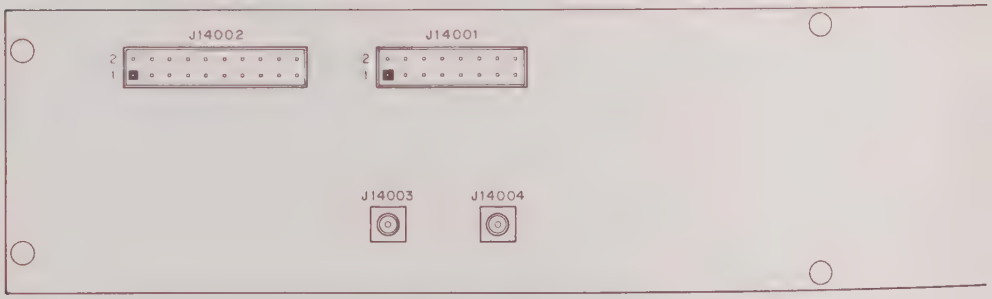


Figure 5-12 Battery Assembly (7005-7624-500-L)

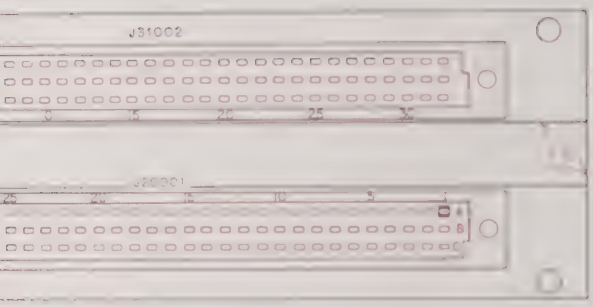


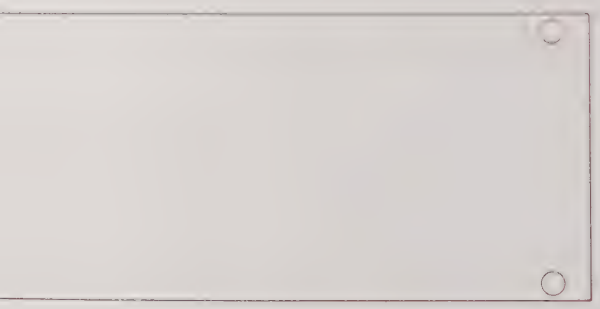
Top View



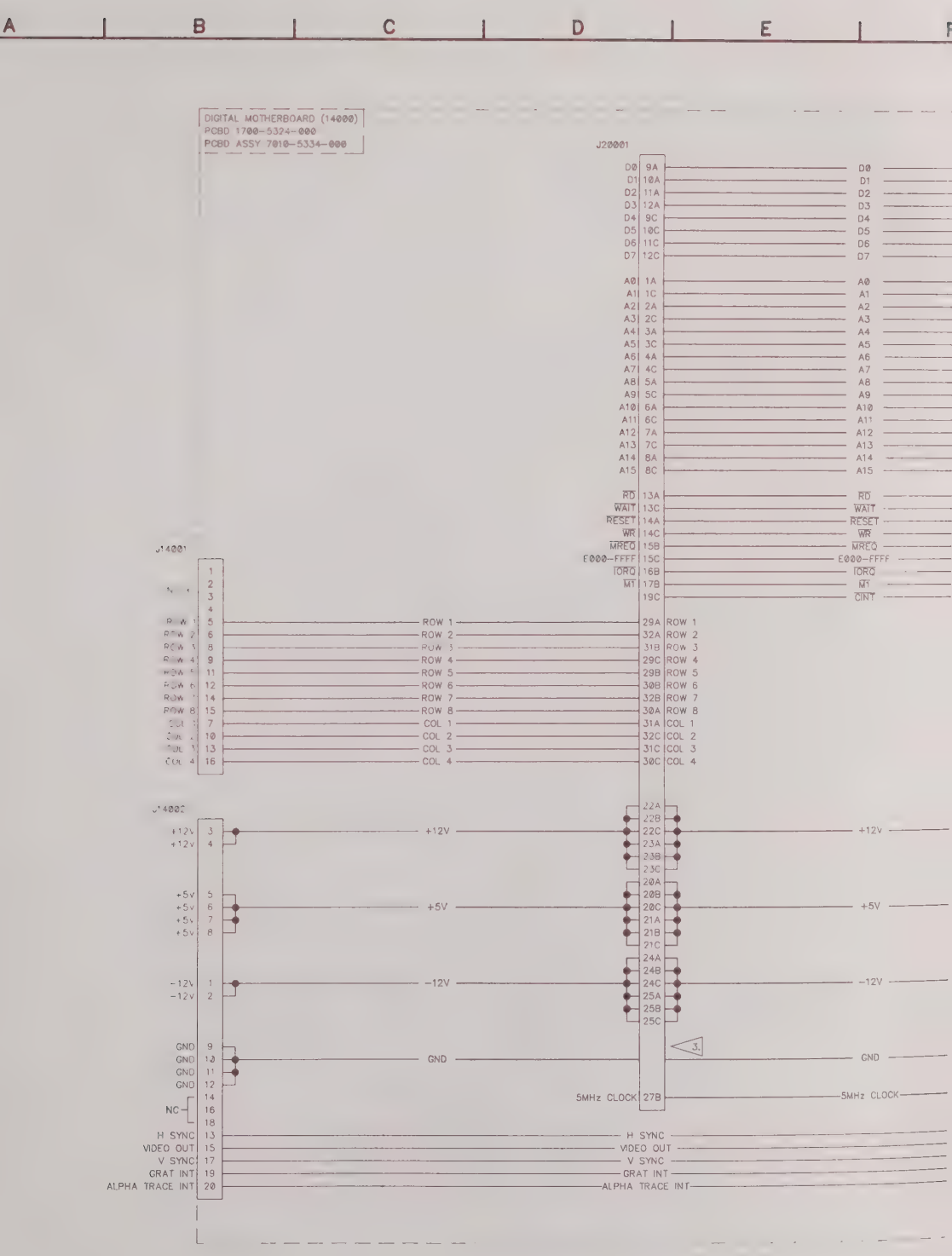
Bottom View

Digital Motherboard PC Bd Assy (701





5334-000-C3)


A
B
C
D
E
DIGITAL MOTHERBOARD (14000)
PCBD 1700-5324-000
PCBD ASSY 7010-5334-000
J20001
D0 9A
D1 10A
D2 11A
D3 12A
D4 9C
D5 10C
D6 11C
D7 12C
A0 1A
A1 1C
A2 2A
A3 2C
A4 3A
A5 3C
A6 4A
A7 4C
A8 5A
A9 5C
A10 6A
A11 6C
A12 7A
A13 7C
A14 8A
A15 8C
RD 13A
WAIT 13C
RESET 14A
WR 14C
MREQ 15B
E000-FFFF 15C
IORQ 16B
M1 17B
19C
CINT
J14001
ROW 1
ROW 2
ROW 3
ROW 4
ROW 5
ROW 6
ROW 7
ROW 8
COL 1
COL 2
COL 3
COL 4
29A ROW 1
32A ROW 2
31B ROW 3
29C ROW 4
29B ROW 5
30B ROW 6
32B ROW 7
30A ROW 8
31A COL 1
32C COL 2
31C COL 3
30C COL 4
J14002
+12V
+5V
-12V
GND
NC
H SYNC
VIDEO OUT
V SYNC
GRAT INT
ALPHA TRACE INT
5MHz CLOCK 27B
3.

G
H
J
J14003
5MHz CLOCK
3B H SYNC
4 VIDEO OUT
4B V SYNC
5A GRAT INT
5B ALPHA TRACE INT

NOTES (UNLESS OTHERWISE STATED):

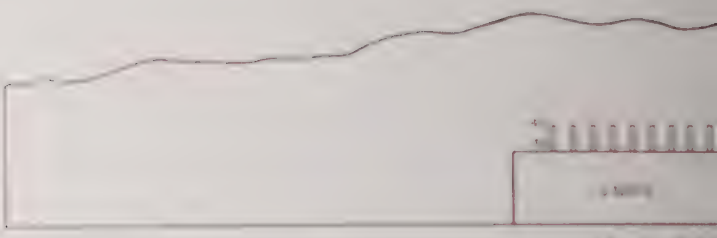
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES: 14000.

2. NOT USED.

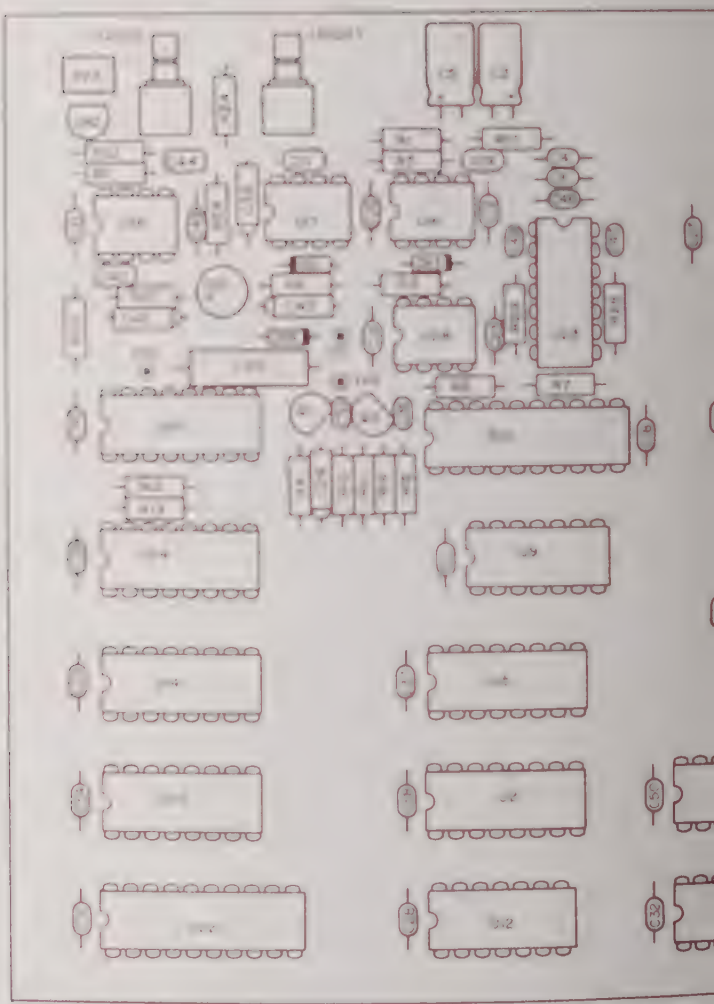
3. FOR J20001, THE FOLLOWING PINS ARE GROUND: 1B THRU 14B (B ONLY), 15A, 16A, 16C, 17A, 17C, 18A, 18B, 18C, 19A, 19B, 26A, 26B, 27A, 27C, 28A, 28B, 28C.

4. FOR J31002, THE FOLLOWING PINS ARE GND: 1A, 1C, 2A, 2B, 2C, 3A, 3C, 4A, 5C, 6A, 6C, 7A, 7B, 7C, 14A, 14B, 15A, 15B, 15C, 16A, 16C, 17A, 17C, 18A, 19B THRU 32B (B ONLY).

Figure 5-13 Digital Motherboard PC Board Assembly (0000-5314-100-D2)

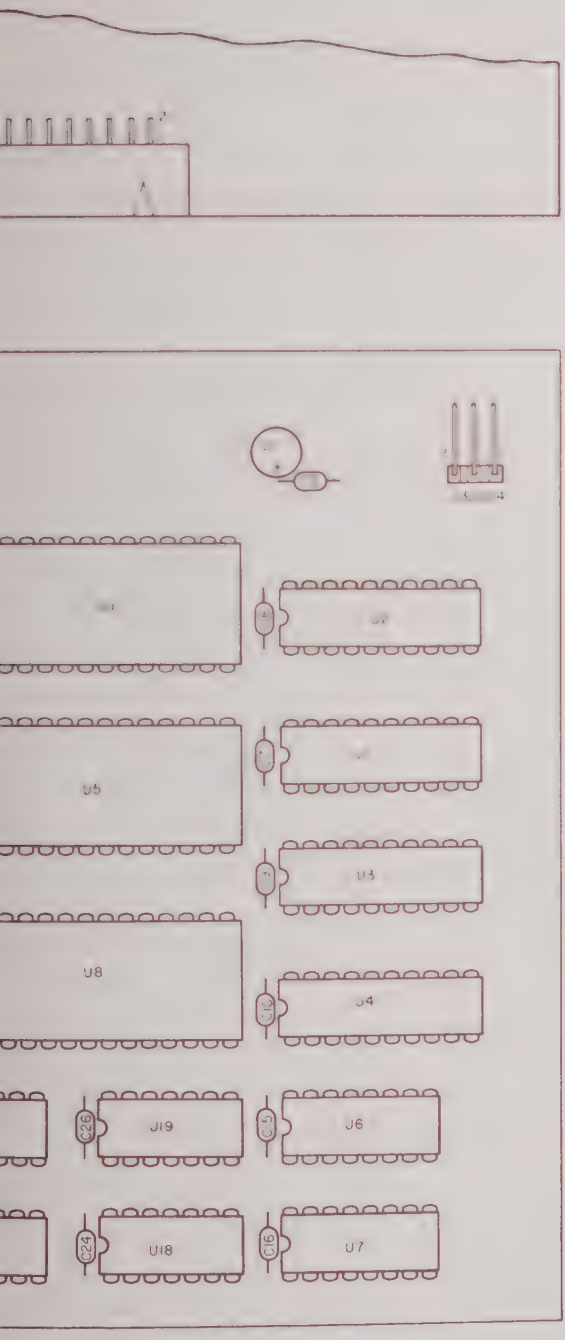


Top Vie

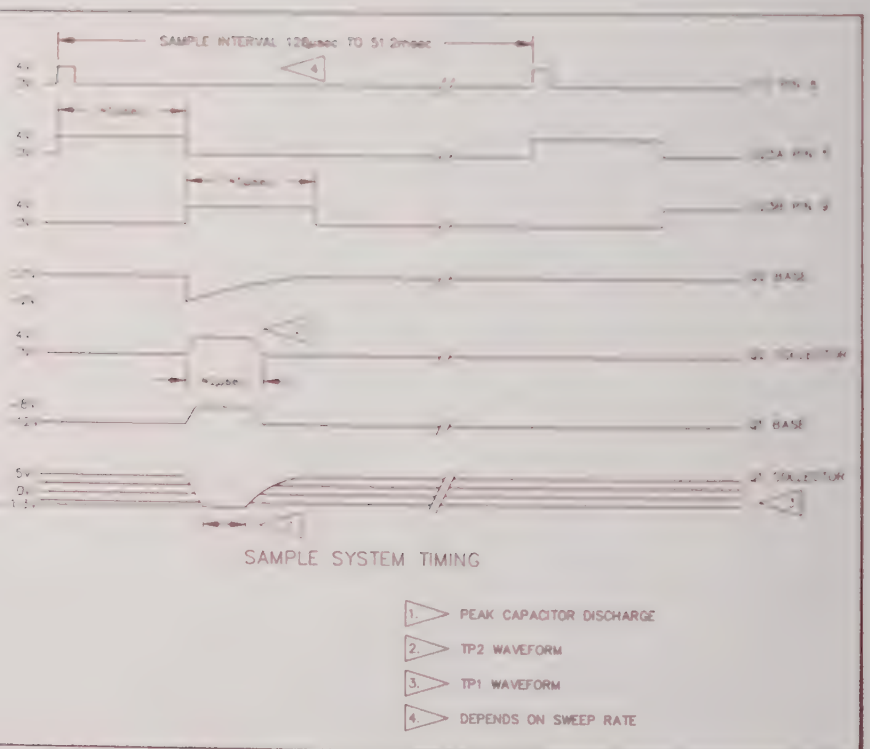


Bottom V

Sweep Digitizer PC Bd As

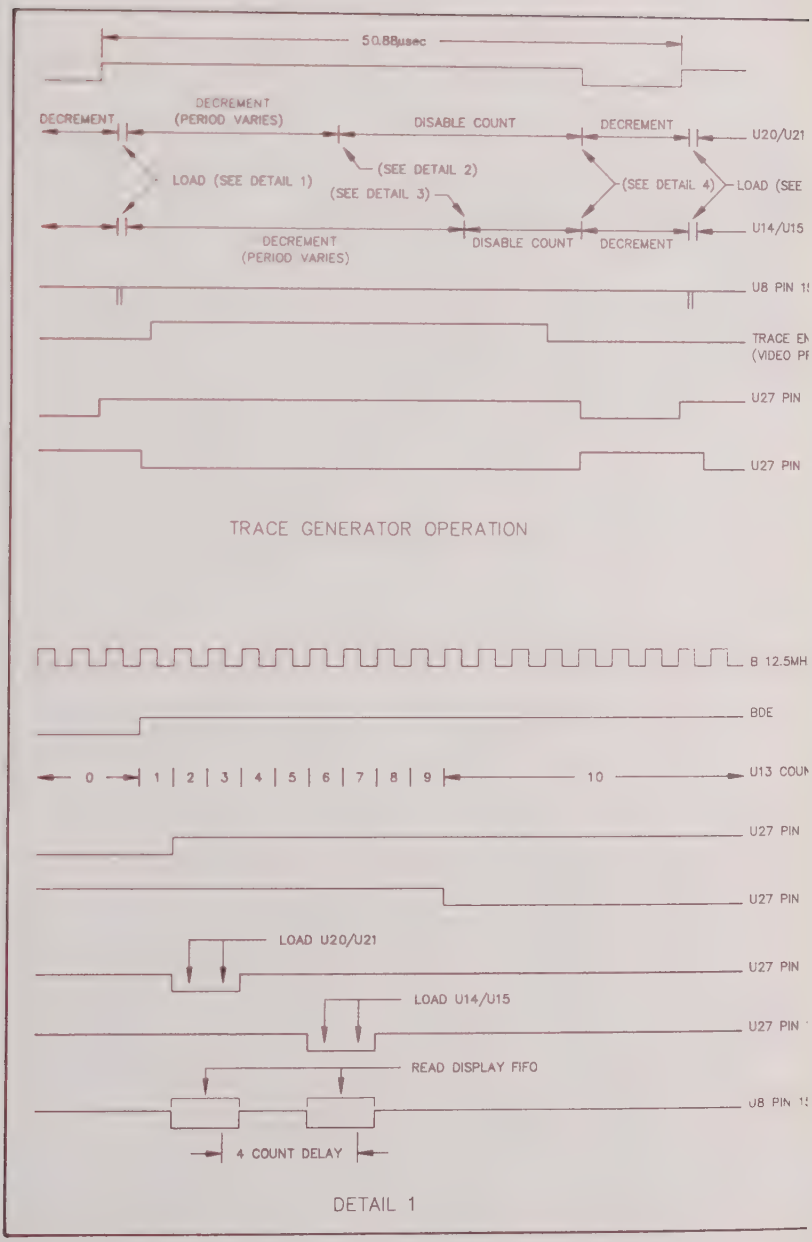


7010-5337-400-B1)



SAMPLE SYSTEM TIMING

1. PEAK CAPACITOR DISCHARGE
2. TP2 WAVEFORM
3. TP1 WAVEFORM
4. DEPENDS ON SWEEP RATE


50.88µsec
DECREMENT
DECREMENT (PERIOD VARIES)
DISABLE COUNT
DECREMENT
U20/U21
LOAD (SEE DETAIL 1)
(SEE DETAIL 2)
(SEE DETAIL 3)
(SEE DETAIL 4)
LOAD (SEE
U14/U15
DECREMENT (PERIOD VARIES)
DISABLE COUNT
DECREMENT
U8 PIN 1
TRACE EN (VIDEO PI
U27 PIN
U27 PIN
TRACE GENERATOR OPERATION
B 12.5MH
BDE
0
1
2
3
4
5
6
7
8
9
10
U13 COUN
U27 PIN
U27 PIN
LOAD U20/U21
U27 PIN
LOAD U14/U15
U27 PIN
READ DISPLAY FIFO
U8 PIN 1
4 COUNT DELAY
DETAIL 1

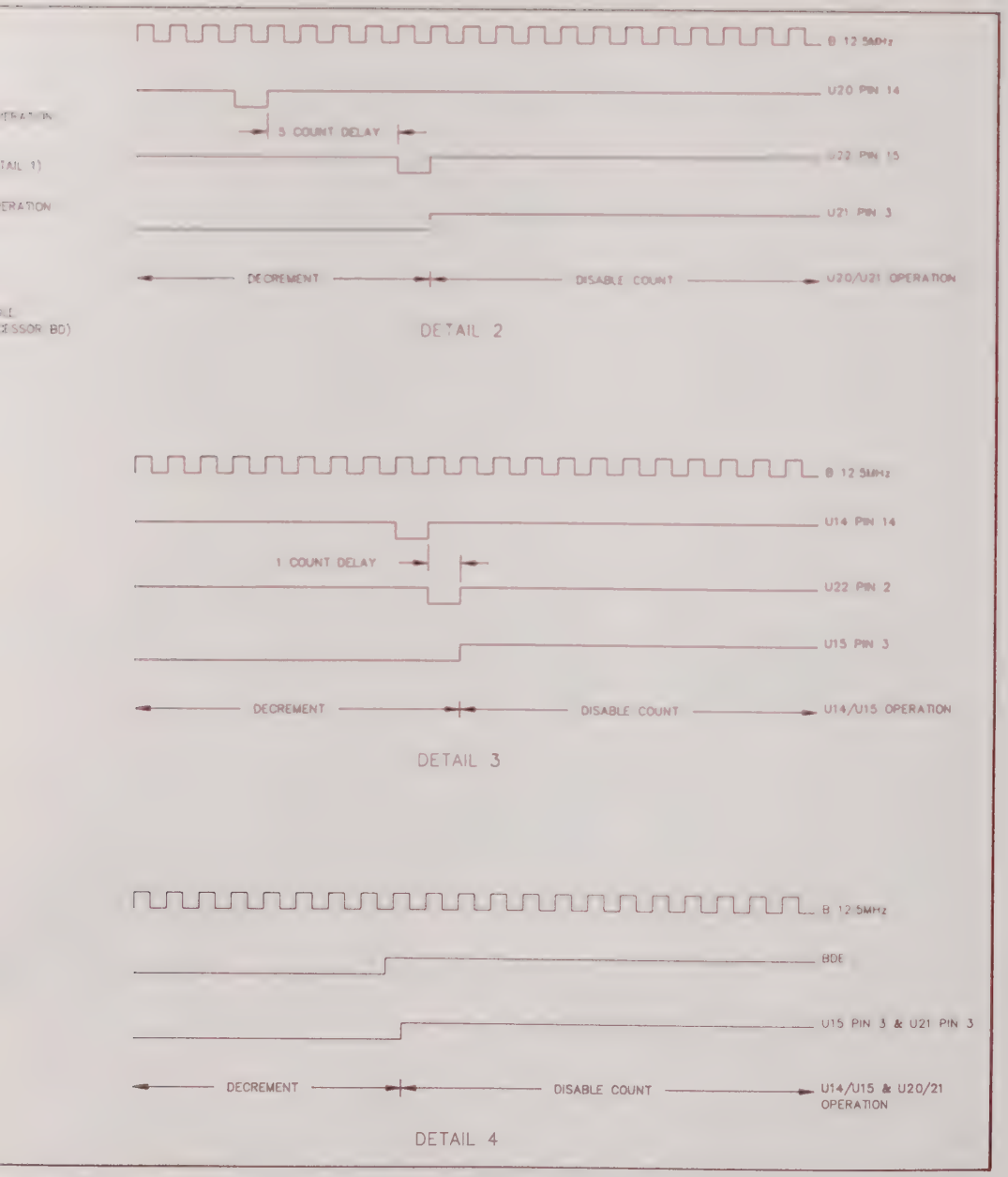
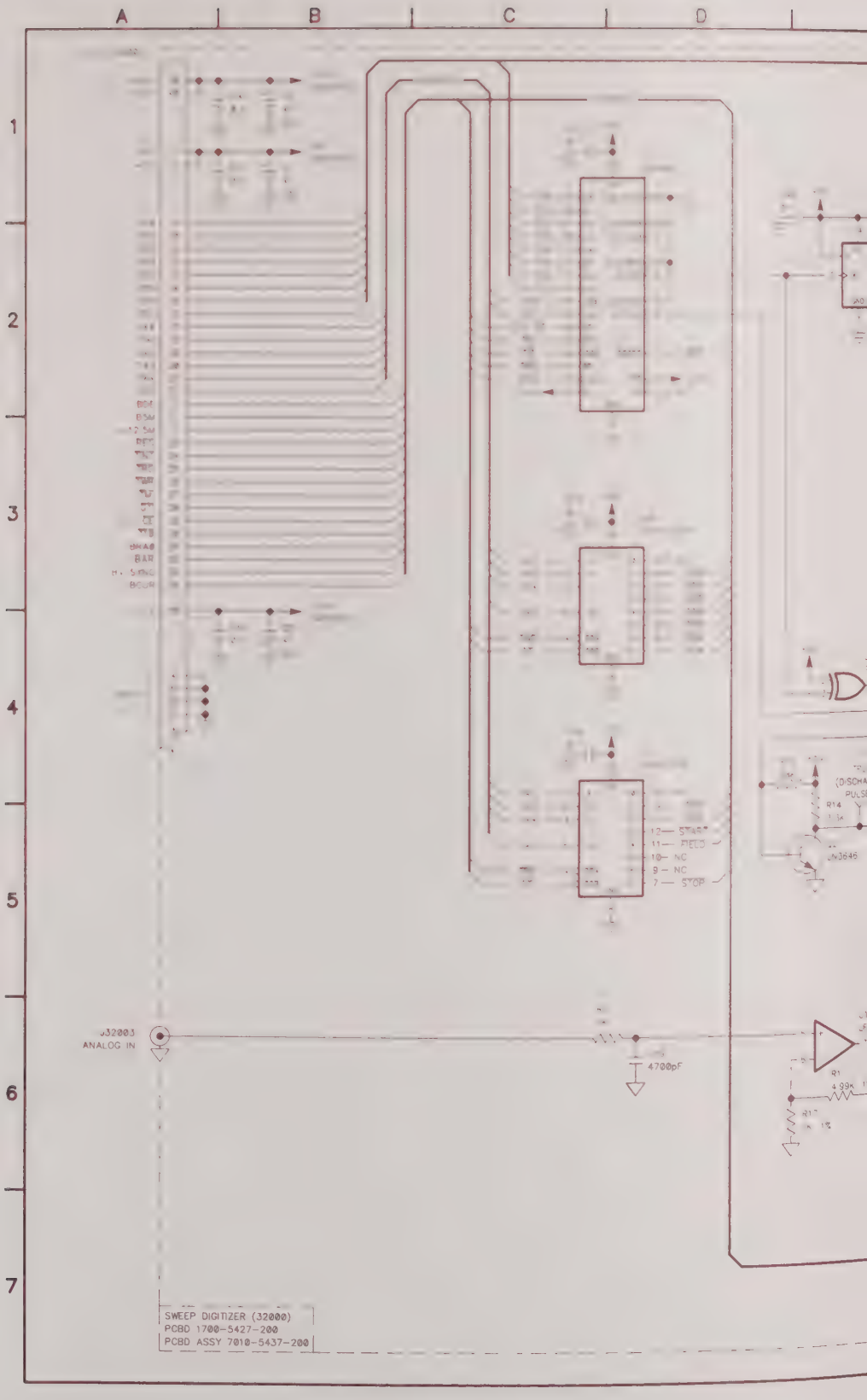
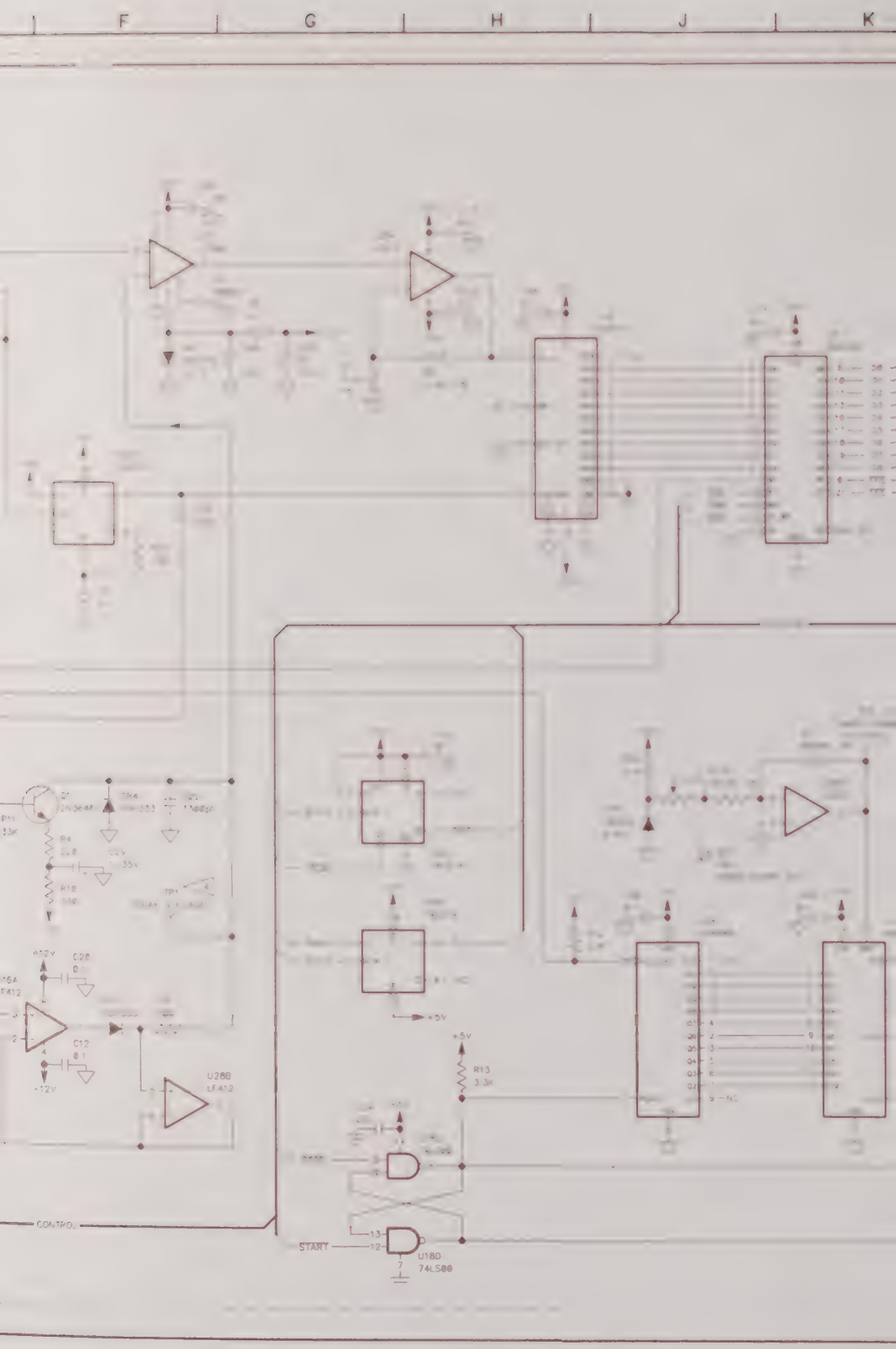
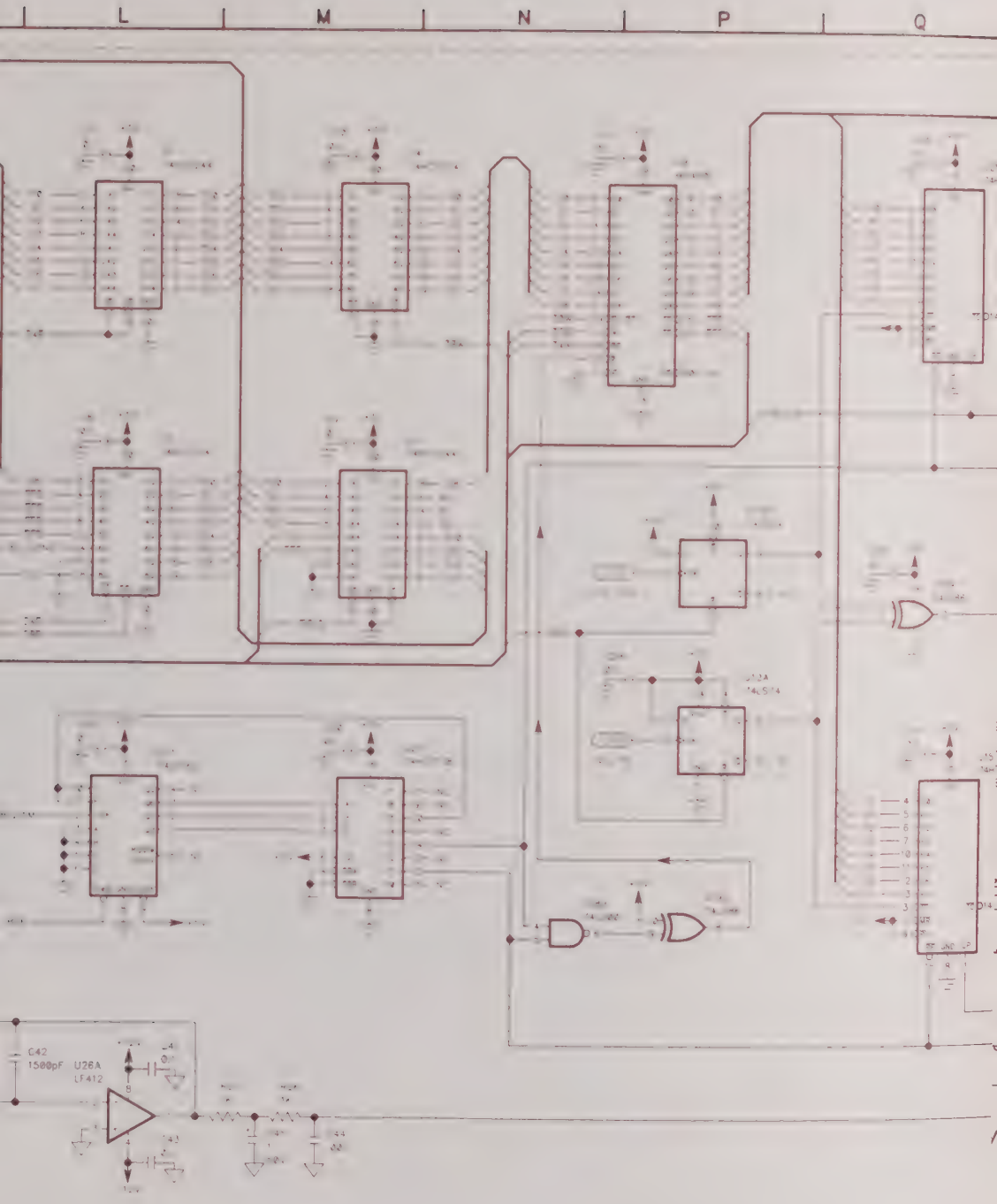
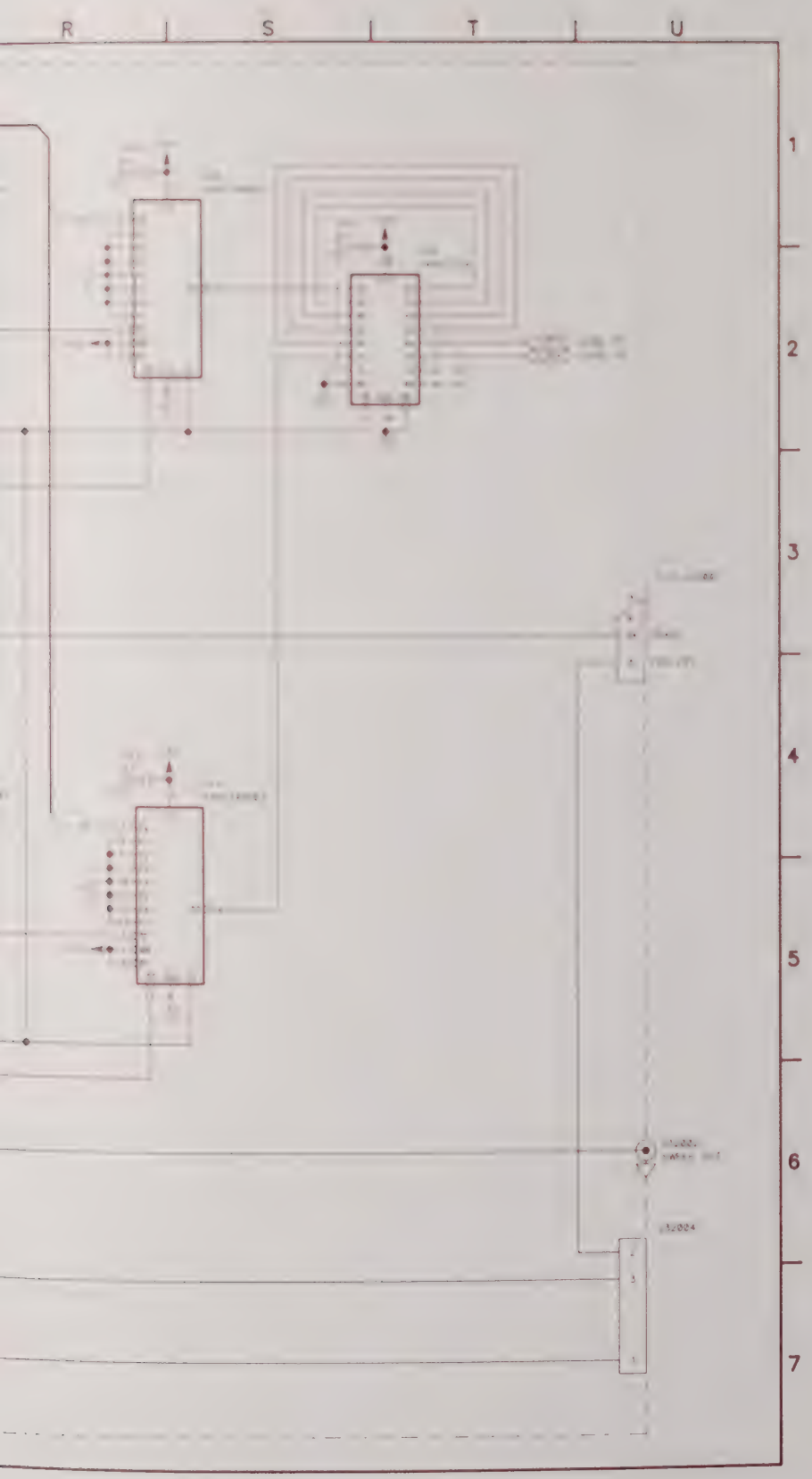


Figure 5-14 Sweep Digitizer PC Board Assembly (Sheet 1 of 2) (0000-6317-400-B)


A
B
C
D
1
2
3
4
5
6
7
J32003
ANALOG IN
4700pF
R1
4.99K
12— START
11— FIELD
10— NC
9 — NC
7 — STOP
SWEEP DIGITIZER (32000)
PCBD 1700-5427-200
PCBD ASSY 7010-5437-200


F
G
H
J
K
+5V
R13
3.3K
U28B
LF412
C12
0.1
-12V
CONTROL
START
13
12
7
U18D
74LS00


L
M
N
P
Q
C42
1500pF
U26A
LF412


R
S
T
U
1
2
3
4
5
6
7

NOTES (UNLESS OTHERWISE STATED):

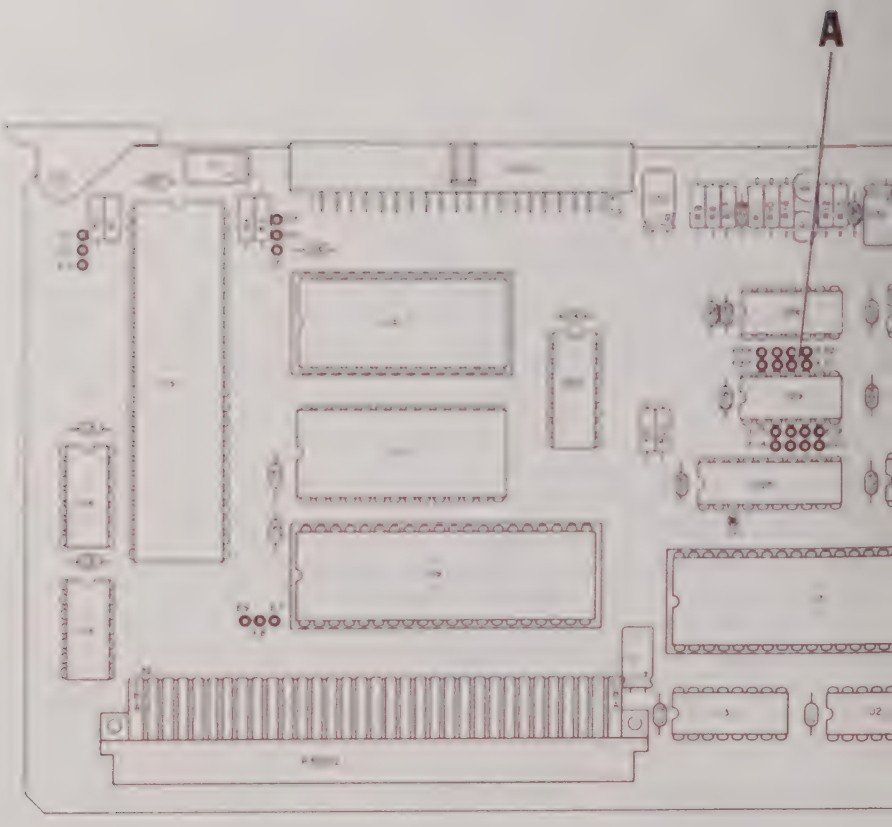
1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES: 32000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

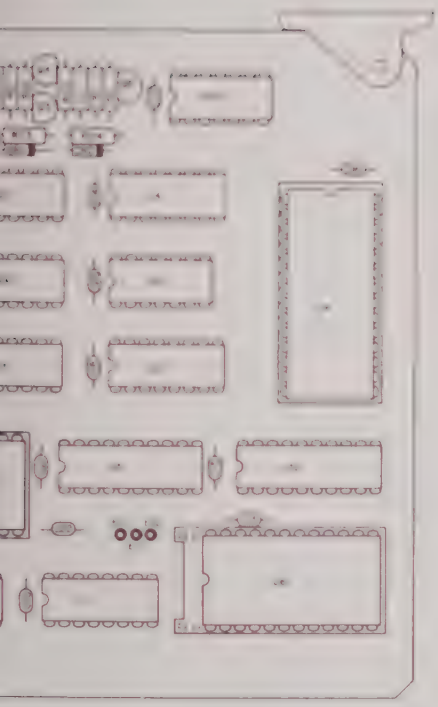
3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

4. TESTPOINT WAVEFORMS WITH 5 ms/DIV SWEEP ARE PRESENTED ON PREVIOUS PAGE.

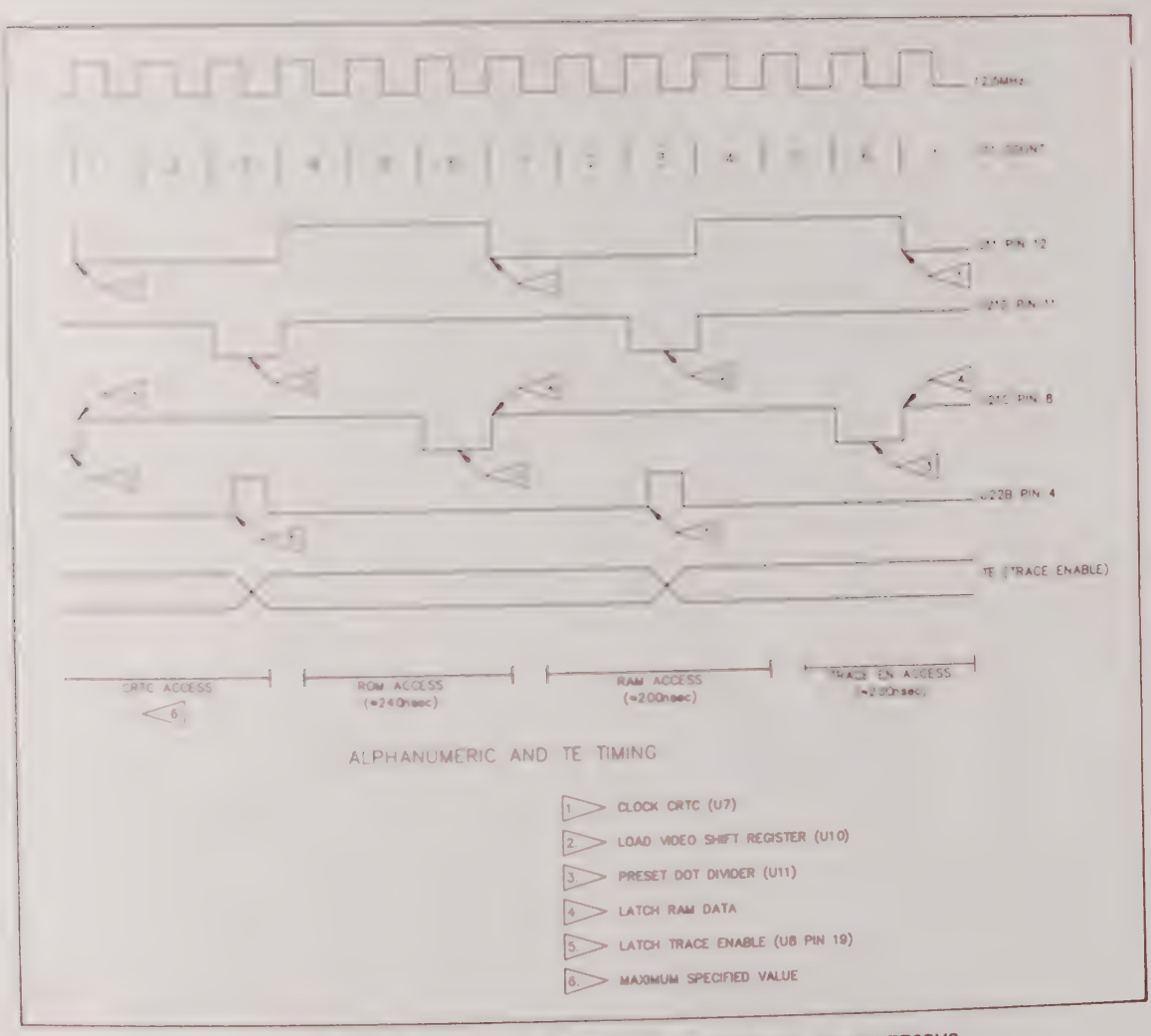
Figure 5-14 Sweep Digitizer PC Board Assembly (Sheet 2 of 2) (0000-6317-400-B)



Video Processor PC Bd As
(7010-5336-501-B4)

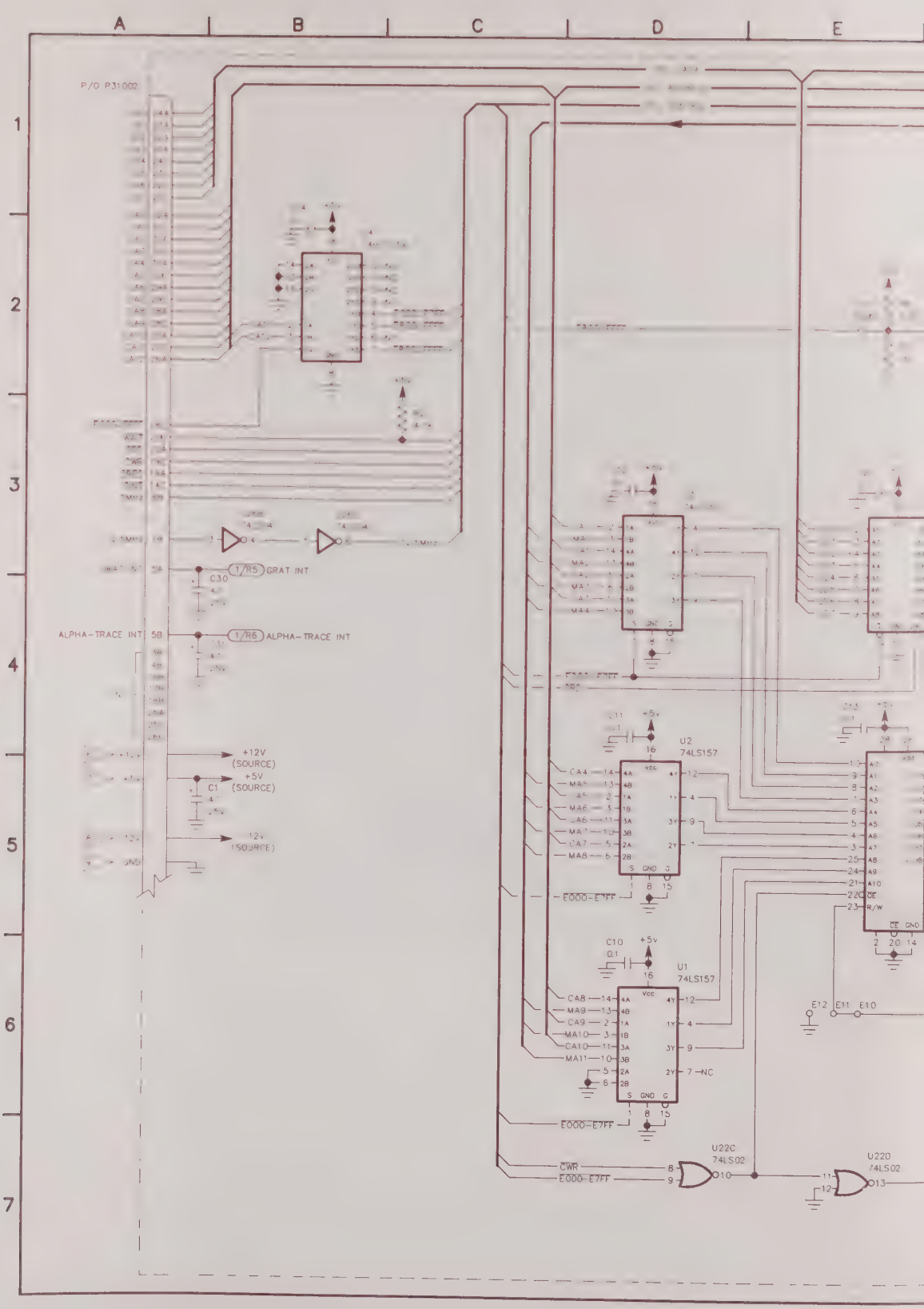


DETAIL **A**

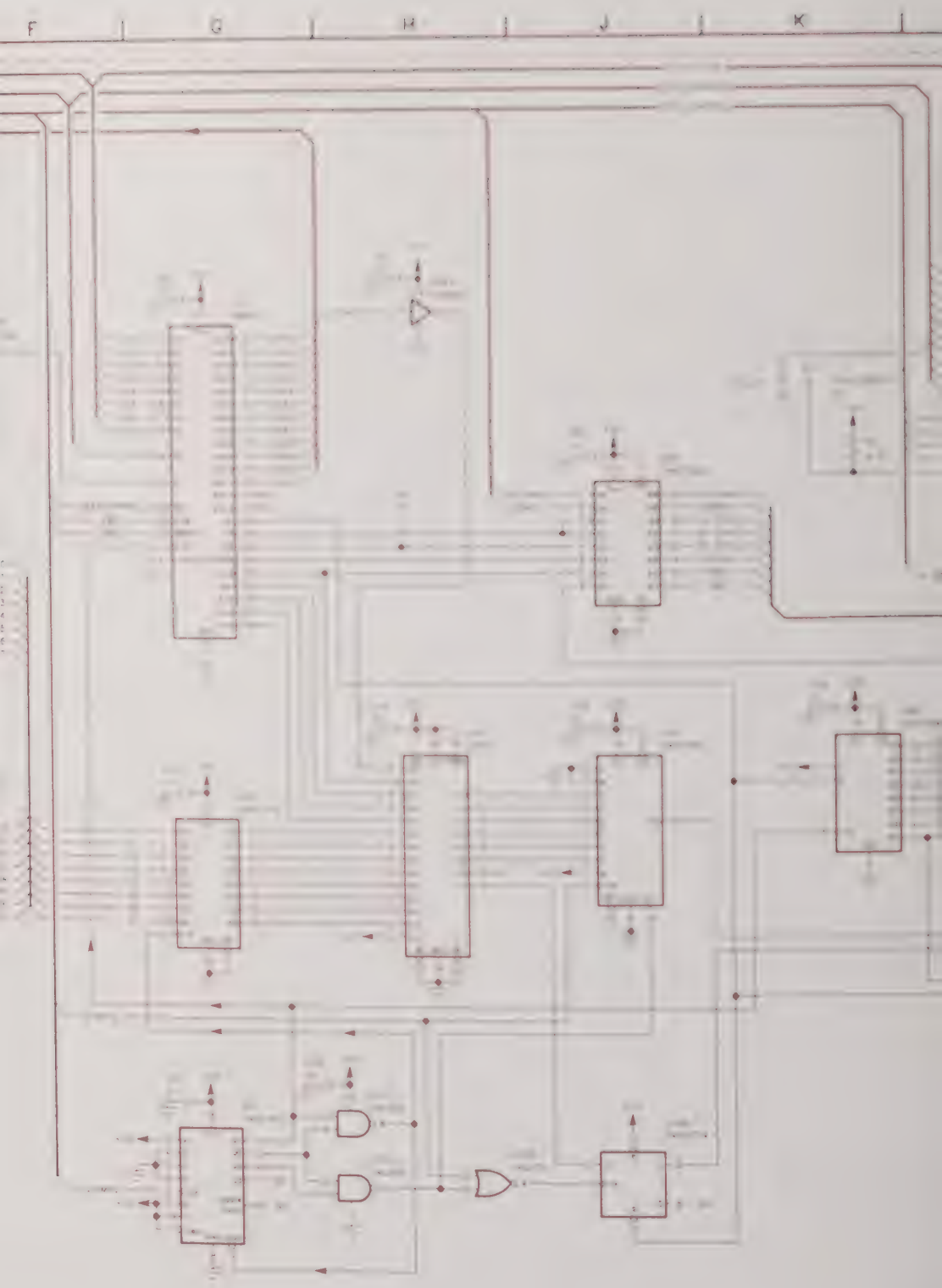


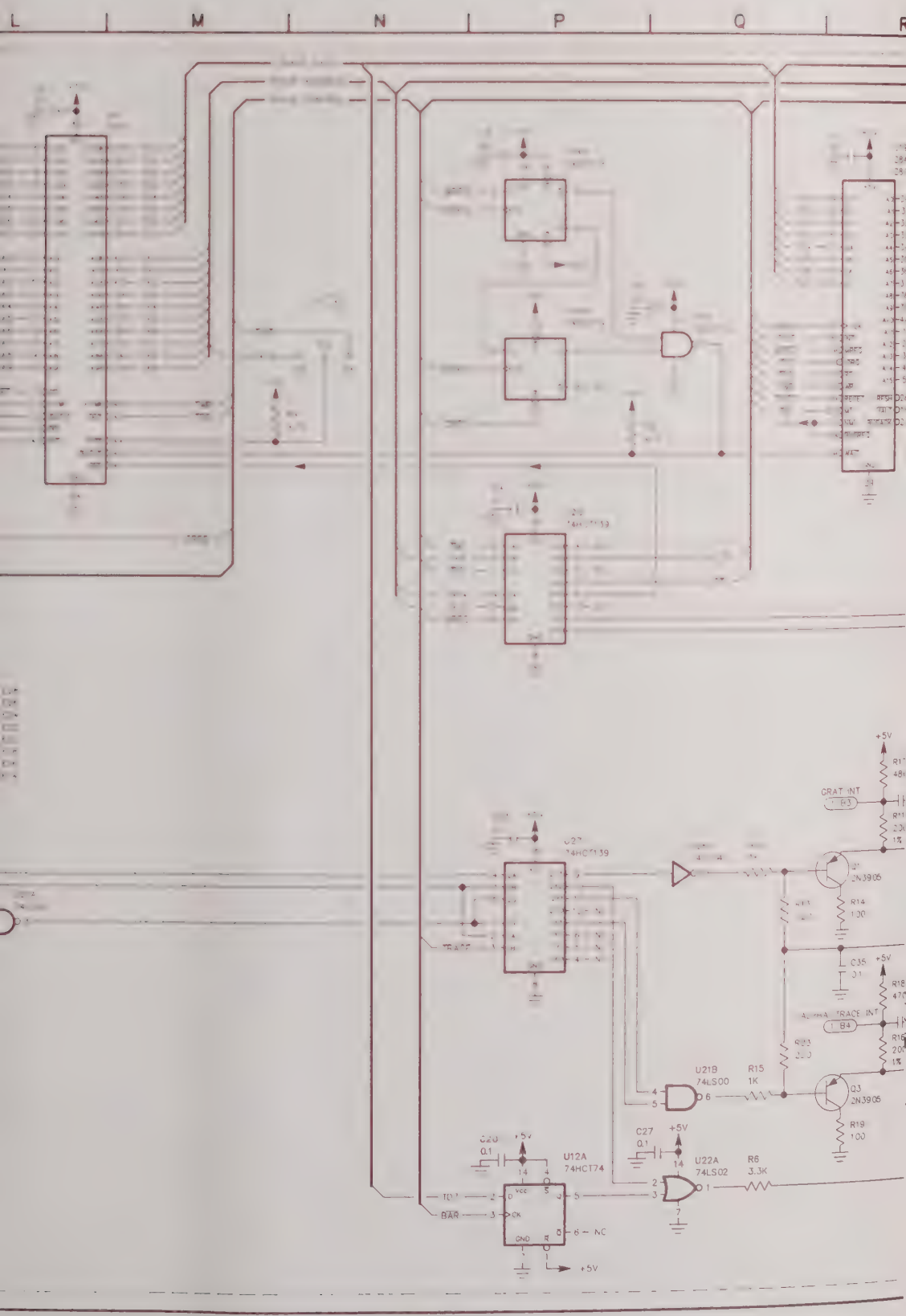
NOTE: SEE VIDEO PROCESSOR SCHEMATIC FOR SOURCES OF WAVEFORMS

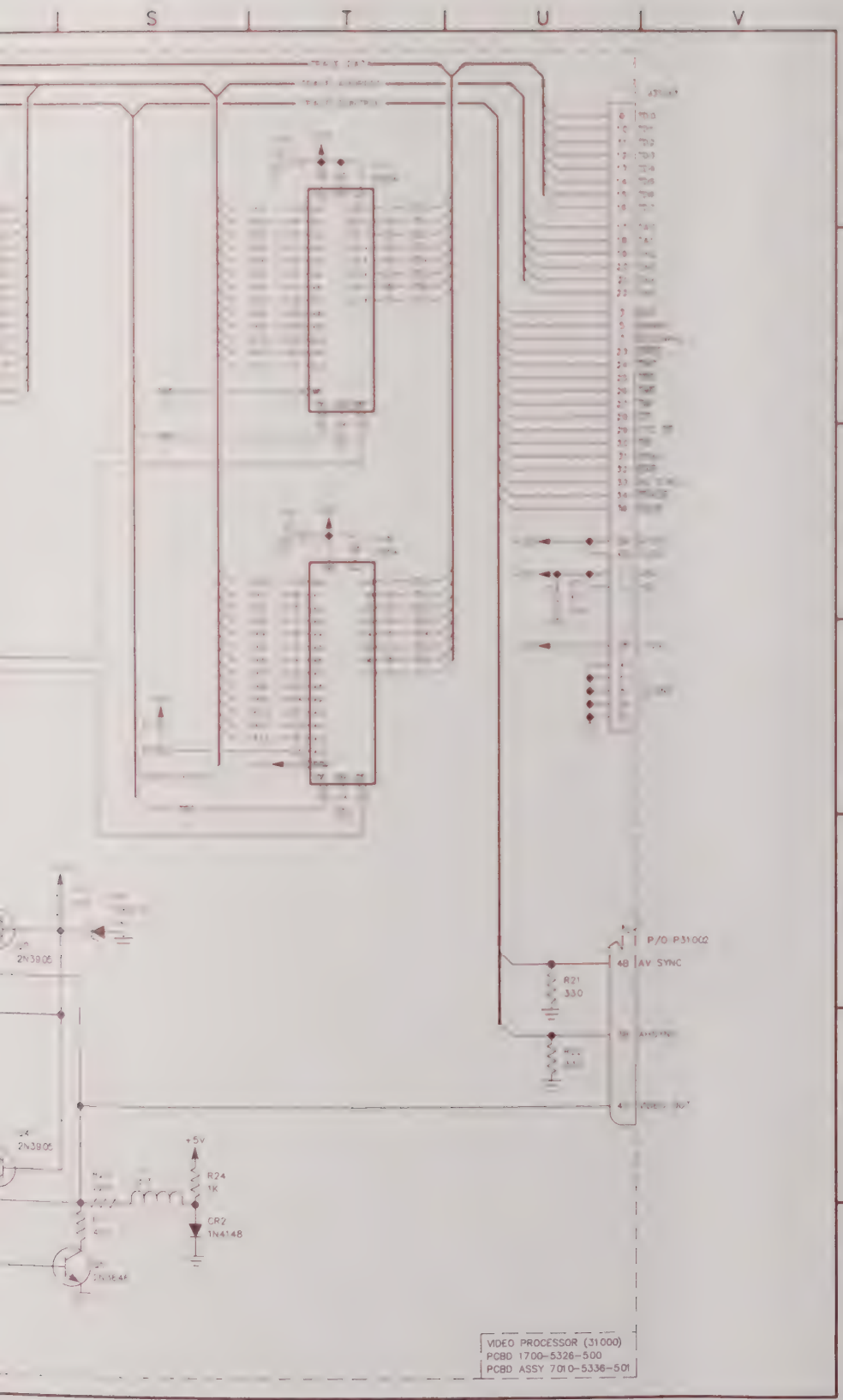
Figure 5-15 Video Processor PC Board Assembly (Sheet 1 of 2) (0000-5316-501-B1)



A
B
C
D
E
1
2
3
4
5
6
7
P/O P31002
1/R5 GRAT INT
C30
ALPHA-TRACE INT 5B
1/R6 ALPHA-TRACE INT
+12V (SOURCE)
+5V (SOURCE)
C1
U2
74LS157
U1
74LS157
C10
0.1
+5V
E000-E7FF
CWR
U22C
74LS02
U22D
74LS02
E12
E11
E10


F
G
H
J
K


L
M
N
P
Q
R
+5V
GRAT INT
1 B3
2N3905
R14
100
C35
0.1
TRACE INT
1 B4
U21B
74LS00
R15
1K
Q3
2N3905
R19
100
C27
0.1
U22A
74LS02
R6
3.3K
U12A
74HCT74
TD7
BAR
NC
GND
+5V


S
T
U
V
1
2
3
4
5
6
7
P/O P31002
48 AV SYNC
R21
330
2N3906
2N3906
+5V
R24
1K
CR2
1N4148
VIDEO PROCESSOR (31000)
PCBD 1700-5326-500
PCBD ASSY 7010-5336-501

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES: 31000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

4. FOR ENGINEERING USE ONLY.

5. U6 IS A 24-PIN IC INSTALLED IN A 28-PIN SOCKET. PIN NUMBERS ARE RELATIVE TO THE SOCKET (E.G., PIN 3 OF THE SOCKET IS PIN 1 OF THE 24-PIN IC).

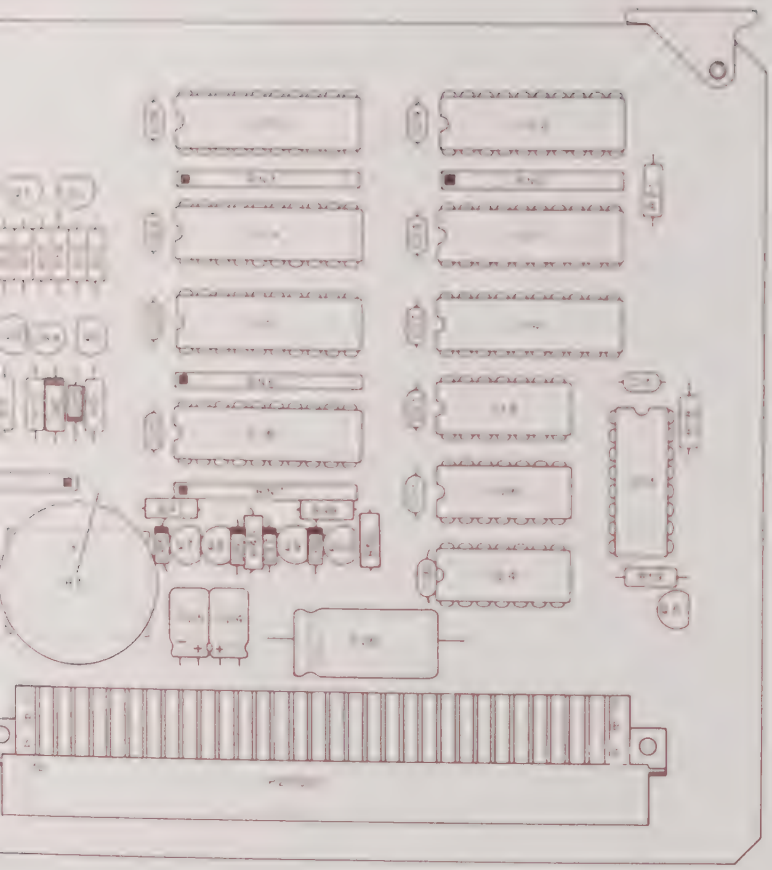
6. FOR P31002, THE FOLLOWING PIN NUMBERS ARE +12V: 10A, 10B, 10C, 11A, 11B, 11C.

7. FOR P31002, THE FOLLOWING PIN NUMBERS ARE +5V: 12A, 12B, 12C, 13A, 13B, 13C.

8. FOR P31002, THE FOLLOWING PIN NUMBERS ARE -12V: 8A, 8B, 8C, 9A, 9B, 9C.

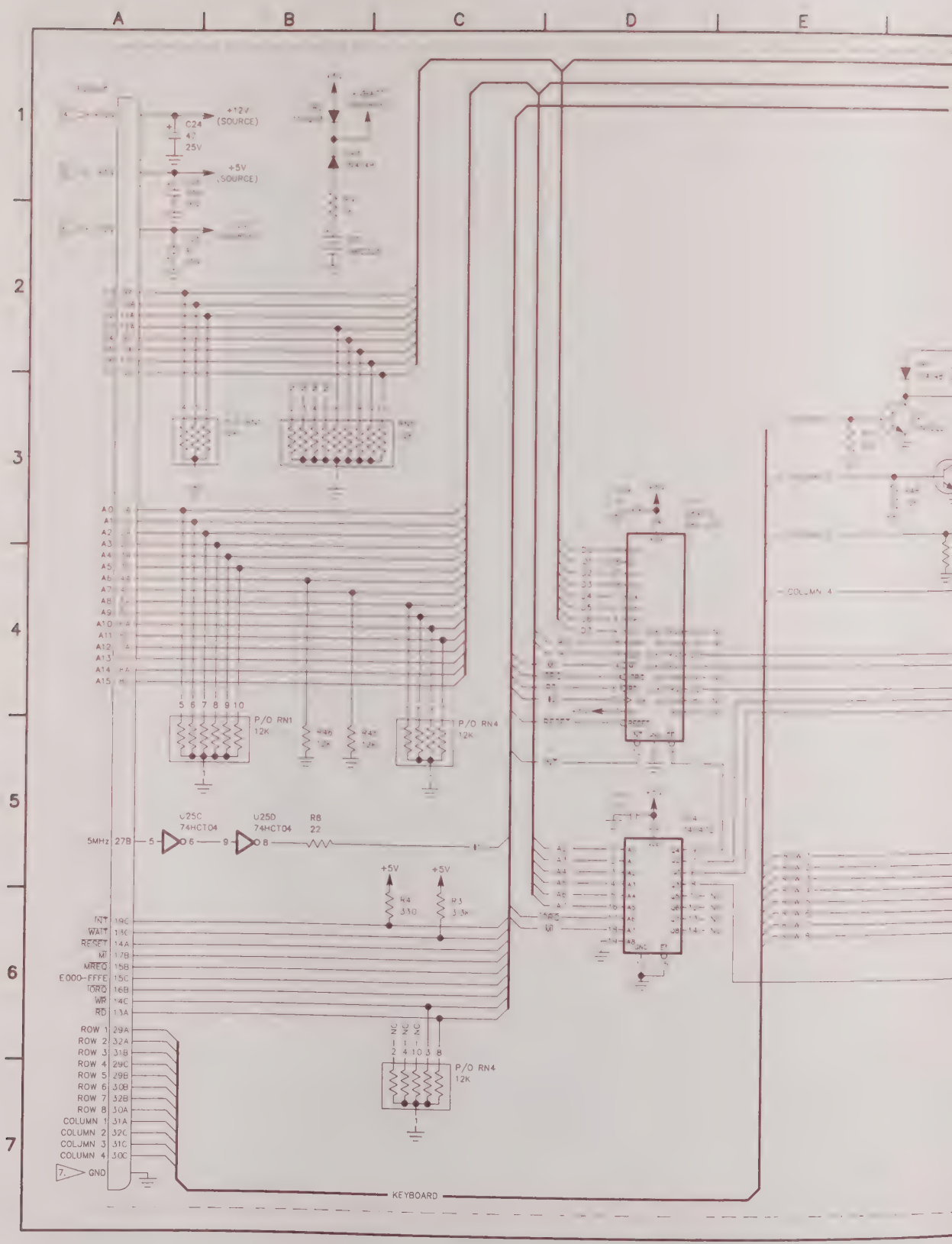
9. FOR P31002, THE FOLLOWING PIN NUMBERS ARE GND: 1A, 1C, 2A, 2B, 2C, 3A, 3B, 3C, 4A, 4B, 5C, 6A, 6C, 7A, 7B, 7C, 14A, 14B, 15A, 15B, 15C, 16A, 16C, 17A, 17C, 18A, 19B THRU 32B (B ONLY).

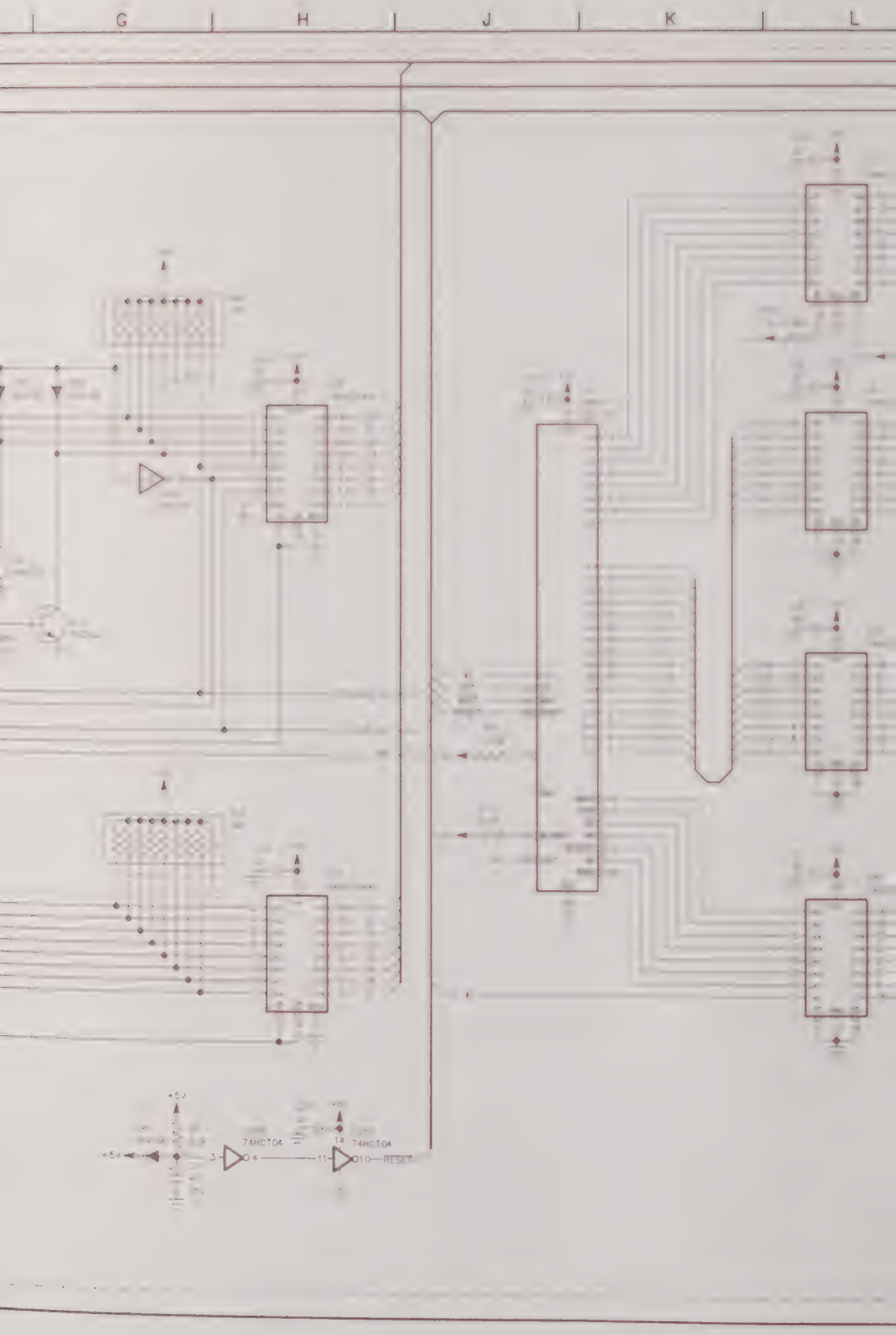
Figure 5-15 Video Processor PC Board Assembly (Sheet 2 of 2) (0000-5316-501-B1)

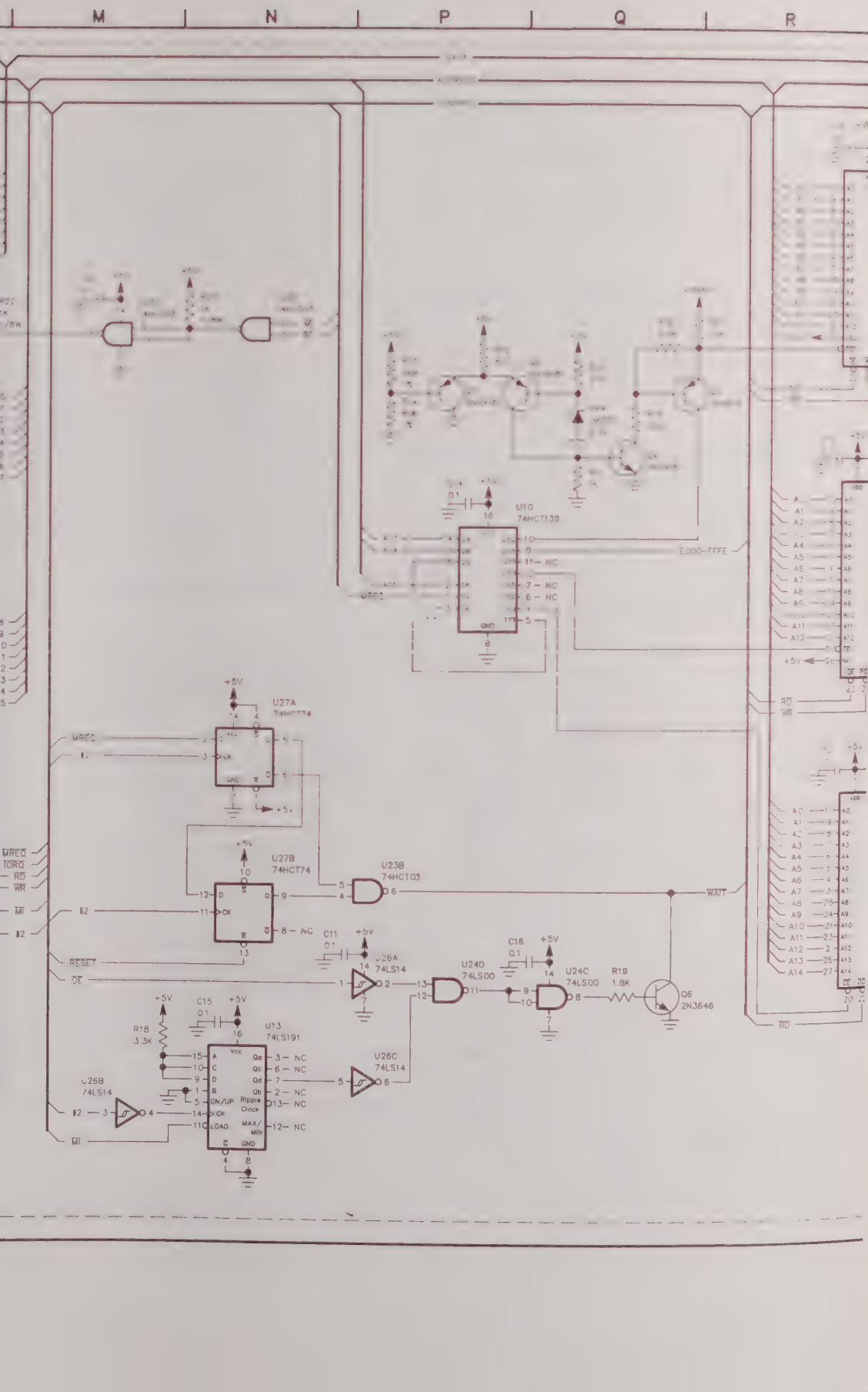


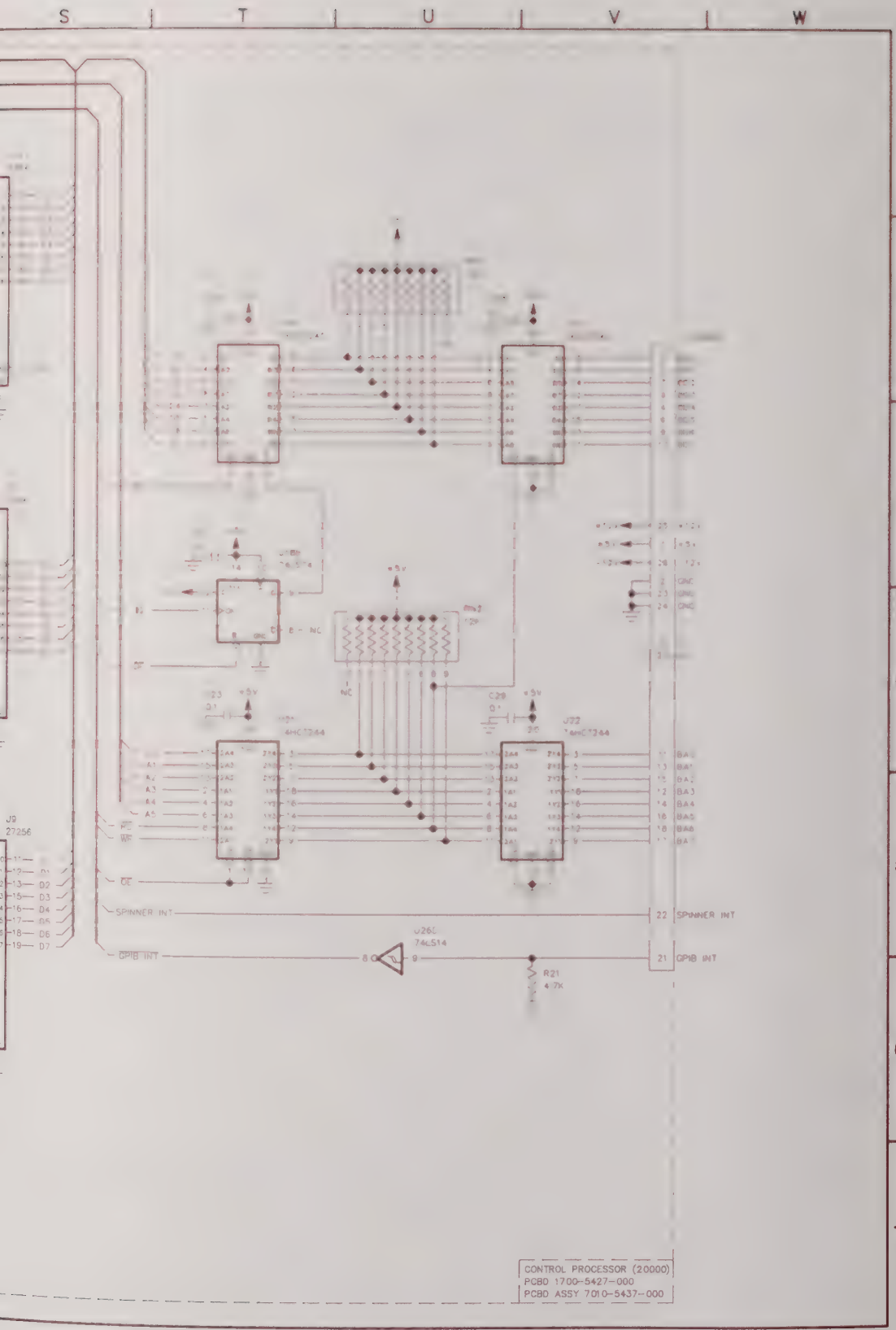
010-5336-601-C3)

Figure 5-16 Processor PC Board Assembly (Sheet 1 of 2)
(0000-5316-601-C)


A
B
C
D
E
1
2
3
4
5
6
7
+12V (SOURCE)
C24
47
25V
+5V (SOURCE)
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
5 6 7 8 9 10
P/O RN1
12K
P/O RN4
12K
U25C
74HCT04
U25D
74HCT04
R8
22
5MHz
27B
+5V
+5V
R4
330
R3
3.3K
INT 19C
WAIT 13C
RESET 14A
M1 17B
MREQ 15B
E000-FFFE 15C
IORQ 16B
WR 14C
RD 13A
ROW 1 29A
ROW 2 32A
ROW 3 31B
ROW 4 29C
ROW 5 29B
ROW 6 30B
ROW 7 32B
ROW 8 30A
COLUMN 1 31A
COLUMN 2 32C
COLUMN 3 31C
COLUMN 4 30C
GND
NC NC NC
1 2 4 10 3 8
P/O RN4
12K
COLUMN 4
KEYBOARD


G
H
J
K
L
+5V
74HCT04
74HCT04
RESET


M
N
P
Q
R
U10
74HCT139
E000-FFFE
U27A
74HCT74
U27B
74HCT74
U23B
74HCT03
WAIT
C11
0.1
U26A
74LS14
U24D
74LS00
C16
0.1
U24C
74LS00
R19
1.8K
Q6
2N3646
R18
3.3K
C15
0.1
U13
74LS191
U26C
74LS14
U26B
74LS14
MREQ
IORQ
RD
WR
MI
RESET
OE
+5V
NC


S
T
U
V
W
1
2
3
4
5
6
7
SPINNER INT
GPIB INT
R21
4.7K
CONTROL PROCESSOR (20000)
PCBD 1700-5427-000
PCBD ASSY 7010-5437-000

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES: 20000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

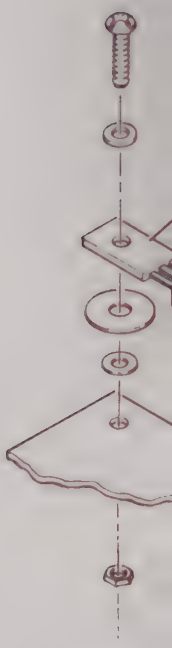
4. FOR P20001, THE FOLLOWING PIN NUMBERS ARE +12V: 22A, 22B, 22C, 23A, 23B, 23C.

5. FOR P20001, THE FOLLOWING PIN NUMBERS ARE +5V: 20A, 20B, 20C, 21A, 21B, 21C.

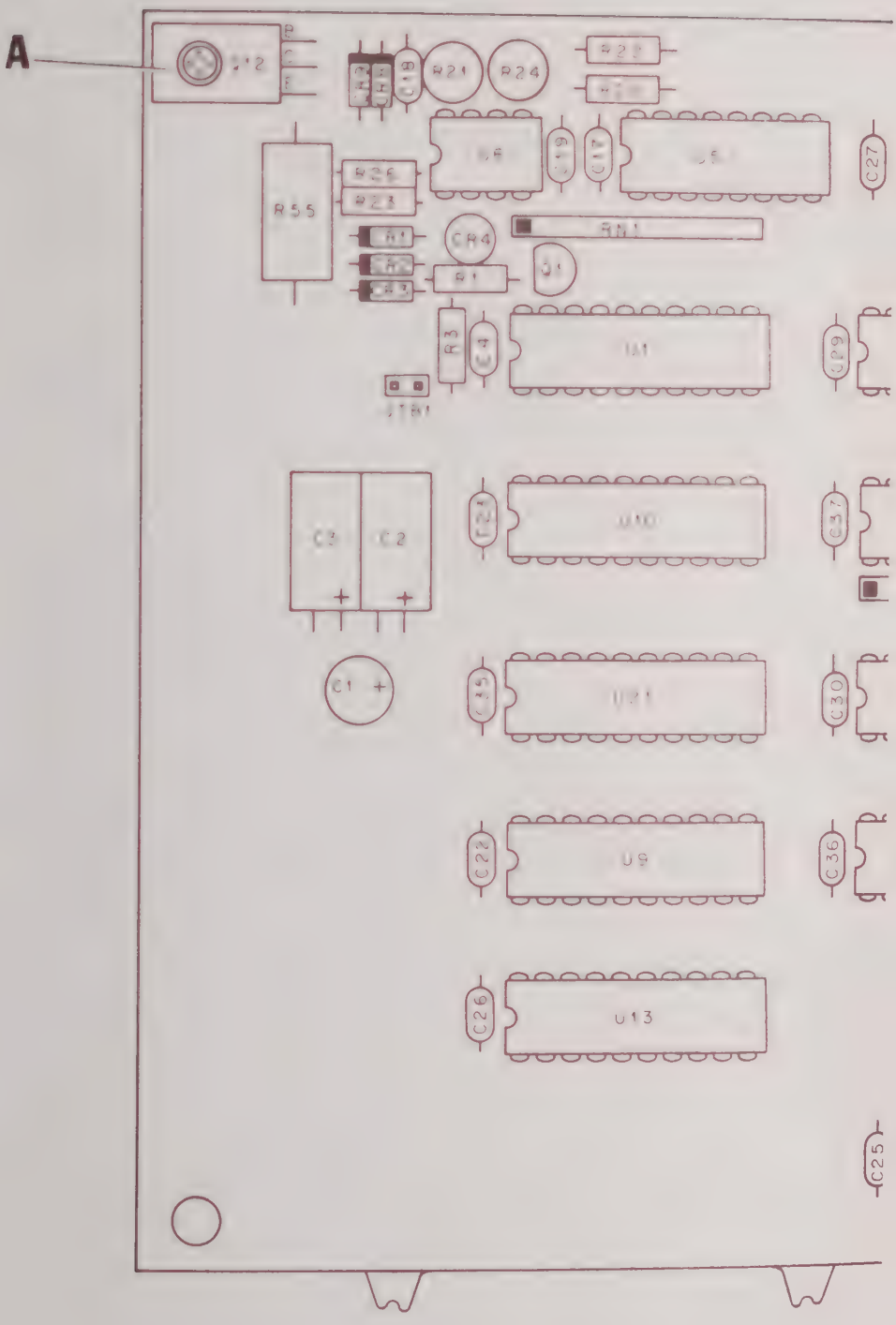
6. FOR P20001, THE FOLLOWING PIN NUMBERS ARE -12V: 24A, 24B, 24C, 25A, 25B, 25C.

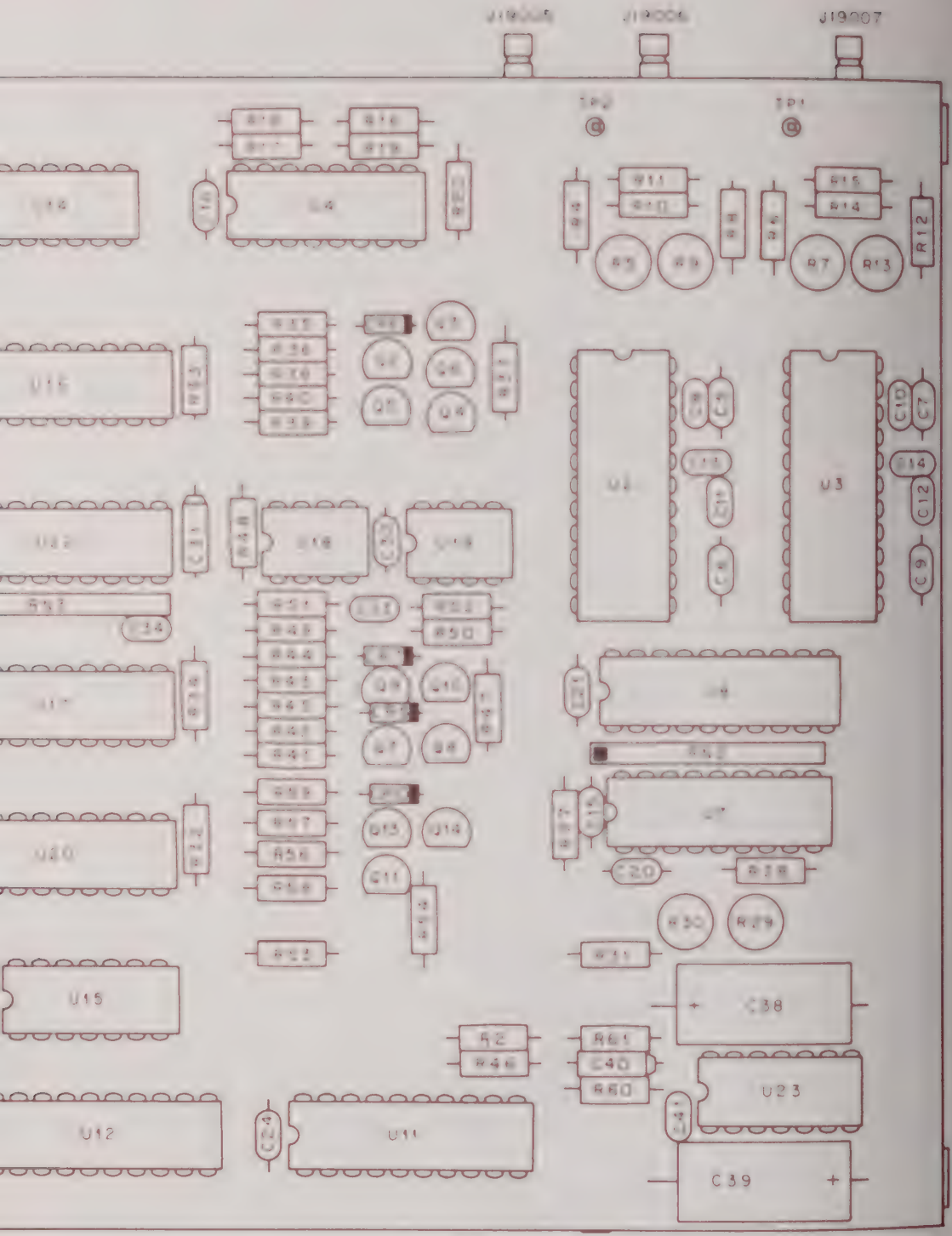
7. FOR P20001, THE FOLLOWING PIN NUMBERS ARE GND: 1B THRU 14B (B ONLY), 15A THRU 19A (A ONLY), 16C, 17C, 18B, 18C, 19B, 26A, 26C, 27A, 27C, 28A, 28B, 28C.

Figure 5-16 Processor PC Board Assembly (Sheet 2 of 2) (0000-5316-601-C)



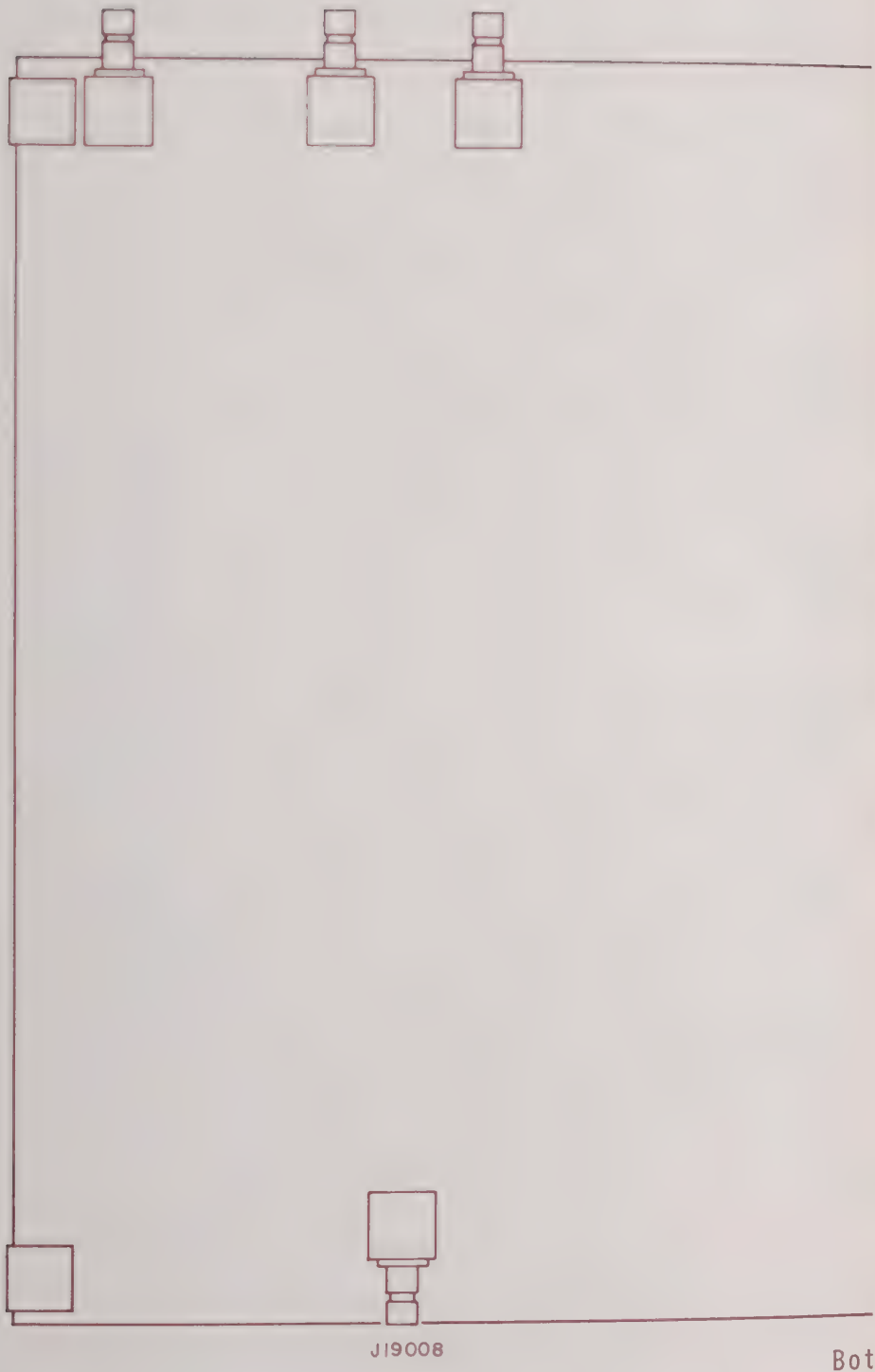
DETAIL


A
R21
R24
R55
R26
R23
CR4
R1
R3
C4
C27
C29
C3
C2
C1
C37
C30
C36
C26
C25
U9
U13



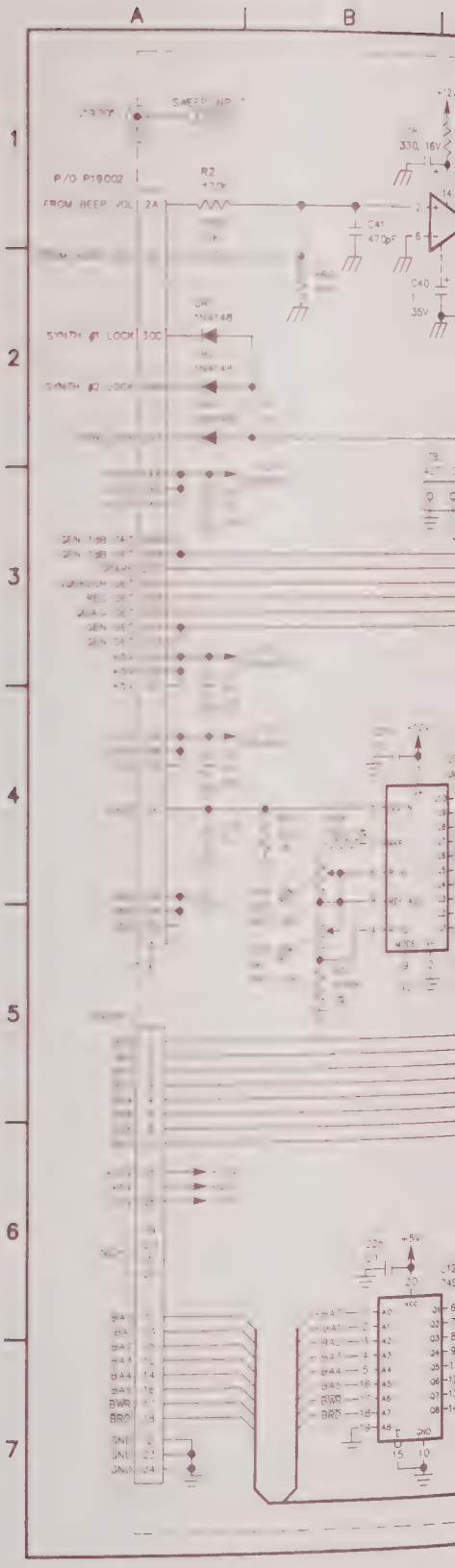
Top View

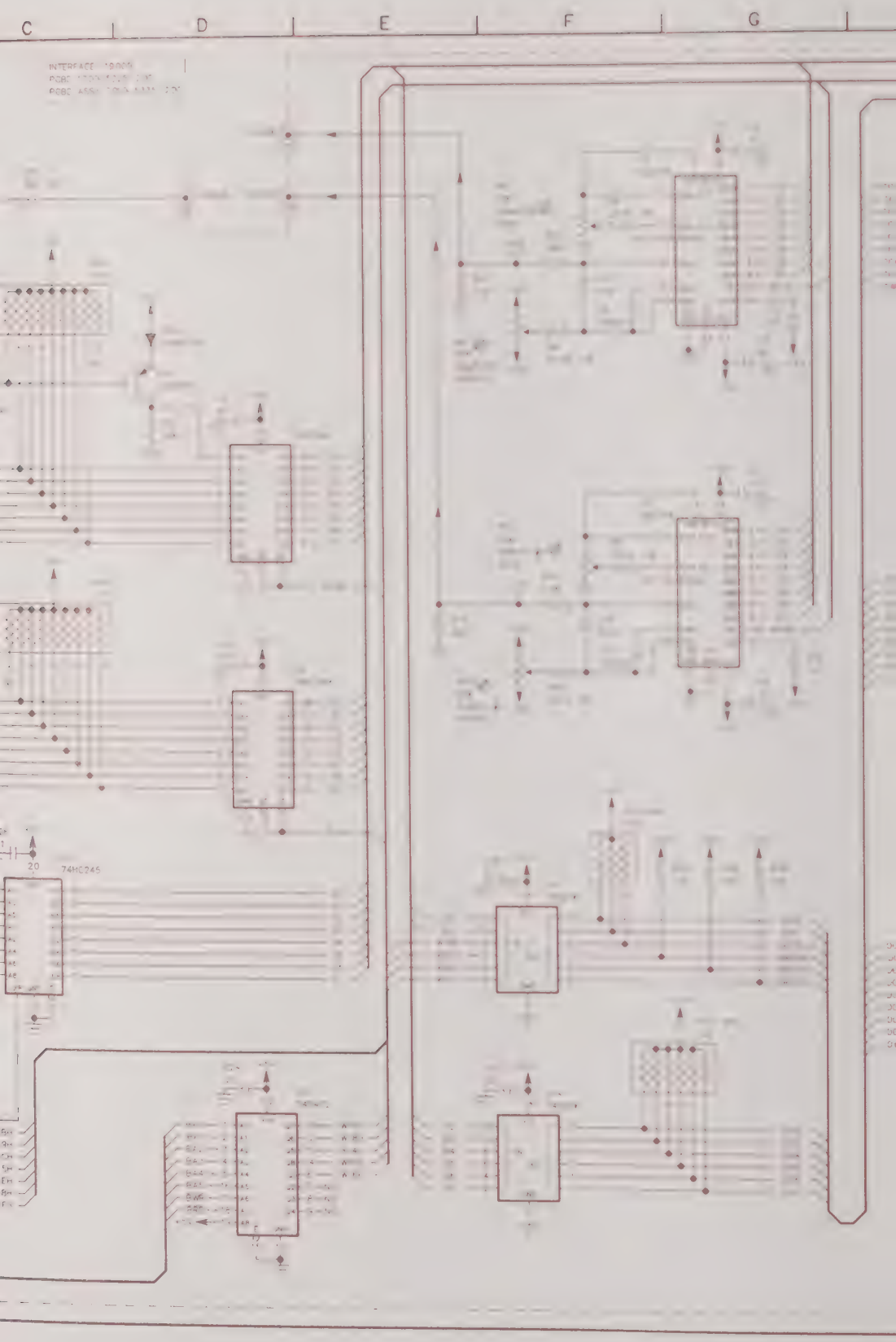
Interface PC B



d Assy (7010-5335-200-C6)

Figure 5-17 Interface PC Bd Assembly
(Sheet 1 of 2) (0000-5315-200-C2)


A
B
1
2
3
4
5
6
7
SWEEP IND
330, 16V
P/O P19002
R2
FROM BEEP VOL
C41
470pF
C40
35V
SYNTH #1 LOCK
SYNTH #2 LOCK
1N4148
+5V
GND


C
D
E
F
G
74HC245

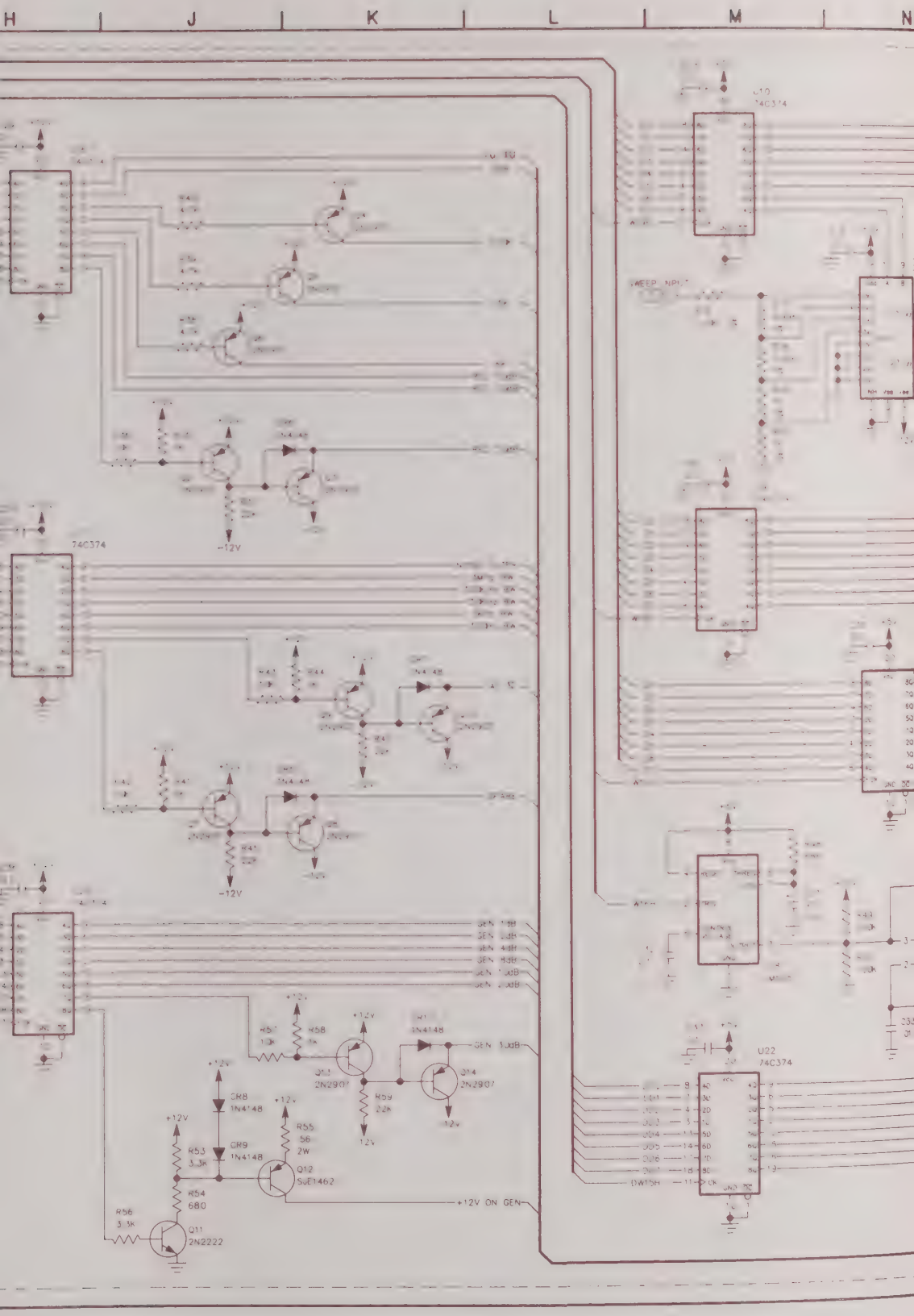
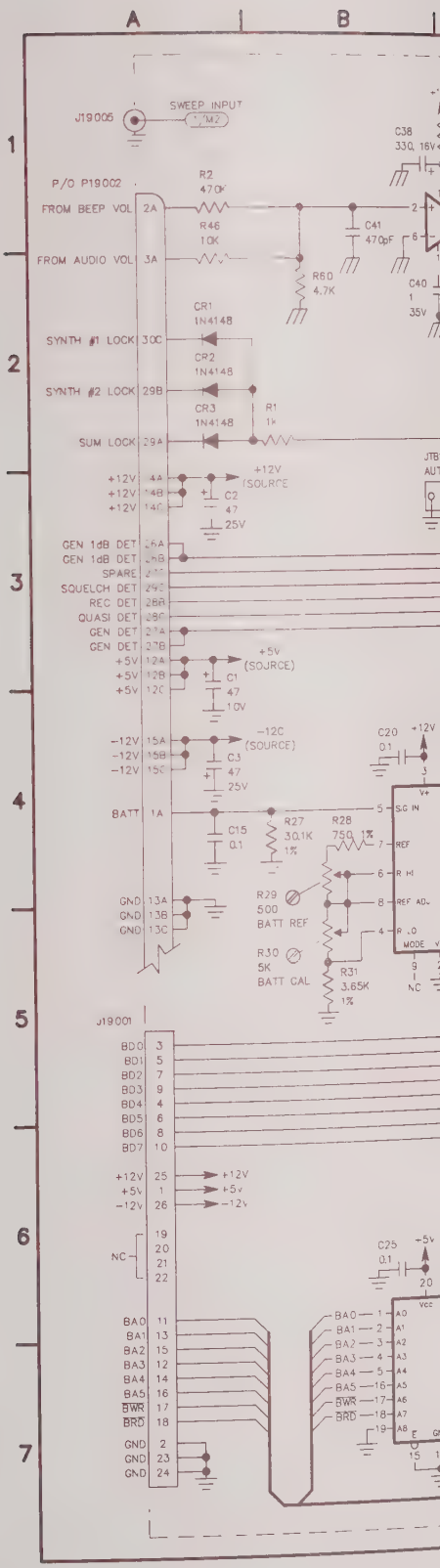
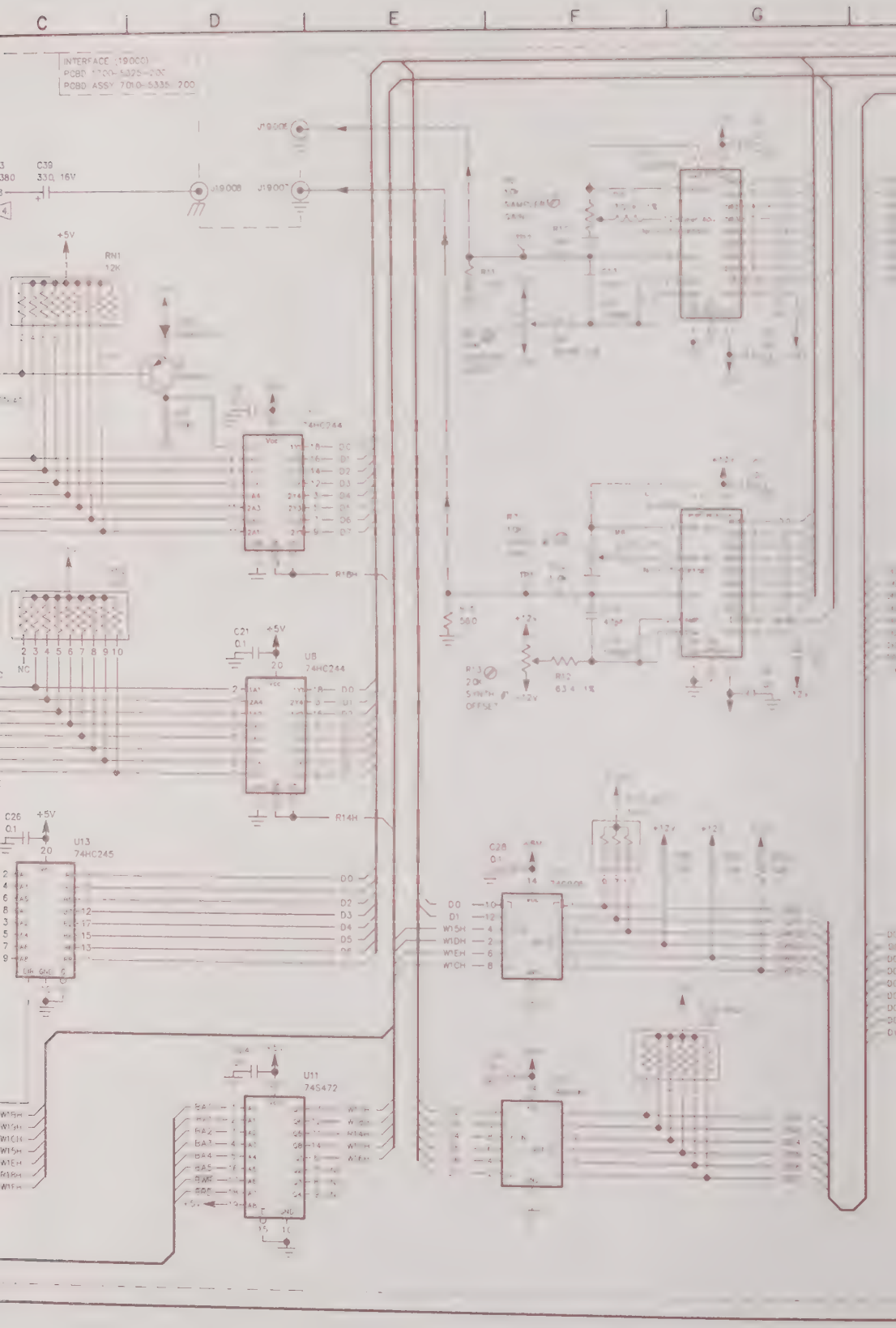
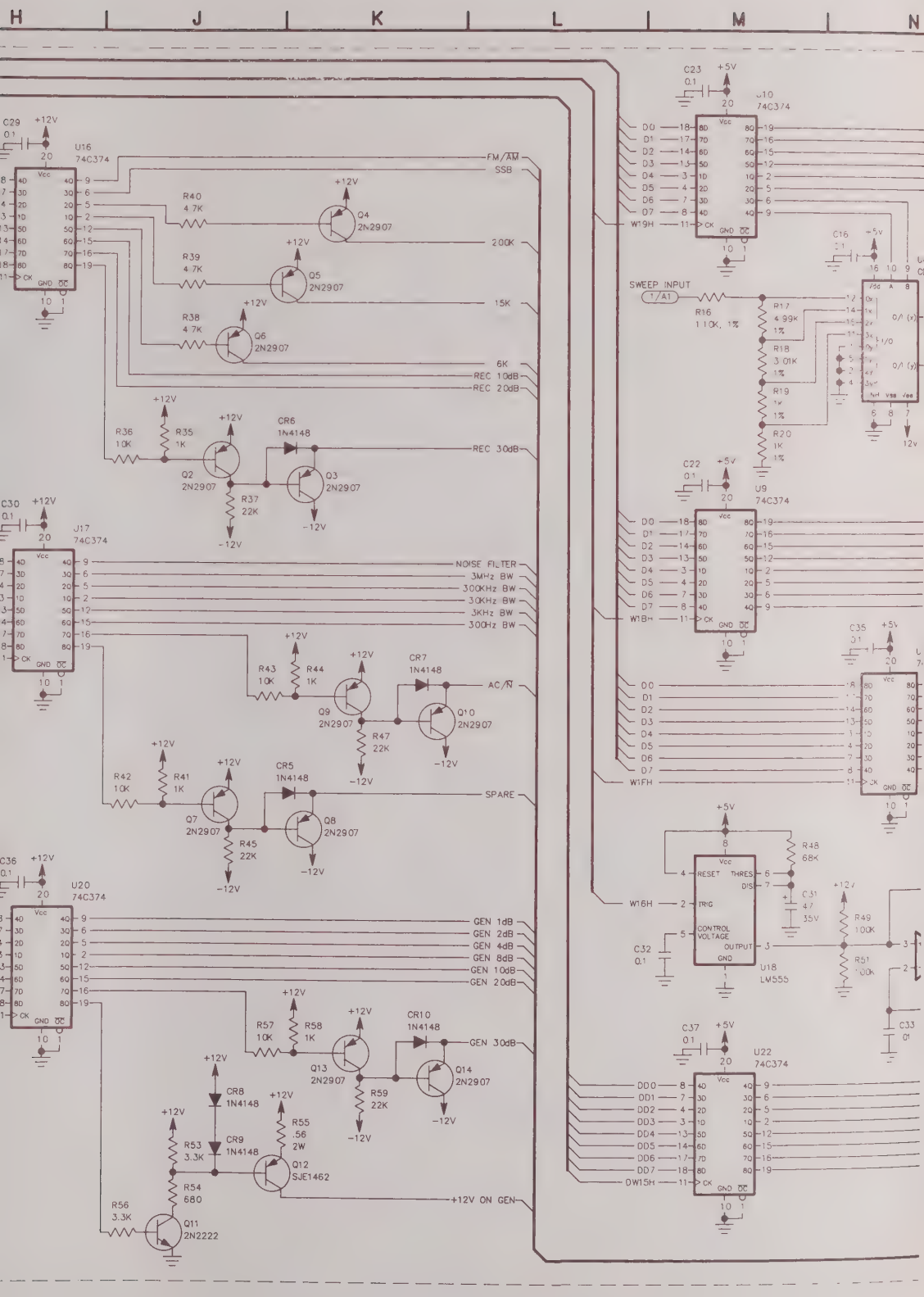
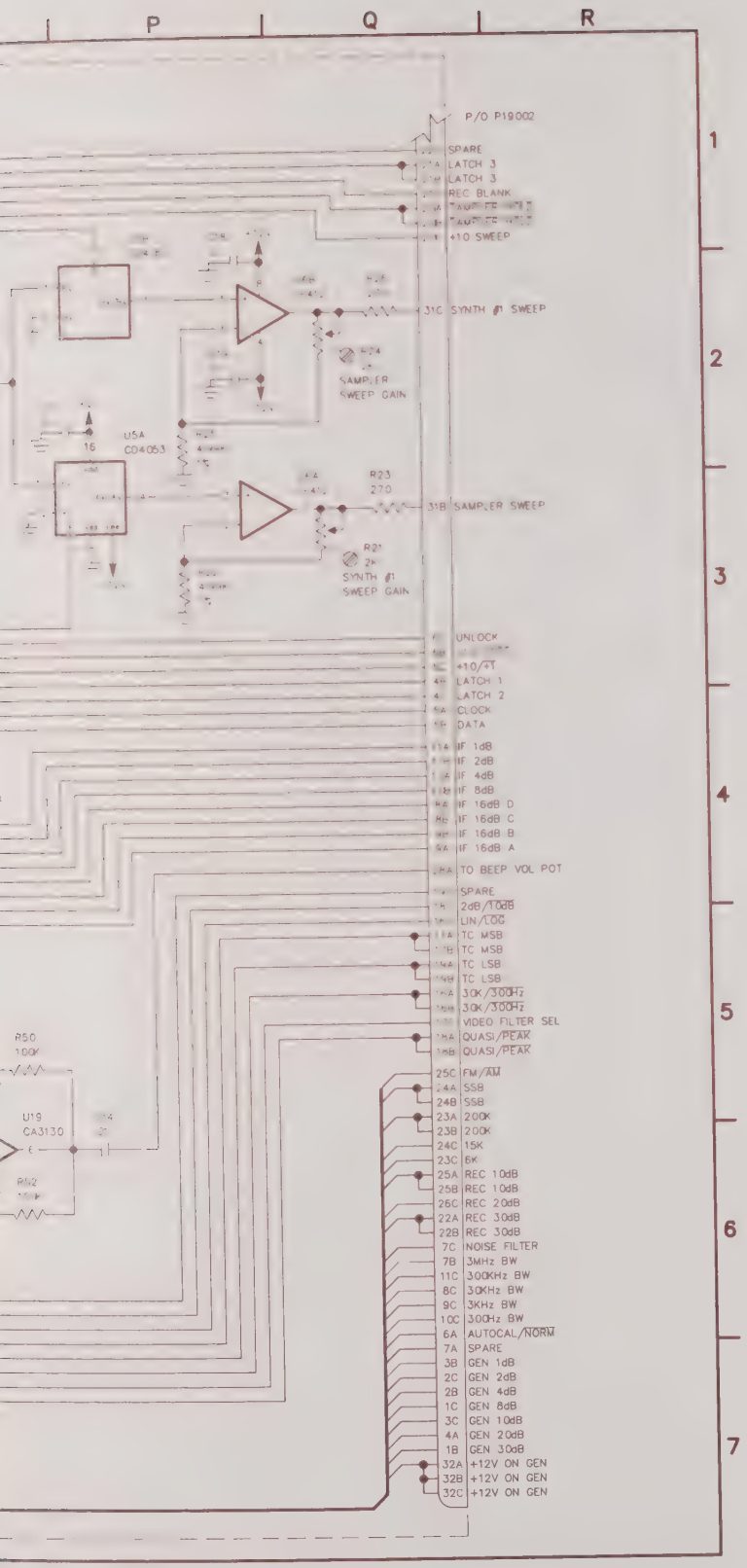

H
J
K
L
M
N
74C374
-12V
-12V
GEN 1dB
GEN 2dB
GEN 4dB
GEN 8dB
GEN 10dB
GEN 20dB
+12V
R57
10k
R58
1k
Q13
2N2907
R59
22k
CR1
1N4148
GEN 30dB
Q14
2N2907
CR8
1N4148
CR9
1N4148
R55
56
2W
Q12
SUE1462
R53
3.3k
R54
680
R56
3.3k
Q11
2N2222
+12V ON GEN
U10
74C374
SWEEP INPUT
U22
74C374
DW15H

Figure 5-17 Interface PC Bd Assembly
(Sheet 1 of 2) (0000-5315-200-C2)

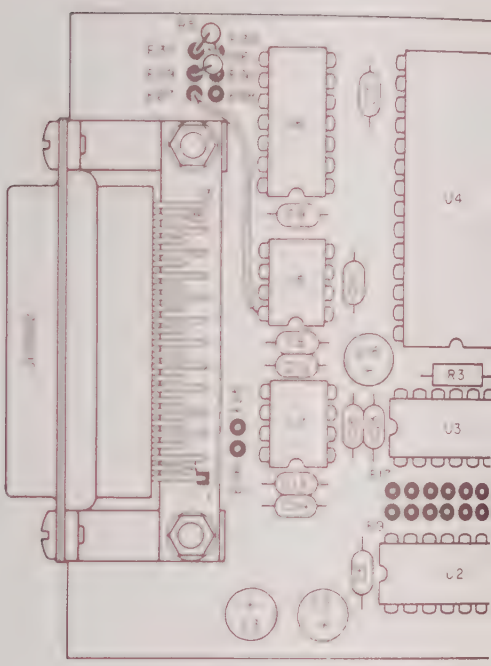

A
B
1
2
3
4
5
6
7
J19006
SWEEP INPUT
P/O P19002
FROM BEEP VOL 2A
FROM AUDIO VOL 3A
R2 470K
R46 10K
R60 4.7K
C41 470pF
C38 330, 16V
C40 35V
CR1 1N4148
CR2 1N4148
CR3 1N4148
R1 1K
SYNTH #1 LOCK 30C
SYNTH #2 LOCK 29B
SUM LOCK 29A
+12V 4A
+12V 14B
+12V 14C
+12V (SOURCE)
C2 47 25V
GEN 1dB DET 26A
GEN 1dB DET 26B
SPARE 27C
SQUELCH DET 24B
REC DET 28A
QUASI DET 28C
GEN DET 27A
GEN DET 27B
+5V 12A
+5V 12B
+5V 12C
+5V (SOURCE)
C1 47 10V
-12V 15A
-12V 15B
-12V 15C
-12C (SOURCE)
C3 47 25V
BATT 1A
C15 0.1
R27 30.1K 1%
R28 750 1%
R29 500 BATT REF
R30 5K BATT CAL
R31 3.65K 1%
GND 13A
GND 13B
GND 13C
C20 0.1
+12V
SG IN
REF
R HI
REF ADJ
R LO
MODE
NC
J19001
BD0 3
BD1 5
BD2 7
BD3 9
BD4 4
BD5 6
BD6 8
BD7 10
+12V 25
+5V 1
-12V 26
+12V
+5v
-12v
NC 19 20 21 22
C25 0.1
+5V
Vcc
BA0 11
BA1 13
BA2 15
BA3 12
BA4 14
BA5 16
BWR 17
BRD 18
GND 2
GND 23
GND 24
A0
A1
A2
A3
A4
A5
A6
A7
A8


C
D
E
F
G
INTERFACE (19000)
PCBD 1700-5325-200
PCBD ASSY 7010-5335-200
J19006
J19008
J19007
C39
330 16V
+5V
RN1
12K
74HC244
R18H
C21
0.1
U8
74HC244
NC
R14H
C26
0.1
U13
74HC245
D0
D2
D3
D4
D5
U11
74S472
+12V
-12V
R13
20K
SYNTH
OFFSET
R12
63.4
C28
0.1
W15H
W1DH
W1EH
W1CH


H
J
K
L
M
N
C29
0.1
+12V
U16
74C374
FM/AM
SSB
R40
4.7K
Q4
2N2907
200K
R39
4.7K
Q5
2N2907
15K
R38
4.7K
Q6
2N2907
6K
REC 10dB
REC 20dB
R36
10K
R35
1K
Q2
2N2907
R37
22K
CR6
1N4148
Q3
2N2907
REC 30dB
-12V
C30
0.1
U17
74C374
NOISE FILTER
3MHz BW
300KHz BW
30KHz BW
3KHz BW
300Hz BW
R43
10K
R44
1K
Q9
2N2907
R47
22K
CR7
1N4148
Q10
2N2907
AC/N
R42
10K
R41
1K
Q7
2N2907
R45
22K
CR5
1N4148
Q8
2N2907
SPARE
C36
0.1
U20
74C374
GEN 1dB
GEN 2dB
GEN 4dB
GEN 8dB
GEN 10dB
GEN 20dB
R57
10K
R58
1K
Q13
2N2907
R59
22K
CR10
1N4148
Q14
2N2907
GEN 30dB
CR8
1N4148
CR9
1N4148
R53
3.3K
R54
680
R55
.56
2W
Q12
SJE1462
+12V ON GEN
R56
3.3K
Q11
2N2222
C23
0.1
+5V
U10
74C374
D0
D1
D2
D3
D4
D5
D6
D7
W19H
C16
0.1
SWEEP INPUT
1/A1
R16
1.10K, 1%
R17
4.99K
1%
R18
3.01K
1%
R19
1%
R20
1K
1%
C22
0.1
U9
74C374
W18H
C35
0.1
W1FH
+5V
R48
68K
W16H
RESET
THRES
DIS
TRIG
CONTROL VOLTAGE
OUTPUT
GND
C31
47
35V
C32
0.1
U18
LM555
R49
100K
R51
100K
C33
01
C37
0.1
U22
74C374
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DW15H


P
Q
R
1
2
3
4
5
6
7
P/O P19002
SPARE
LATCH 3
LATCH 3
REC BLANK
+10 SWEEP
31C SYNTH #1 SWEEP
R24
SAMPLER SWEEP GAIN
U5A
CD4053
16
R23
270
31B SAMPLER SWEEP
R21
2K
SYNTH #1 SWEEP GAIN
UNLOCK
+10/4T
LATCH 1
LATCH 2
CLOCK
DATA
IF 1dB
IF 2dB
IF 4dB
IF 8dB
IF 16dB D
IF 16dB C
IF 16dB B
IF 16dB A
TO BEEP VOL POT
SPARE
2dB/10dB
LIN/LOG
TC MSB
TC MSB
TC LSB
TC LSB
30K/300Hz
30K/300Hz
VIDEO FILTER SEL
QUASI/PEAK
QUASI/PEAK
25C FM/AM
24A SSB
24B SSB
23A 200K
23B 200K
24C 15K
23C 6K
25A REC 10dB
25B REC 10dB
26C REC 20dB
22A REC 30dB
22B REC 30dB
7C NOISE FILTER
7B 3MHz BW
11C 300KHz BW
8C 30KHz BW
9C 3KHz BW
10C 300Hz BW
6A AUTOCAL/NORM
7A SPARE
3B GEN 1dB
2C GEN 2dB
2B GEN 4dB
1C GEN 8dB
3C GEN 10dB
4A GEN 20dB
1B GEN 30dB
32A +12V ON GEN
32B +12V ON GEN
32C +12V ON GEN
R50
100K
U19
CA3130
RV2

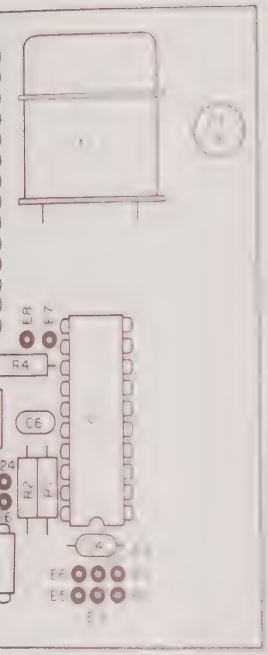
700-E2)



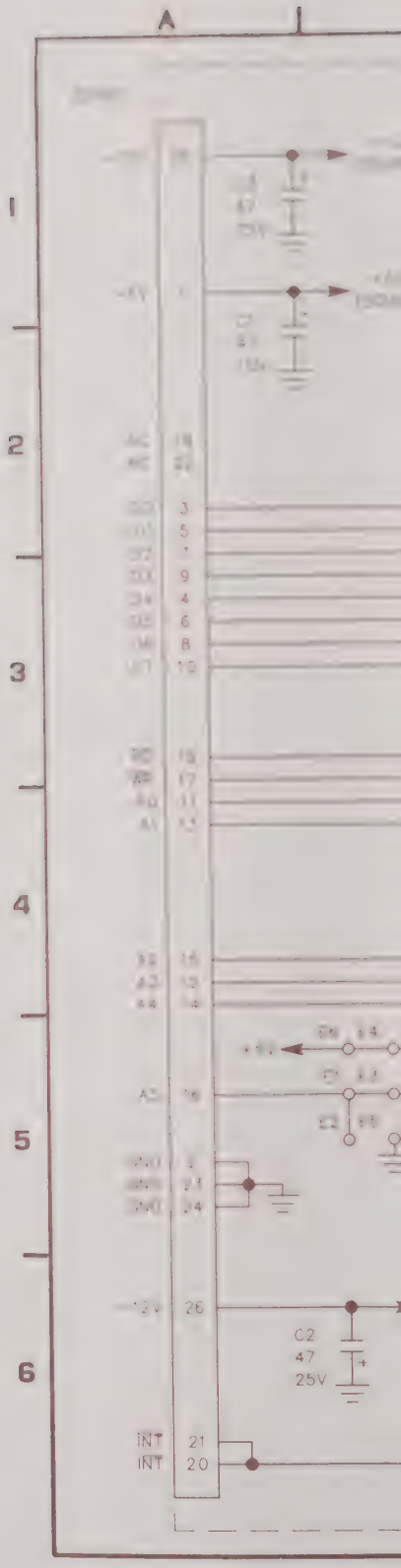
Top View

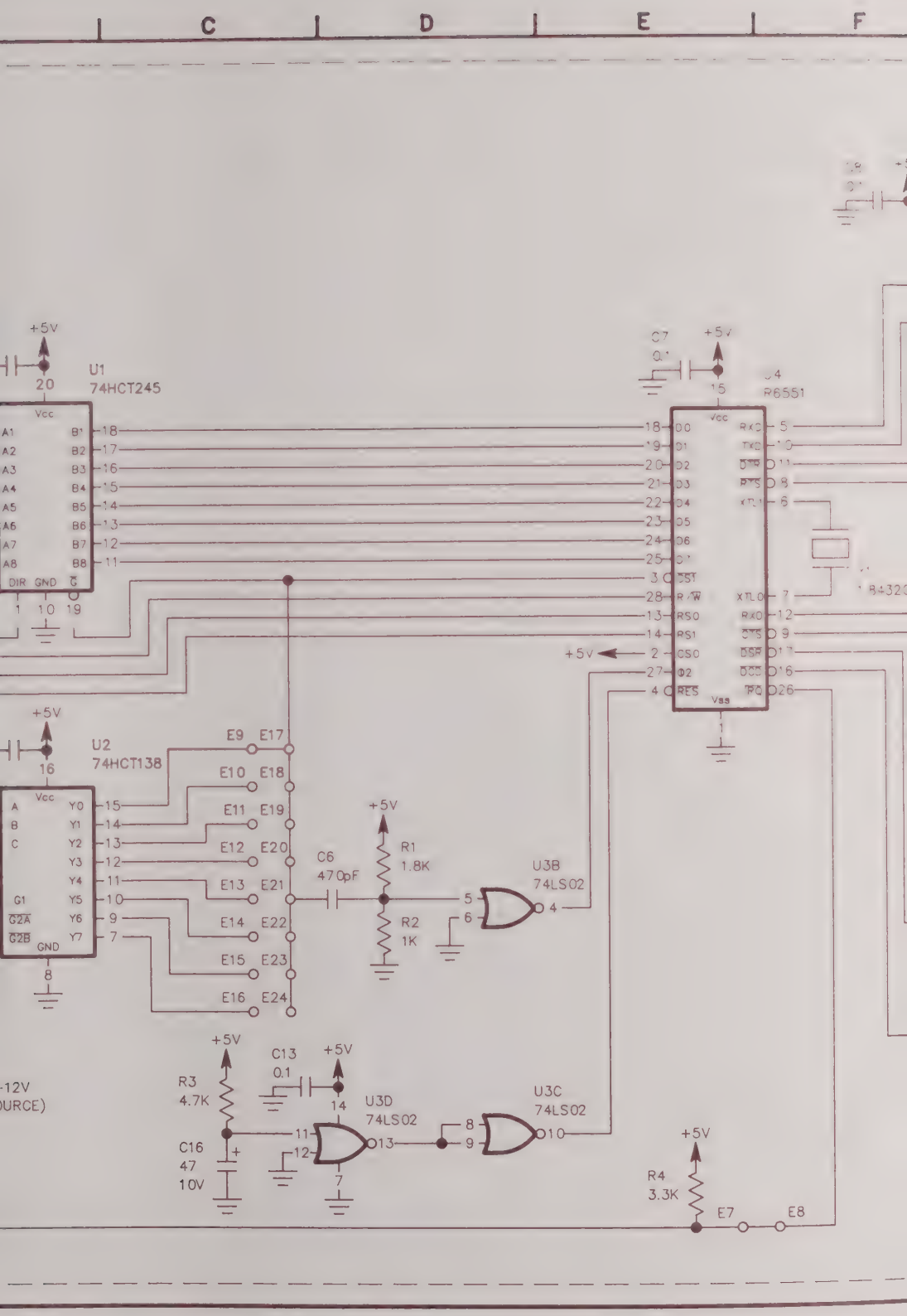
Bottom View

RS-232C PC Bd Assy (7010

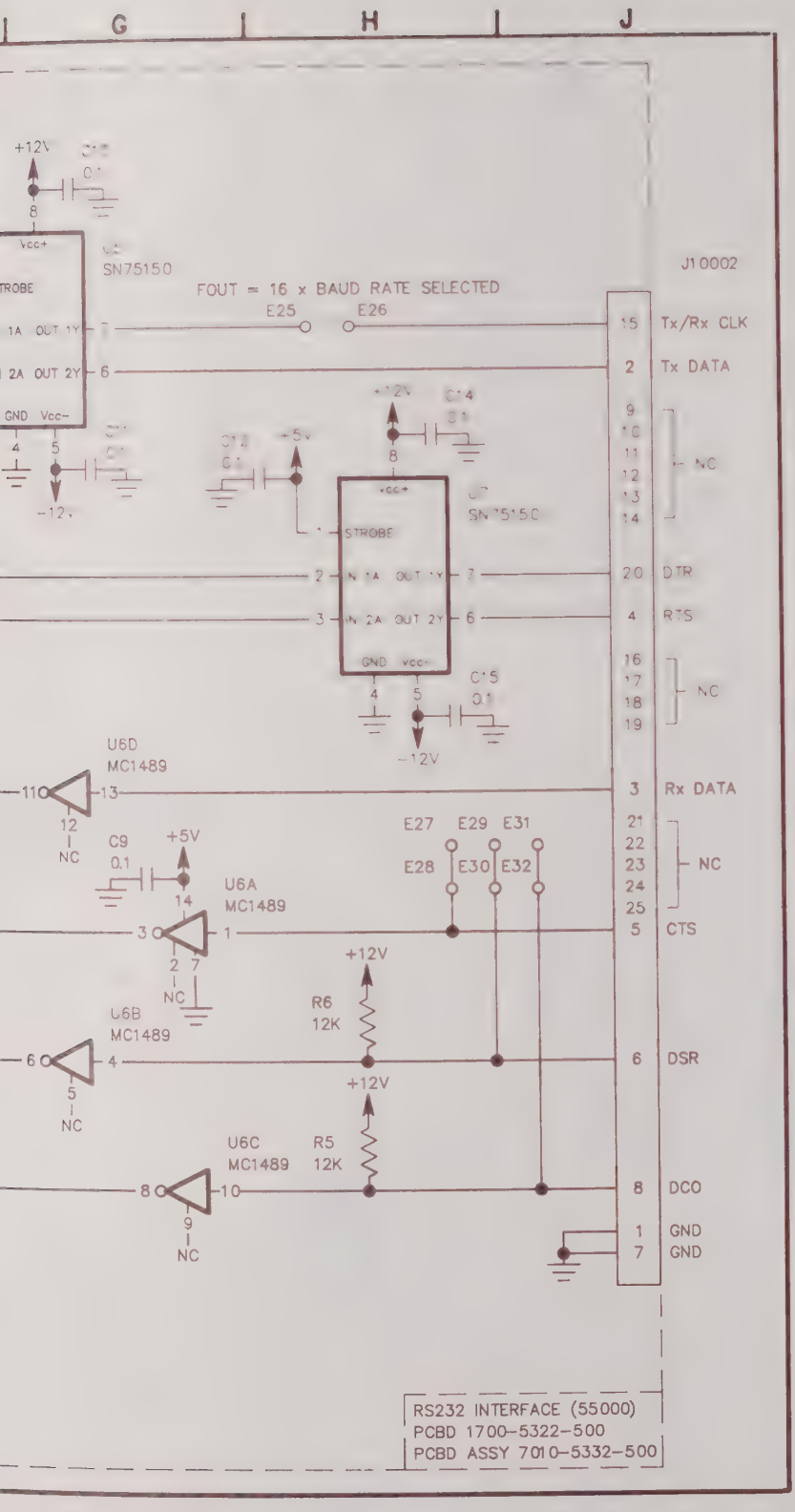


5332-500-F4)





C
D
E
F
U1
74HCT245
U2
74HCT138
U4
R6551
U3B
74LS02
U3C
74LS02
U3D
74LS02
C6
470pF
R1
1.8K
R2
1K
R3
4.7K
R4
3.3K
C13
0.1
C16
47
10V
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18
E19
E20
E21
E22
E23
E24
E7
E8
+5V
Vcc
Vss
GND
DIR


G
H
J
+12V
SN75150
FOUT = 16 x BAUD RATE SELECTED
E25
E26
J10002
15 Tx/Rx CLK
2 Tx DATA
9 10 11 12 13 14 NC
20 DTR
4 RTS
16 17 18 19 NC
3 Rx DATA
21 22 23 24 25 NC
5 CTS
6 DSR
8 DCO
1 GND
7 GND
STROBE
1A OUT 1Y
2A OUT 2Y
GND Vcc-
Vcc+
-12V
+5V
0.1
U6D
MC1489
U6A
MC1489
U6B
MC1489
U6C
MC1489
C9
R6
12K
R5
12K
E27 E29 E31
E28 E30 E32
NC
RS232 INTERFACE (55000)
PCBD 1700-5322-500
PCBD ASSY 7010-5332-500

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES: 55000.

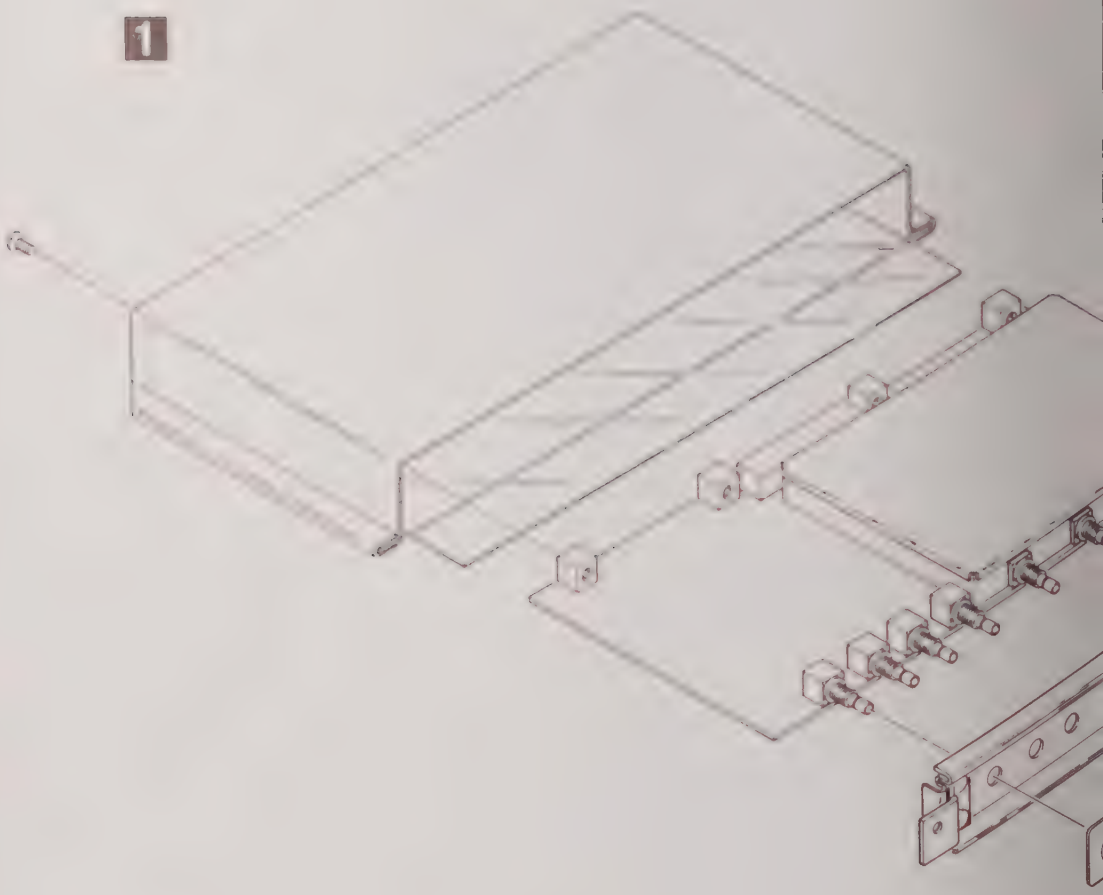
2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

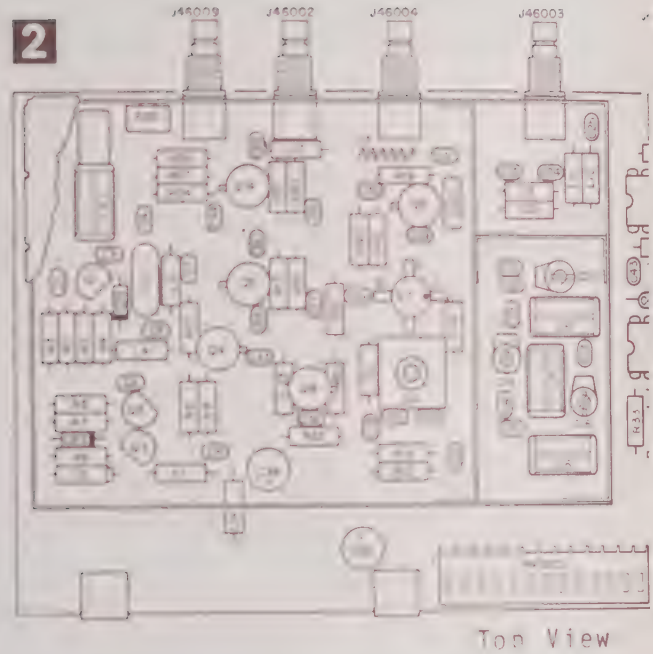
3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

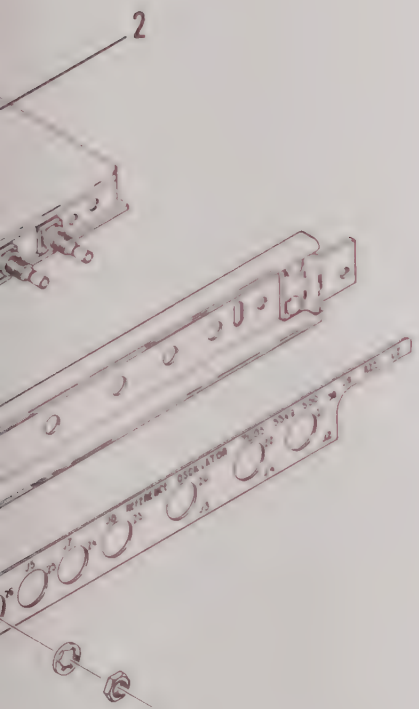
Figure 5-19 RS-232C PC Board Assembly (0000-5312-500-F2)

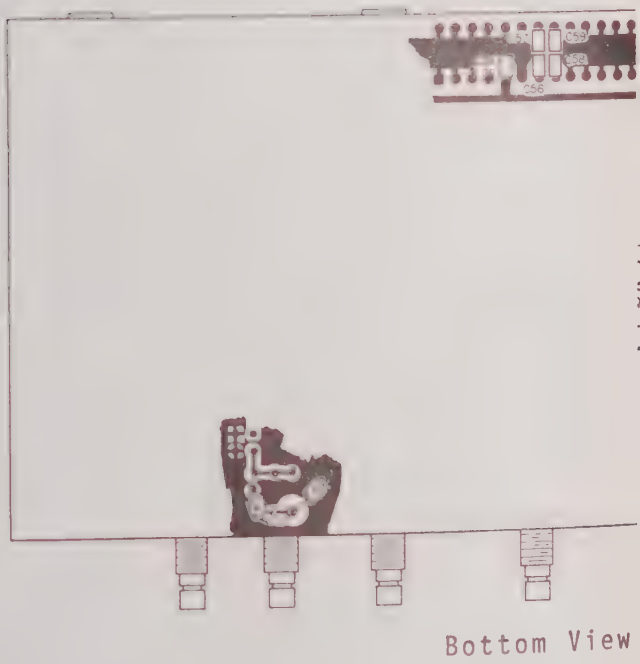
KEY:

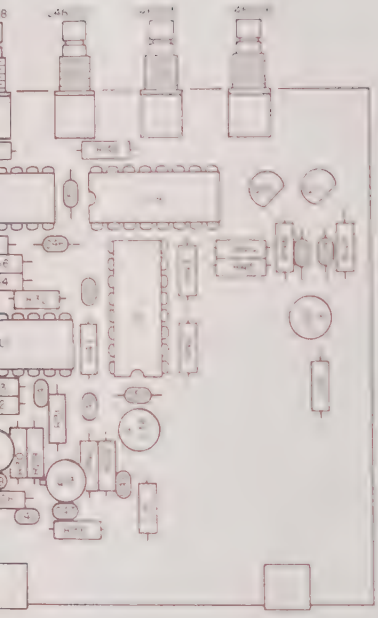
1. Reference Oscillator Assy (7005-5349-500-A)
2. Reference Oscillator PC Bd Assy (7010-5339-500-B3)

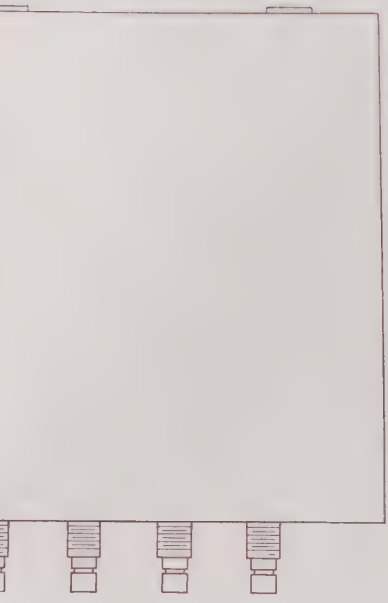


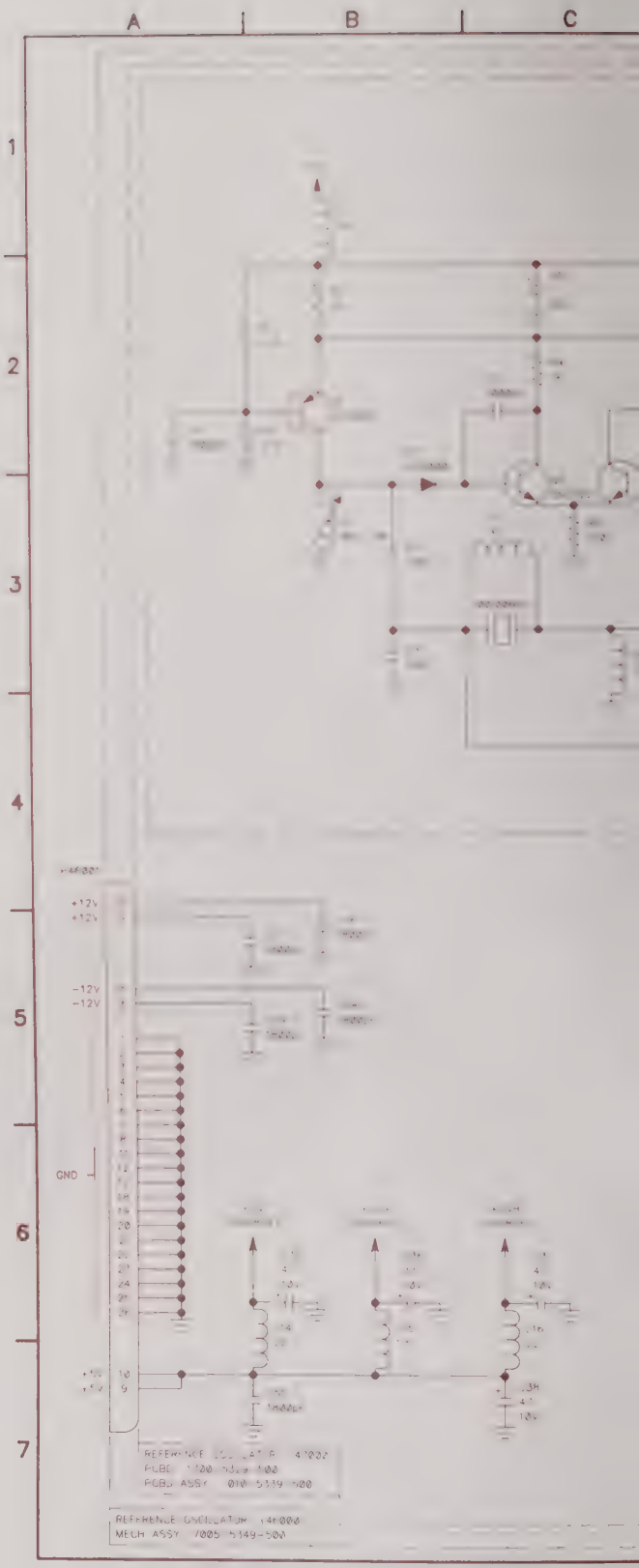

2
J46009
J46002
J46004
J46003
Top View

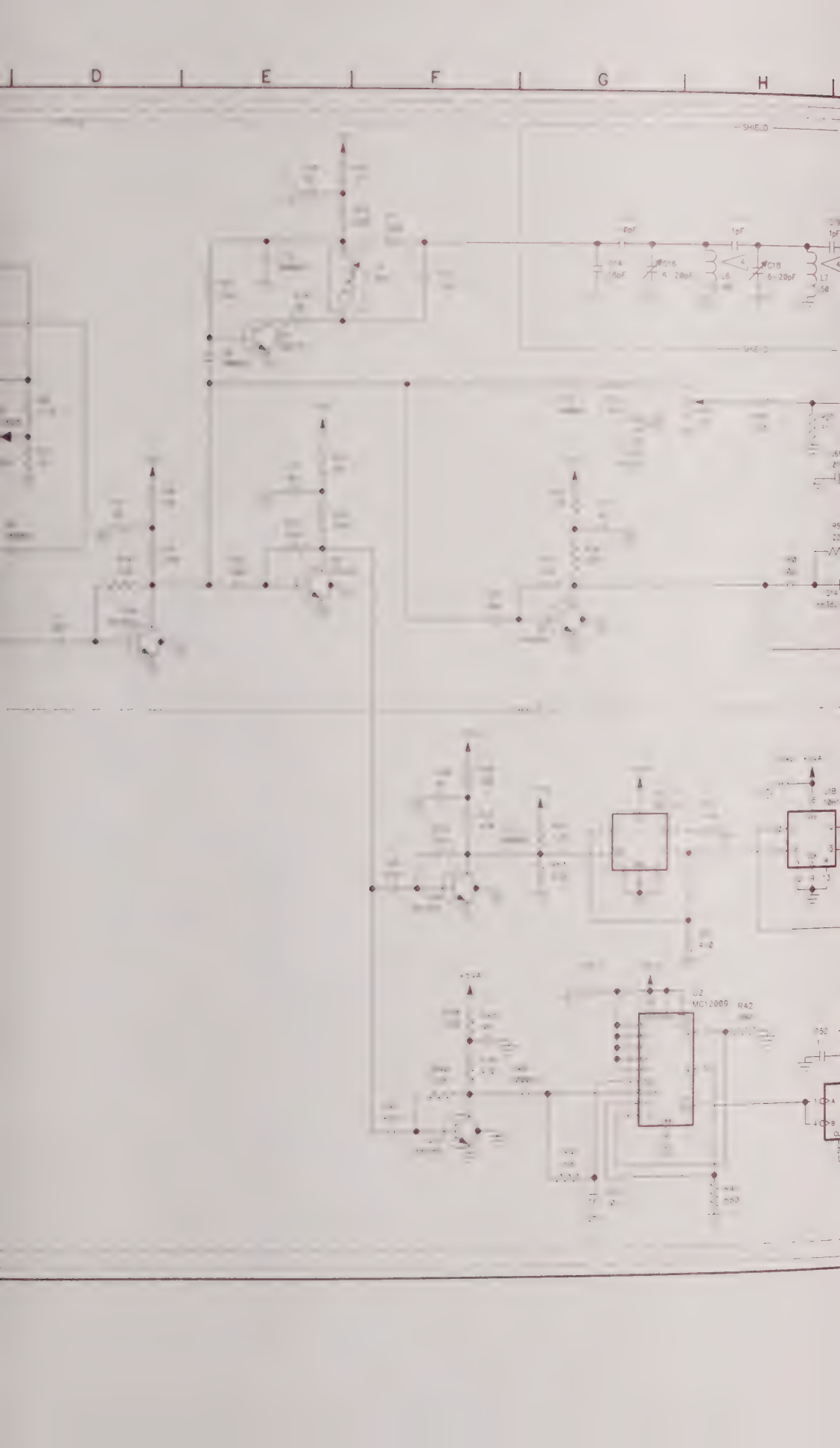

2


Bottom View






A
B
C
1
2
3
4
5
6
7
+12V
+12V
-12V
-12V
GND
+5V
+5V


D
E
F
G
H
SHIELD
SHIELD
MC12009
R42

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 46000.
   B. PC BD ASSY - 47000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

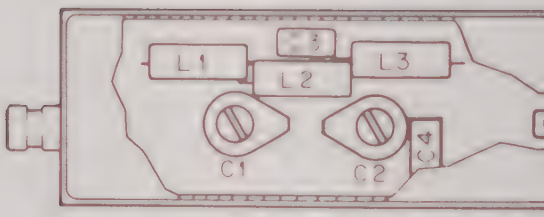
3. L47013 IS 10 TURNS OF 38 GA ENAMELLED EASY-SOLDER WIRE, .38" DIAMETER.

4. L47006, L47007 & L47008 ARE VARIABLE INDUCTORS WITH TUNING SLUGS REMOVED; EFFECTIVE INDUCTANCE = 50 μH.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

6. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

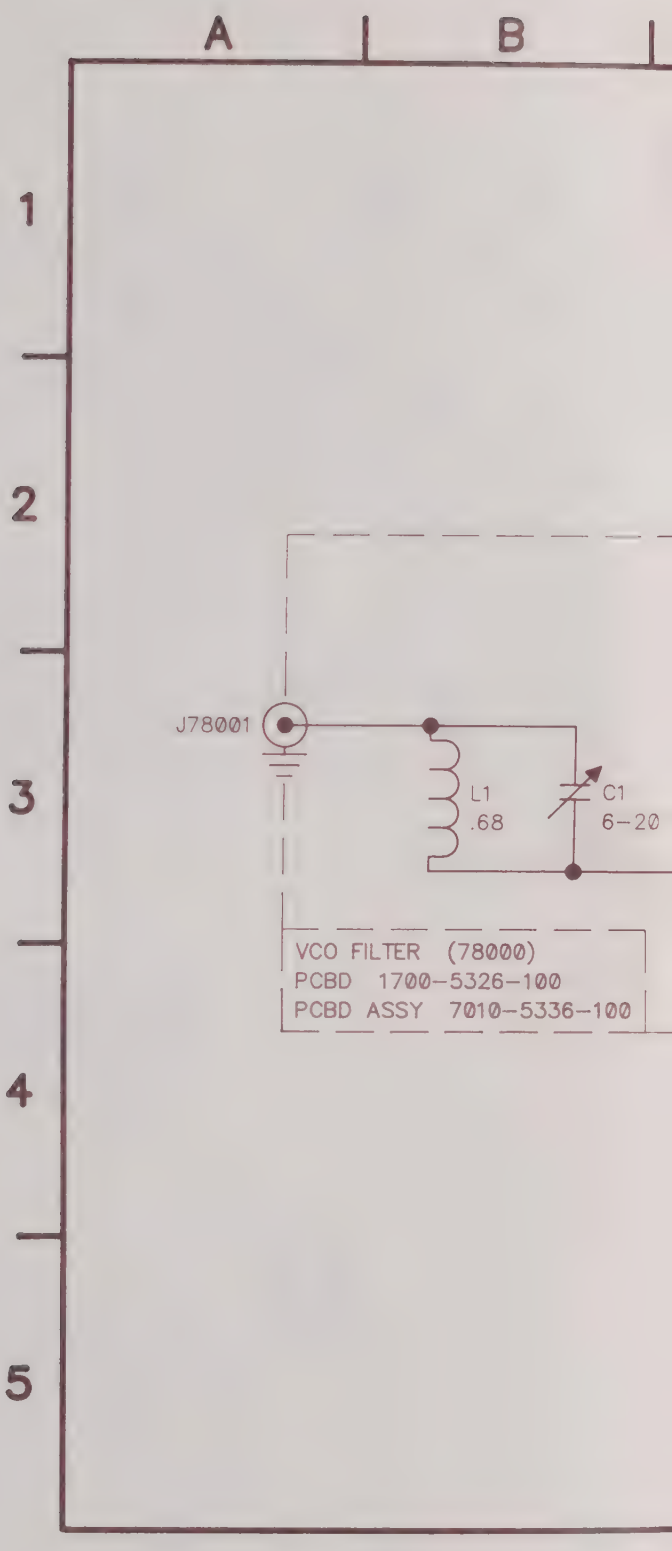
Figure 5-20 Reference Oscillator Assembly (0000-5319-500-B2)



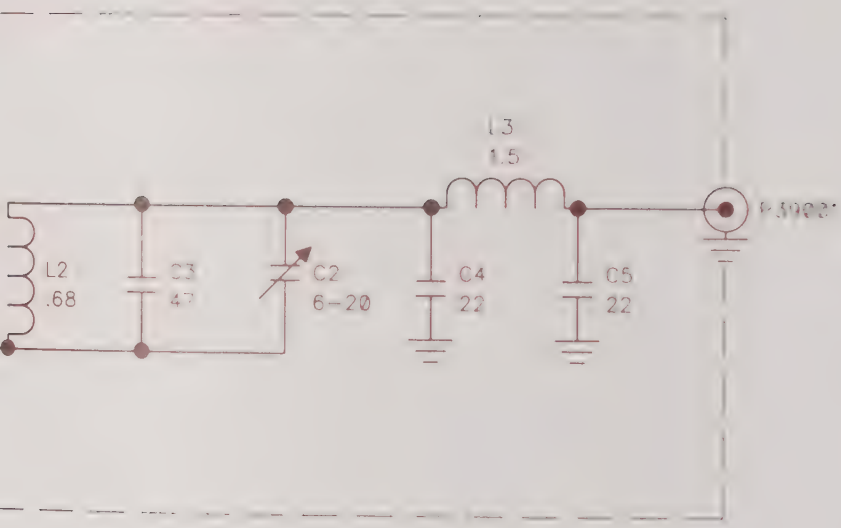
Top View

Bottom View

VCO Filter PC Bd Assy (7010-5336-100-


A
B
1
2
3
4
5
J78001
L1
.68
C1
6-20
VCO FILTER (78000)
PCBD 1700-5326-100
PCBD ASSY 7010-5336-100

C D E F



NOTES (UNLES

1. ALL
ASS
DRA

2. ALL
MIC

3. ALL
PIC

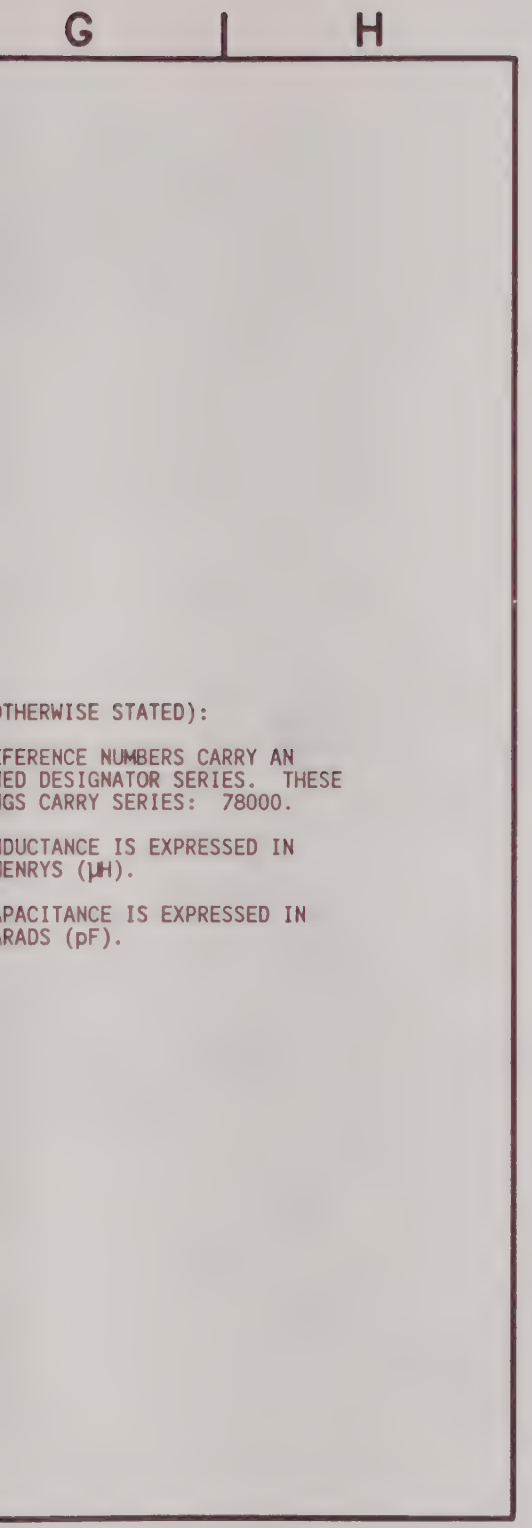
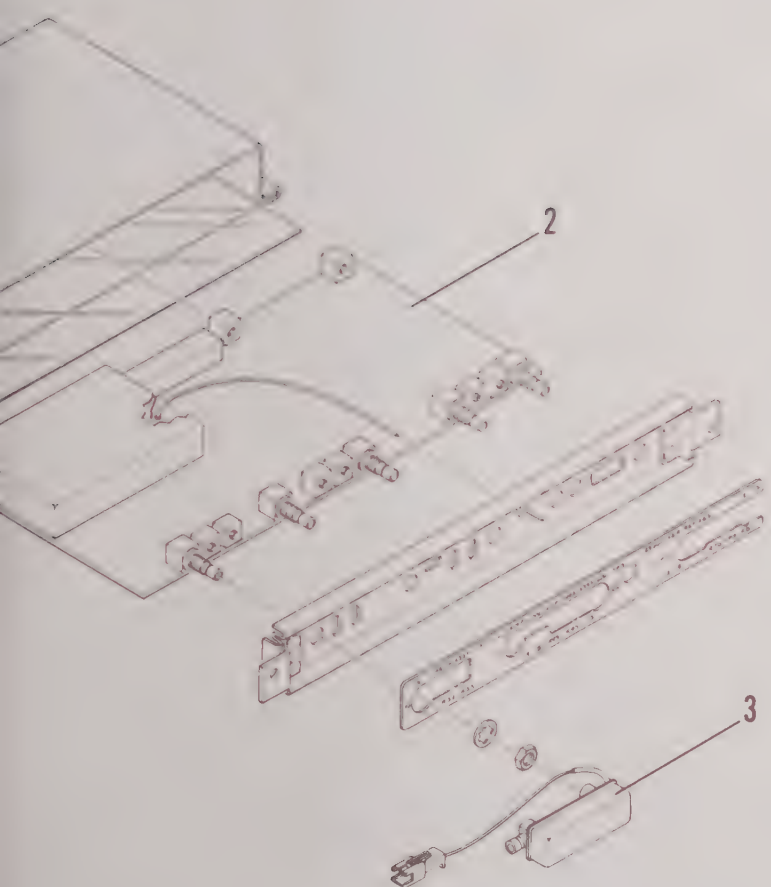


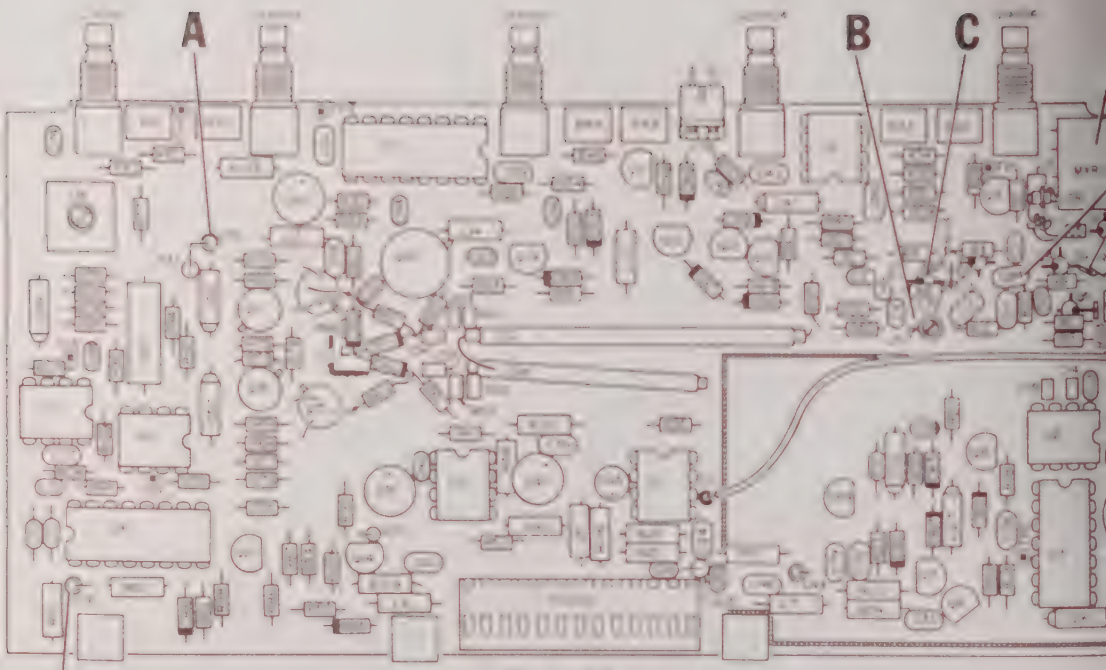
Figure 5-21 1380-2350 MHz VCO Filter PC Bd Assembly (0000-5316-100-D)

KEY:

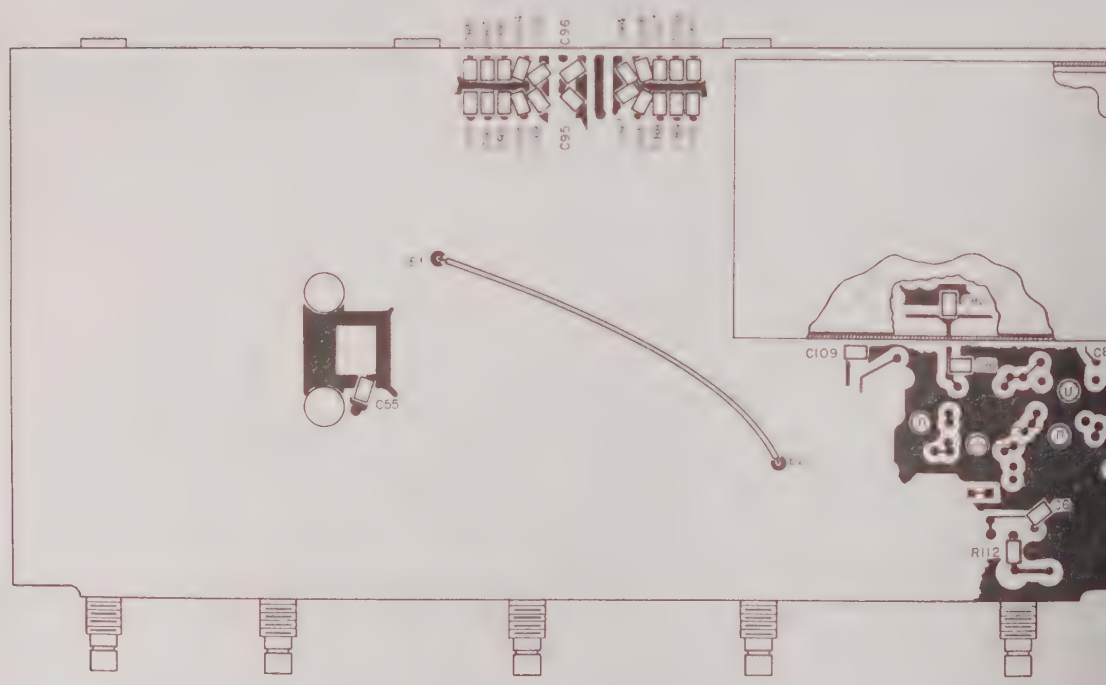
1. First
   (7005
2. First
   (7010
3. Buffe

LO Sampling Loop Assy
5343-600-H)
LO Sampling Loop PC Bd Assy
5334-601-B1)
Amp PC Bd Assy (7010-5036-800-A8)





Top View



Bottom View

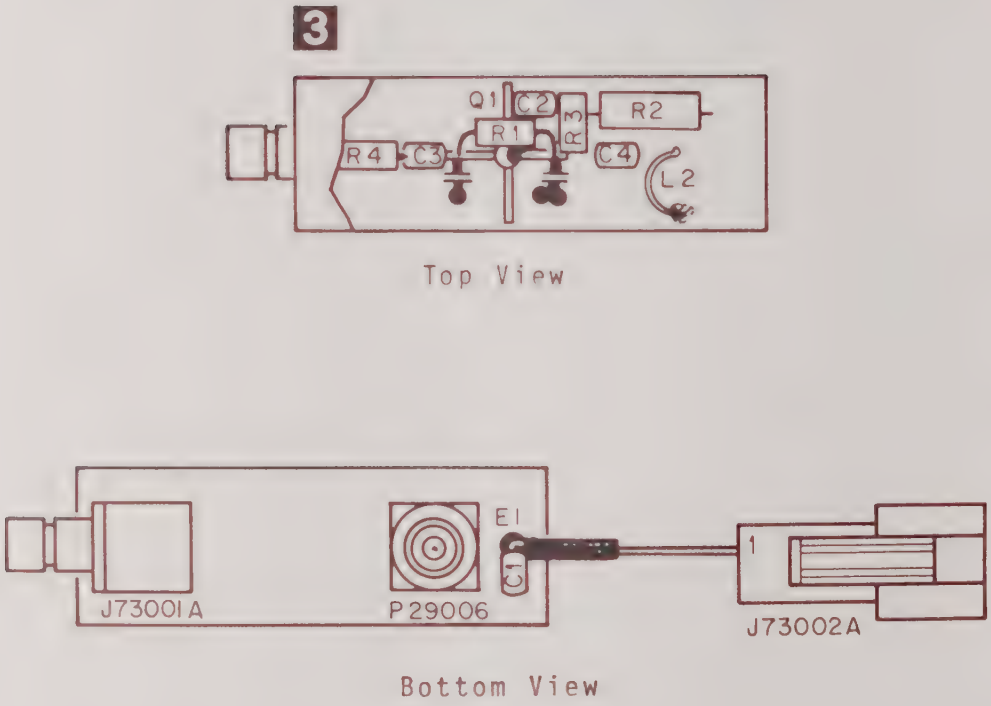
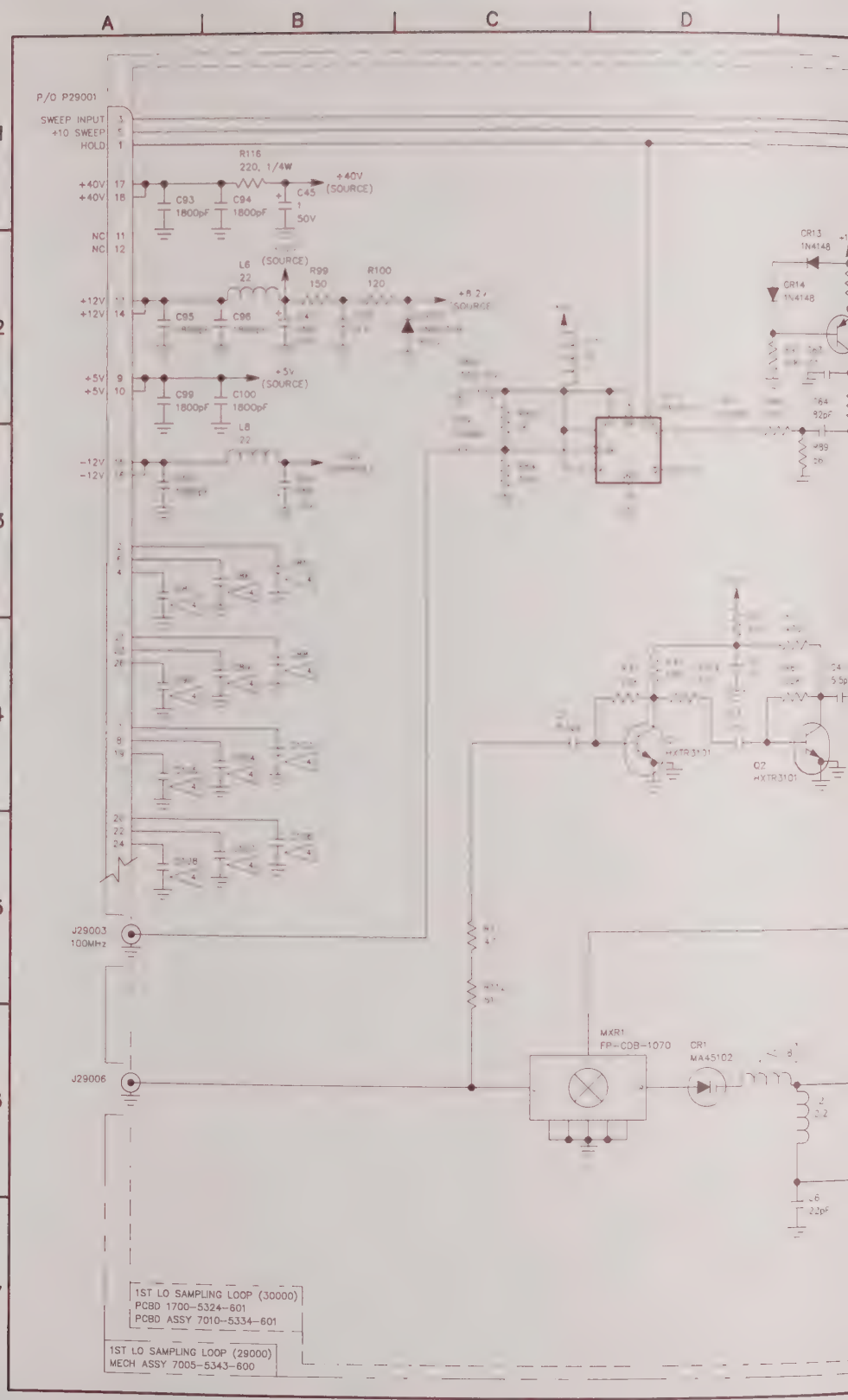
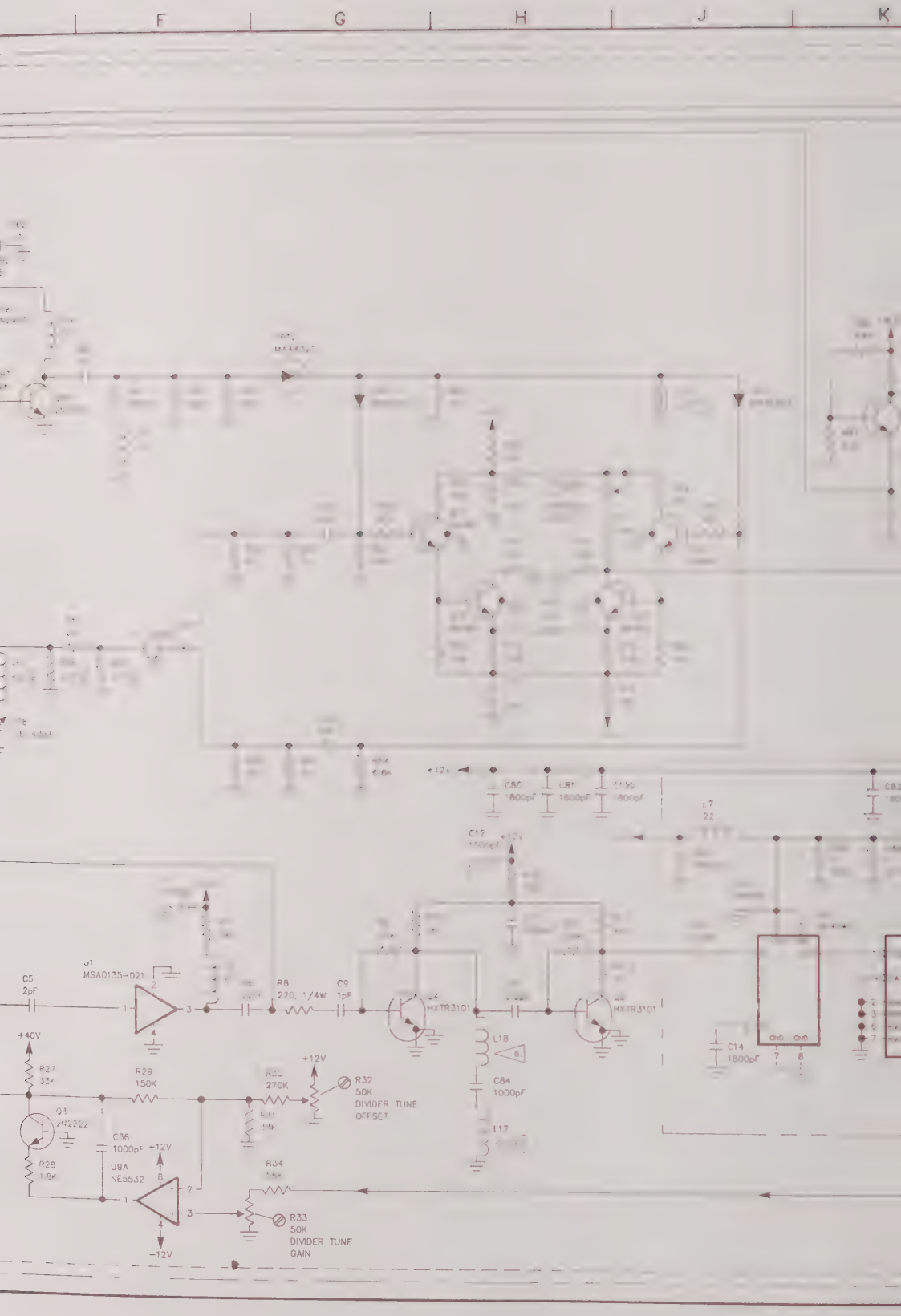
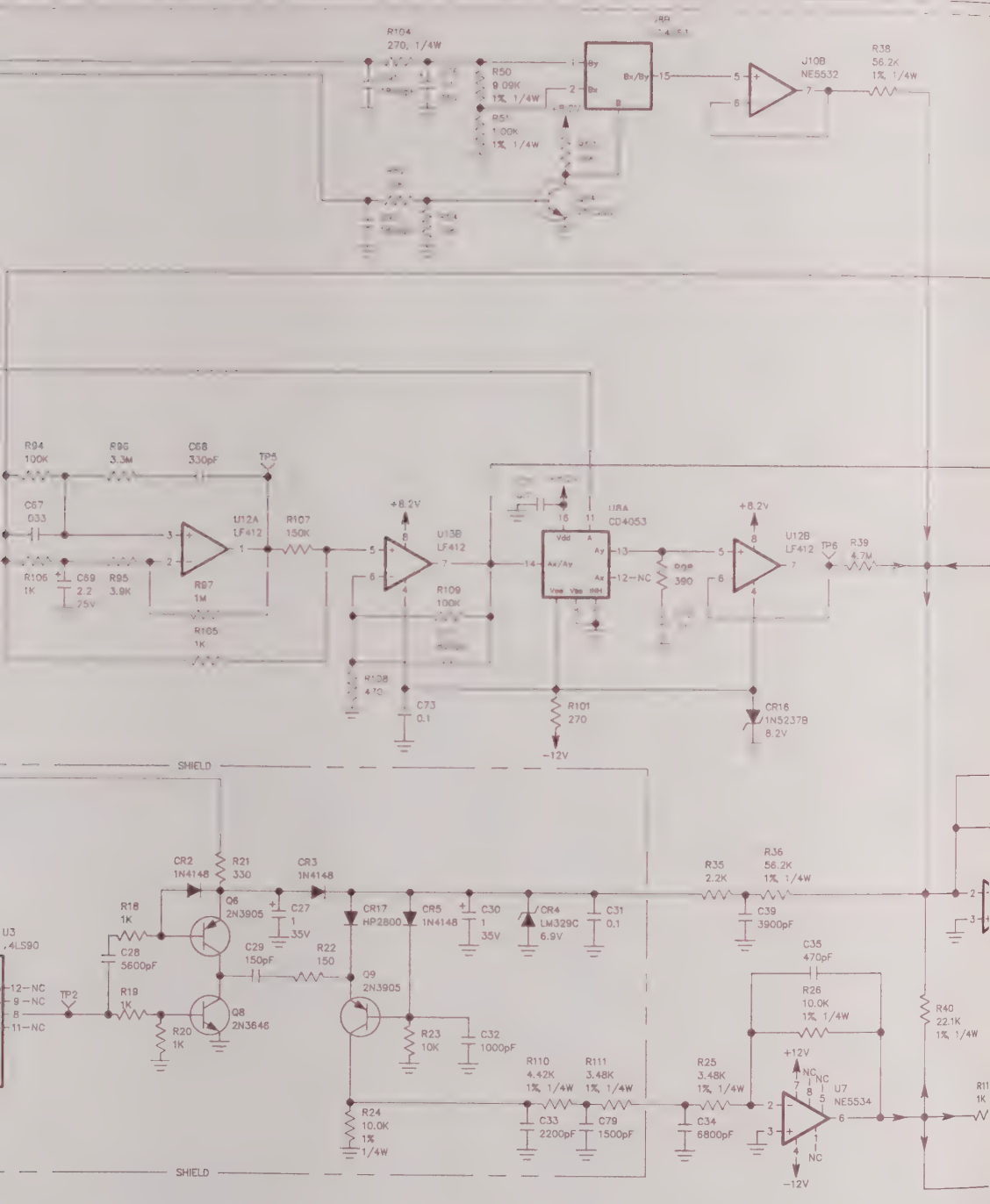
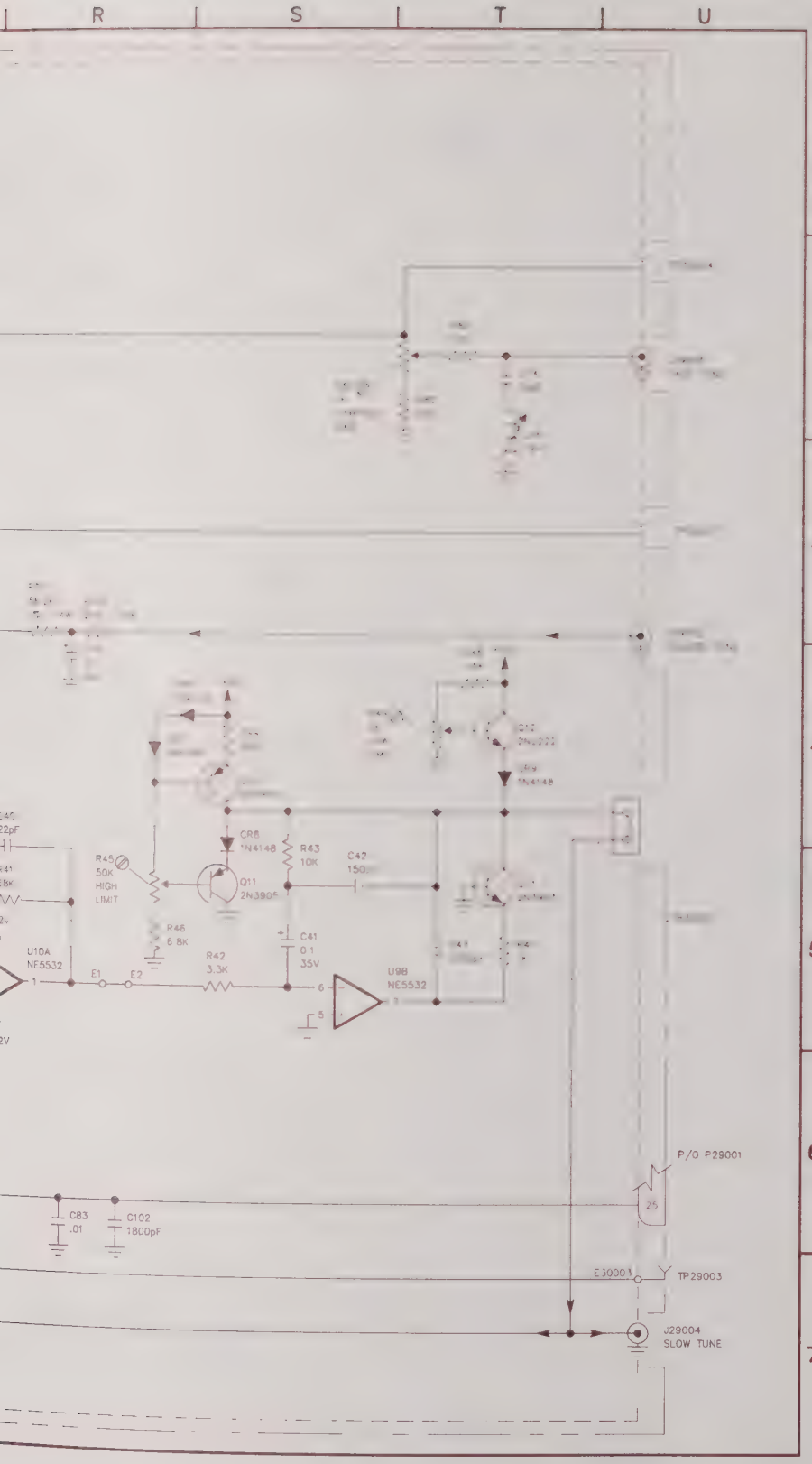


Figure 5-22 First LO Sampling Loop Assembly (Sheet 1 of 2) (0000-5314-601-B)


A
B
C
D
1
2
3
4
5
6
7
P/O P29001
SWEEP INPUT
+10 SWEEP
HOLD
+40V
+40V
NC
NC
+12V
+12V
+5V
+5V
-12V
-12V
R116
220, 1/4W
+40V
(SOURCE)
C93
1800pF
C94
1800pF
C45
1
50V
L6
22
R99
150
R100
120
+8.2V
SOURCE
C95
C96
C99
1800pF
C100
1800pF
+5V
(SOURCE)
L8
22
CR13
1N4148
CR14
1N4148
Q2
HXTR3101
J29003
100MHz
J29006
MXR1
FP-CDB-1070
CR1
MA45102
1ST LO SAMPLING LOOP (30000)
PCBD 1700-5324-601
PCBD ASSY 7010-5334-601
1ST LO SAMPLING LOOP (29000)
MECH ASSY 7005-5343-600


F
G
H
J
K
C5
2pF
U1
MSA0135-021
R8
220, 1/4W
C9
1pF
Q2
HXTR3101
HXTR3101
+40V
R27
33K
R29
150K
R30
270K
+12V
R32
50K
DIVIDER TUNE
OFFSET
L18
C84
1000pF
L17
Q1
2N2222
C36
1000pF
+12V
U9A
NE5532
R28
1.8K
R34
R33
50K
DIVIDER TUNE
GAIN
-12V
C14
1800pF
GND
GND


R104
270, 1/4W
R50
9.09K
1%, 1/4W
R51
1.00K
1%, 1/4W
J10B
NE5532
R38
56.2K
1%, 1/4W
R94
100K
R96
3.3M
C68
330pF
TP5
C67
.033
R106
1K
C69
2.2
75V
R95
3.9K
U12A
LF412
R107
150K
R97
1M
R105
1K
+8.2V
U13B
LF412
R108
470
C73
0.1
R109
100K
U11A
CD4053
R101
270
-12V
R99
390
+8.2V
U12B
LF412
TP6
R39
4.7M
CR16
1N5237B
8.2V
SHIELD
CR2
1N4148
R21
330
CR3
1N4148
R18
1K
Q6
2N3905
C27
1
35V
C28
5600pF
C29
150pF
R22
150
Q9
2N3905
R19
1K
Q8
2N3646
R20
1K
TP2
CR17
HP2800
CR5
1N4148
C30
1
35V
CR4
LM329C
6.9V
C31
0.1
R23
10K
C32
1000pF
R24
10.0K
1%
1/4W
R110
4.42K
1%, 1/4W
R111
3.48K
1%, 1/4W
C33
2200pF
C79
1500pF
R35
2.2K
R36
56.2K
1%, 1/4W
C39
3900pF
C35
470pF
R26
10.0K
1%, 1/4W
R25
3.48K
1%, 1/4W
C34
6800pF
+12V
U7
NE5534
-12V
R40
22.1K
1%, 1/4W
SHIELD


R
S
T
U
1
2
3
4
5
6
7
CR8
1N4148
R43
10K
C42
150
R45
50K
HIGH
LIMIT
Q11
2N3905
R46
6.8K
C41
0.1
35V
U10A
NE5532
E1
E2
R42
3.3K
U9B
NE5532
P/O P29001
25
C83
.01
C102
1800pF
E30001
TP29003
J29004
SLOW TUNE

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 29000.
   B. PC BD ASSY - 30000.

2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

4. C30085 THRU C30090 & C30103 THRU C30108 ARE SELECTED AT TEST (S.A.T.) AND USED AS REQUIRED.
   NOMINAL VALUE = 1800 pF.

5. R30056 AND R30057 ARE SELECTED AT TEST (S.A.T.):
   NOMINAL VALUE = 120Ω
   RANGE = 68Ω THRU 150Ω.

6. L30017 AND L30018 ARE 0.1" LENGTHS OF C30084 LEADS.

7. L30012 IS 0.02" X 0.2" PATH ON PC BD.

8. L30001 IS 1.5" LENGTH OF 26 AWG WIRE.

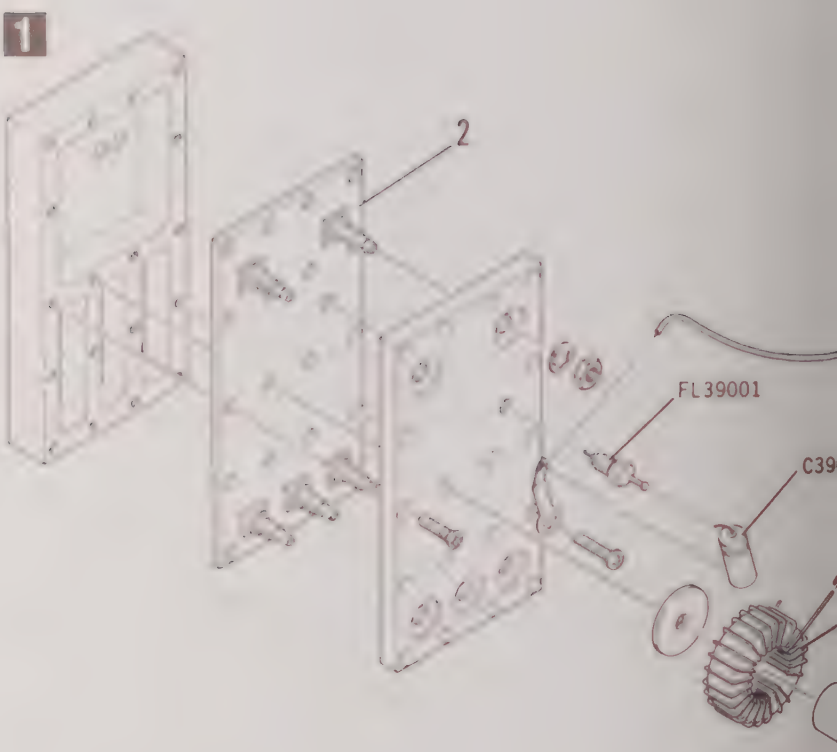
9. L30004 IS 0.3" LENGTH OF 22 GA. BUS WIRE.

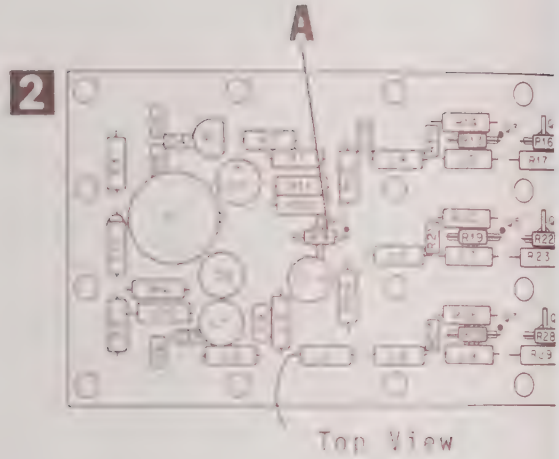
10. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

Figure 5-22 First LO Sampling Loop Assembly (Sheet 2 of 2) (0000-5314-601-B)

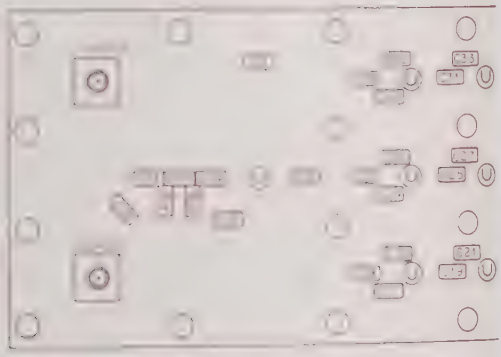
KEY:

1. 1350-2350 MHz VCO Assy (7005-5345-600-E)
2. 1350-2350 MHz VCO PC Bd Ass (7010-5335-600-C5)





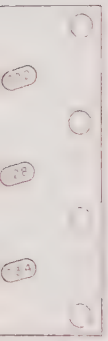
Top View



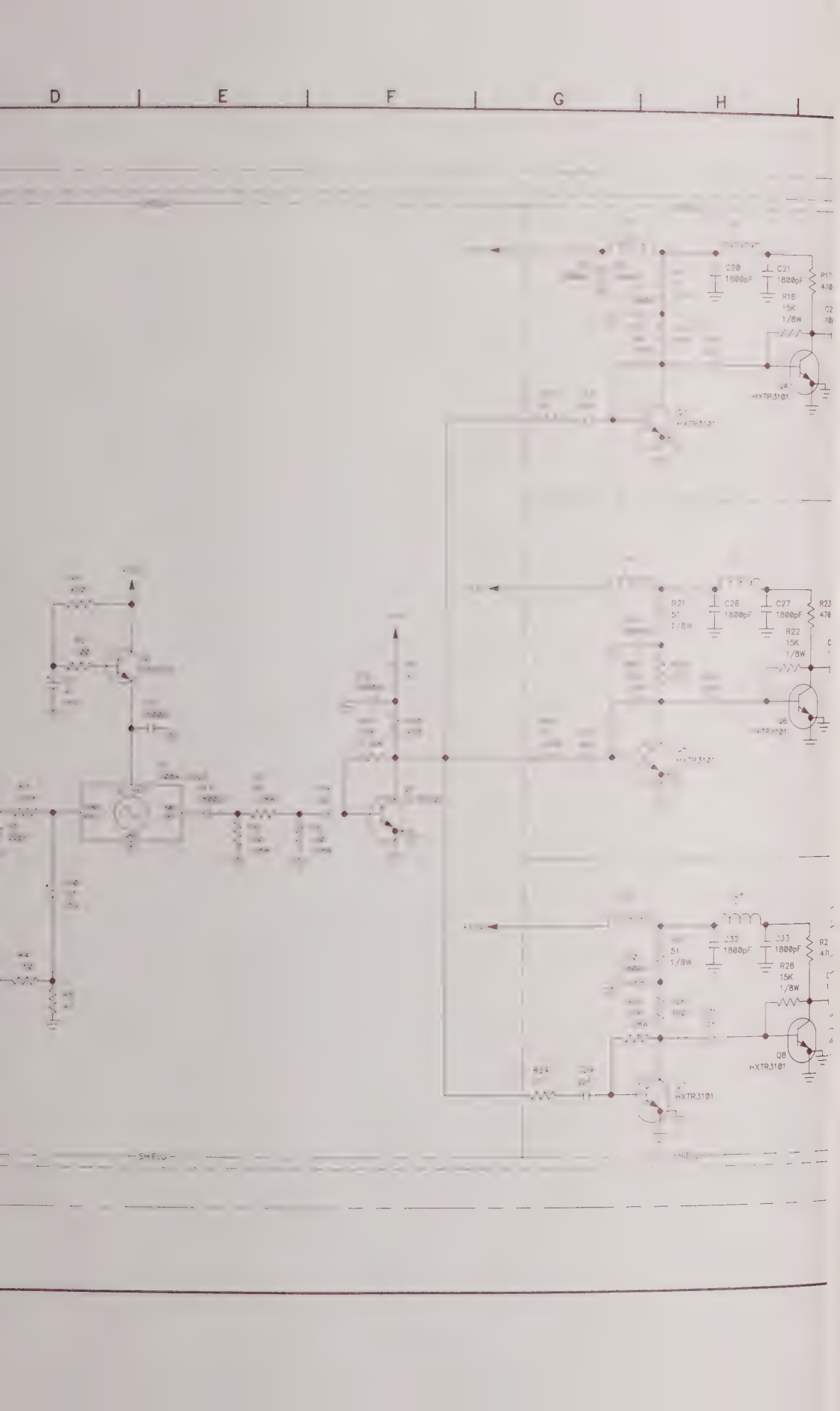
Bottom View

DETAIL **A**

TYPICAL FOR: Q40003 & R40013, Q40004 &
Q40005 & R40019, Q40006 &
Q40007 & R40025, Q40008 &



40016,
40022,
40028.


D
E
F
G
H
C20
1800pF
C21
1800pF
R16
15K
1/8W
HXTR3101
R21
C26
1800pF
C27
1800pF
R22
15K
1/8W
HXTR3101
C32
1800pF
C33
1800pF
R28
15K
1/8W
Q8
HXTR3101
HXTR3101

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 39000.
   B. PC BD ASSY - 40000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

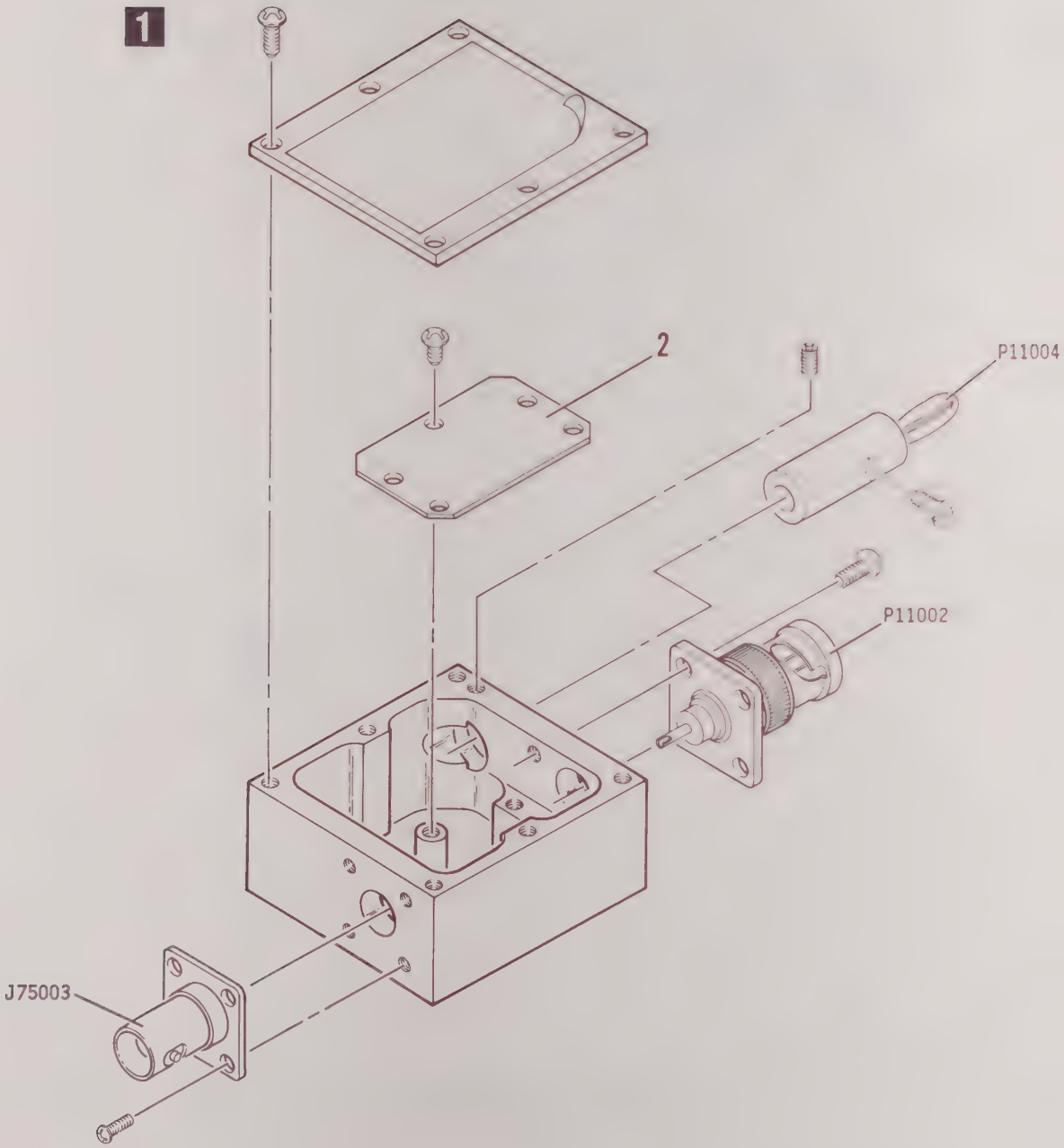
3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

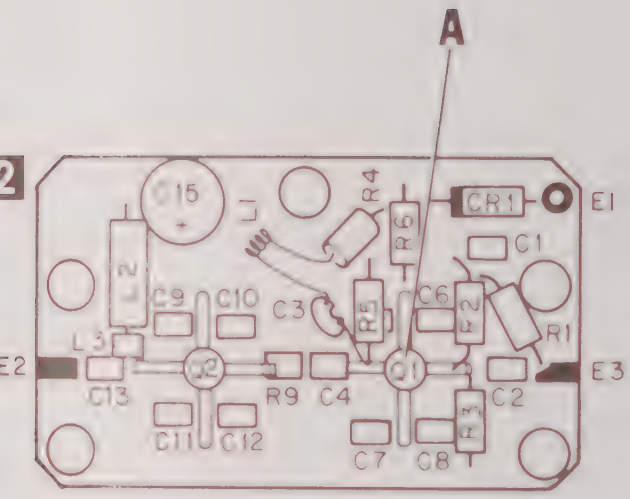
4. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

Figure 5-23 1350-2350 MHz VCO Assembly (0000-5315-600-C4)

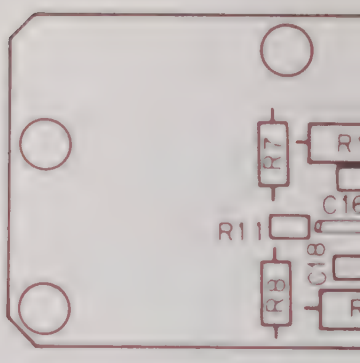
KEY:

1. +20 dB External Amp Assy (7005-5346-000-F)
2. +20 dB External Amp PC Bd Assy (7010-5336-000-C6)

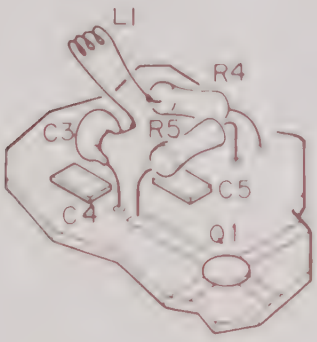




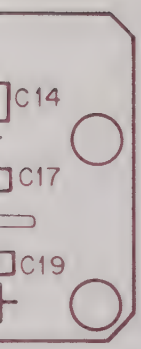
Top View

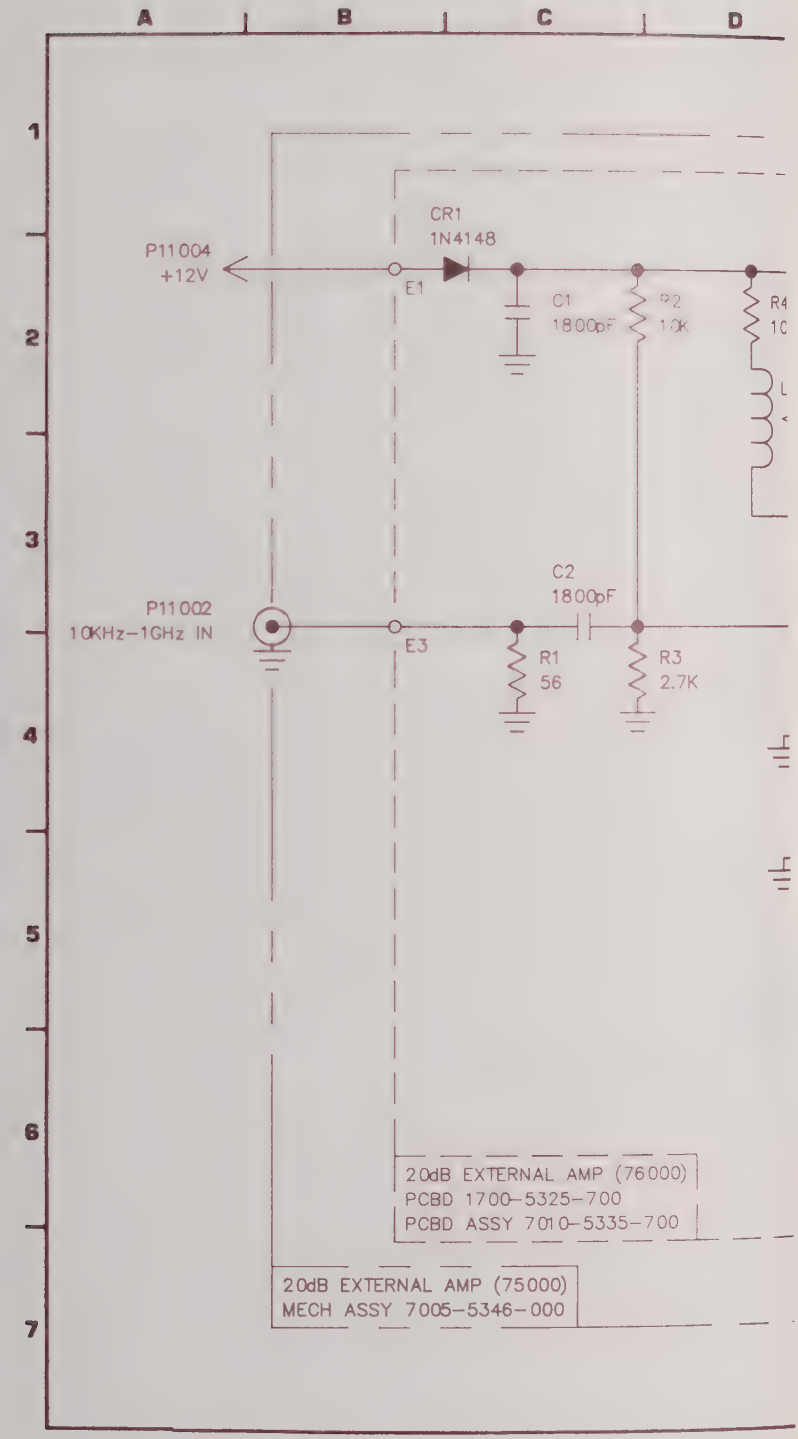


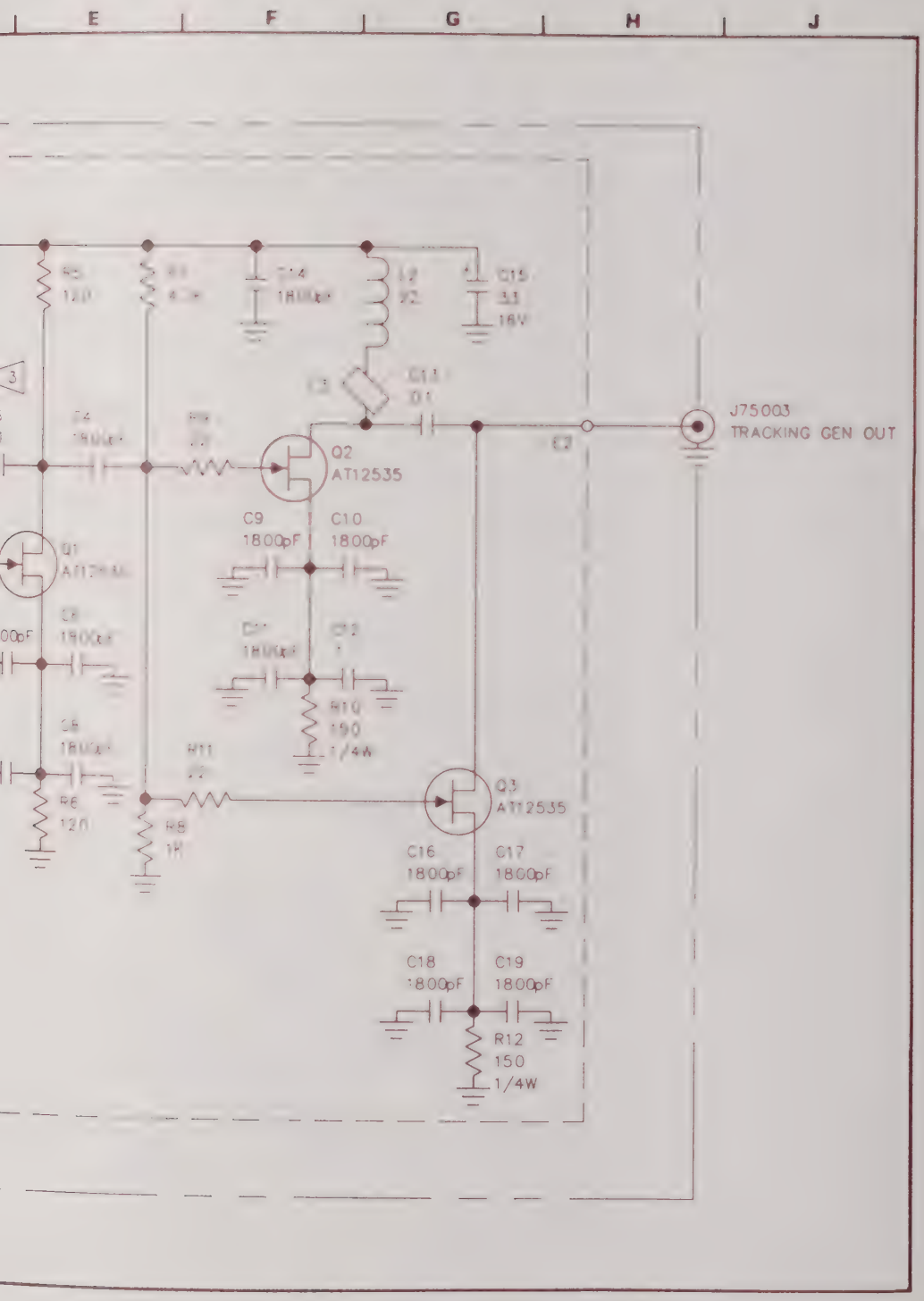
Bottom Vie



DETAIL **A**


C14
C17
C19


A
B
C
D
1
2
3
4
5
6
7
CR1
1N4148
P11004
+12V
E1
C1
1800pF
R2
10K
R4
10
C2
1800pF
P11002
10KHz-1GHz IN
E3
R1
56
R3
2.7K
20dB EXTERNAL AMP (76000)
PCBD 1700-5325-700
PCBD ASSY 7010-5335-700
20dB EXTERNAL AMP (75000)
MECH ASSY 7005-5346-000


E
F
G
H
J
Q2
AT12535
C9
1800pF
C10
1800pF
Q3
AT12535
C16
1800pF
C17
1800pF
C18
1800pF
C19
1800pF
R10
190
1/4W
R12
150
1/4W
J75003
TRACKING GEN OUT

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY THE FOLLOWING SERIES:

   A. MECH ASSY - 75000
   B. PC BD ASSY - 76000

2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. L76001 IS 4 TURNS OF 38 GA. ENAMELLED EASY-SOLDER WIRE, .38" DIAMETER.

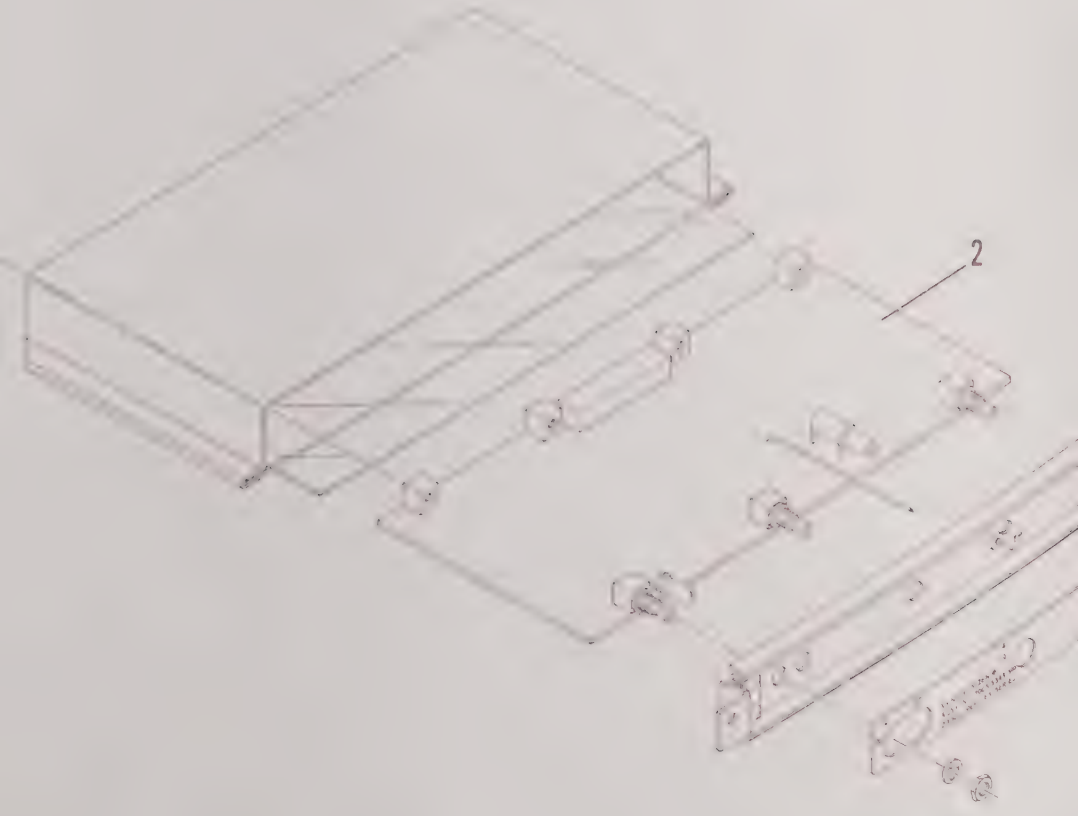
4. ALL CAPACITANCE IS EXPRESSED IN PICOFARADS (pF).

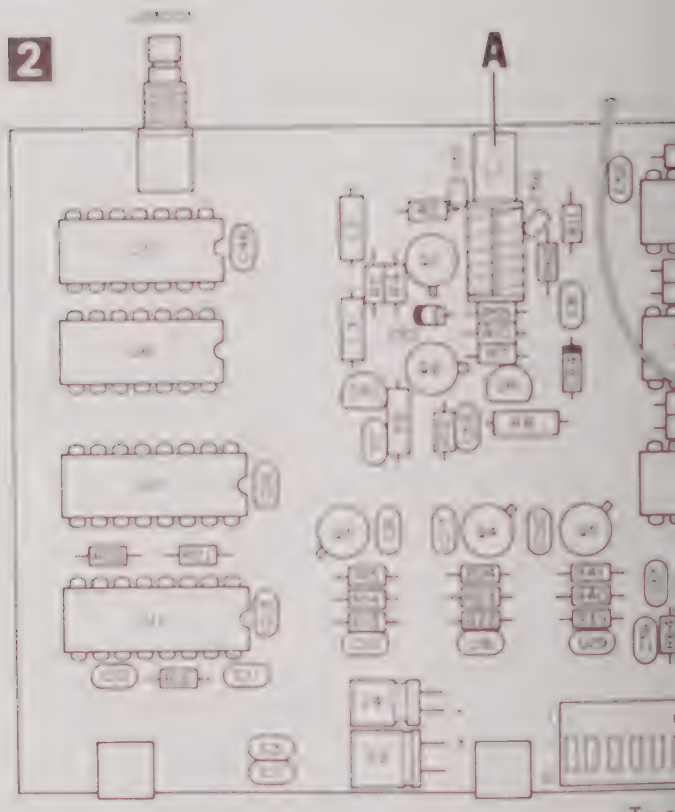
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

Figure 5-24 +20 dB External Amplifier Assembly (0000-5315-700-C4)

KEY:

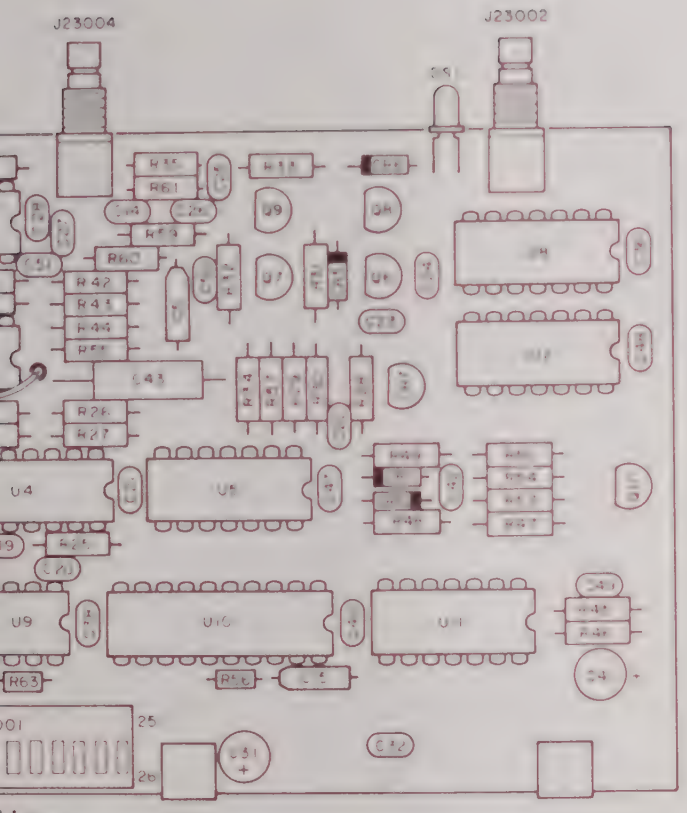
1. Synthesizer #1 Assy (7005-5343-500-G)
2. Synthesizer #1 PC Bd Assy (7010-5333-501-B1)



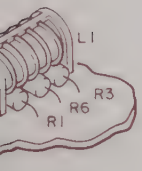


Top

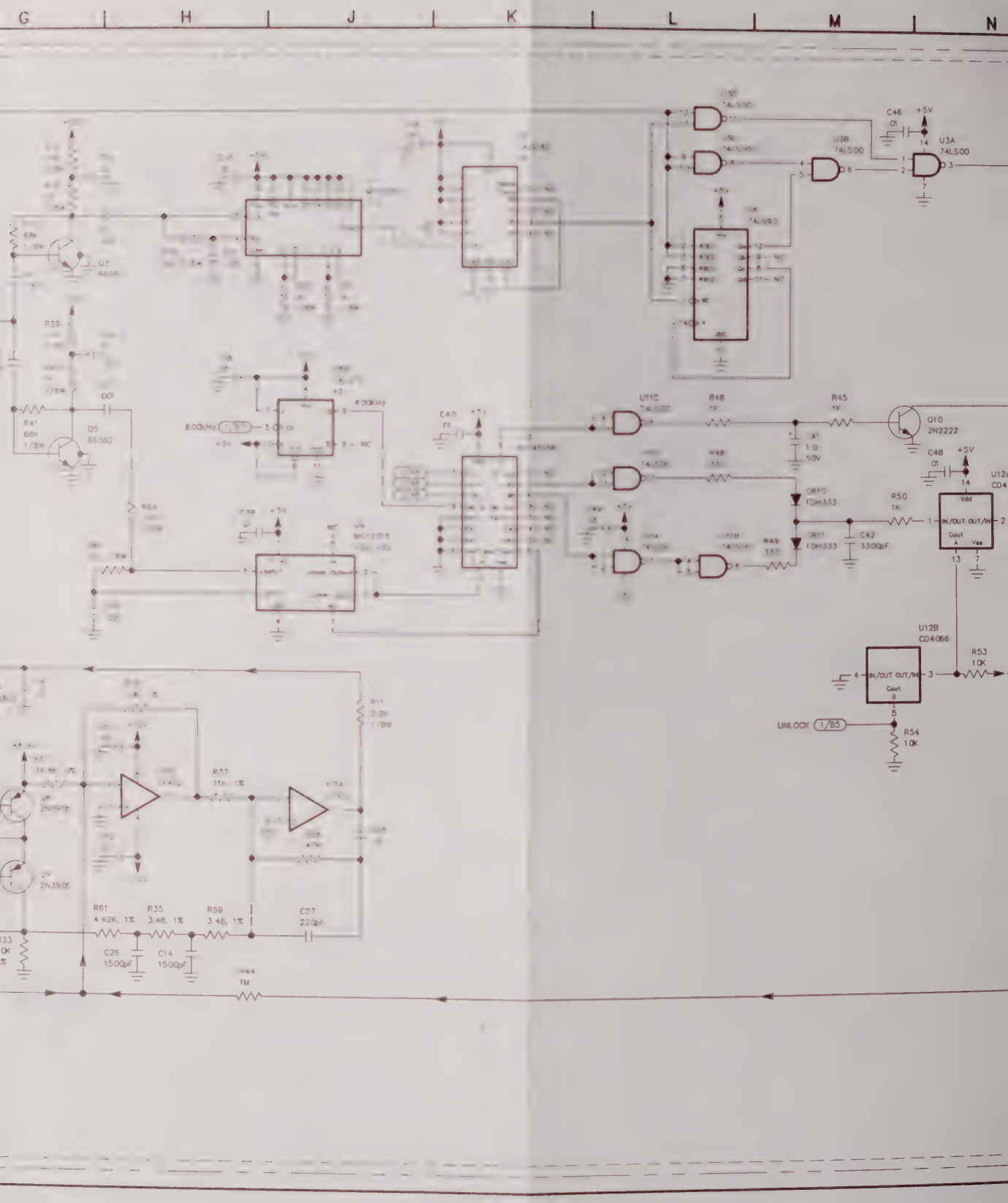
DE

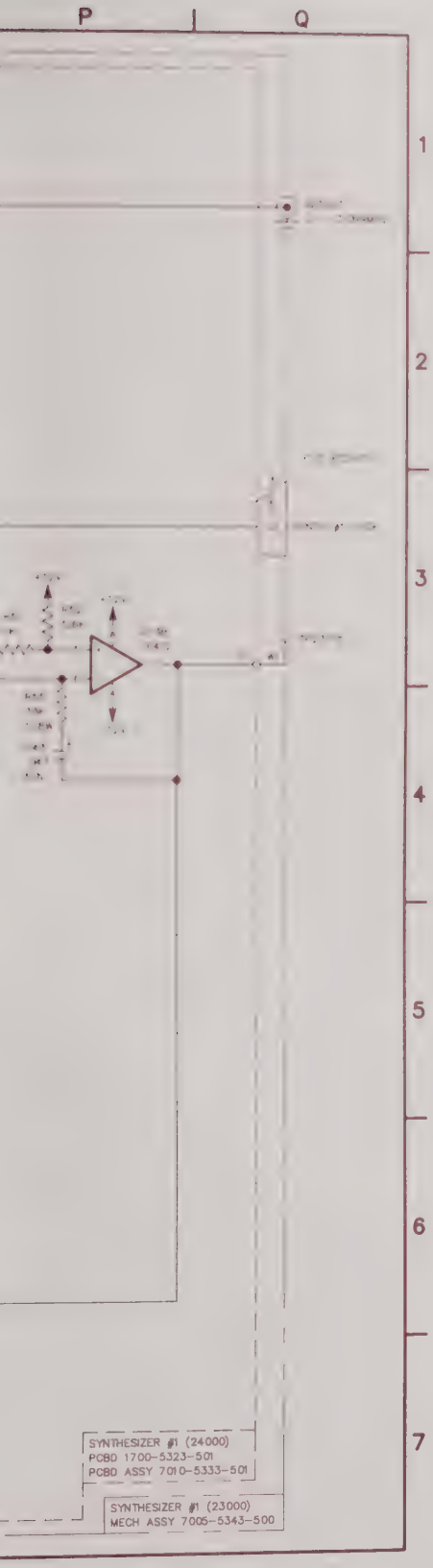


iew



IL **A**


G
H
J
K
L
M
N
C46
+5V
U3B
74LS00
U3A
74LS00
R39
R41
68K
1/8W
Q5
66382
R64
800KHz
C40
U11C
R46
R45
1K
Q10
2N2222
C48
+5V
R50
1K
C42
3300pF
U12B
CD4066
R53
10K
UNLOCK
1/B5
R54
10K
R11
2.2K
1/8W
R37
11K 1%
2N3905
R61
4.42K, 1%
R35
3.48, 1%
R59
3.48, 1%
C27
220pF
C26
1500pF
C14
1500pF
1M



NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 23000.
   B. PC BD ASSY - 24000.

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

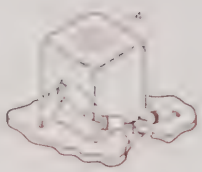
3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

4. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

5. C24060, C24061 & C24074 THRU C24082 ARE SELECTED AT TEST (S.A.T.) AND USED AS REQUIRED.
   NOMINAL VALUE = 1800 pF.

6. TUNE L24001 FOR +9 VDC ON PIN 1 OF U24007 WITH OSCILLATOR AT 200 MHz (+N - 4000).

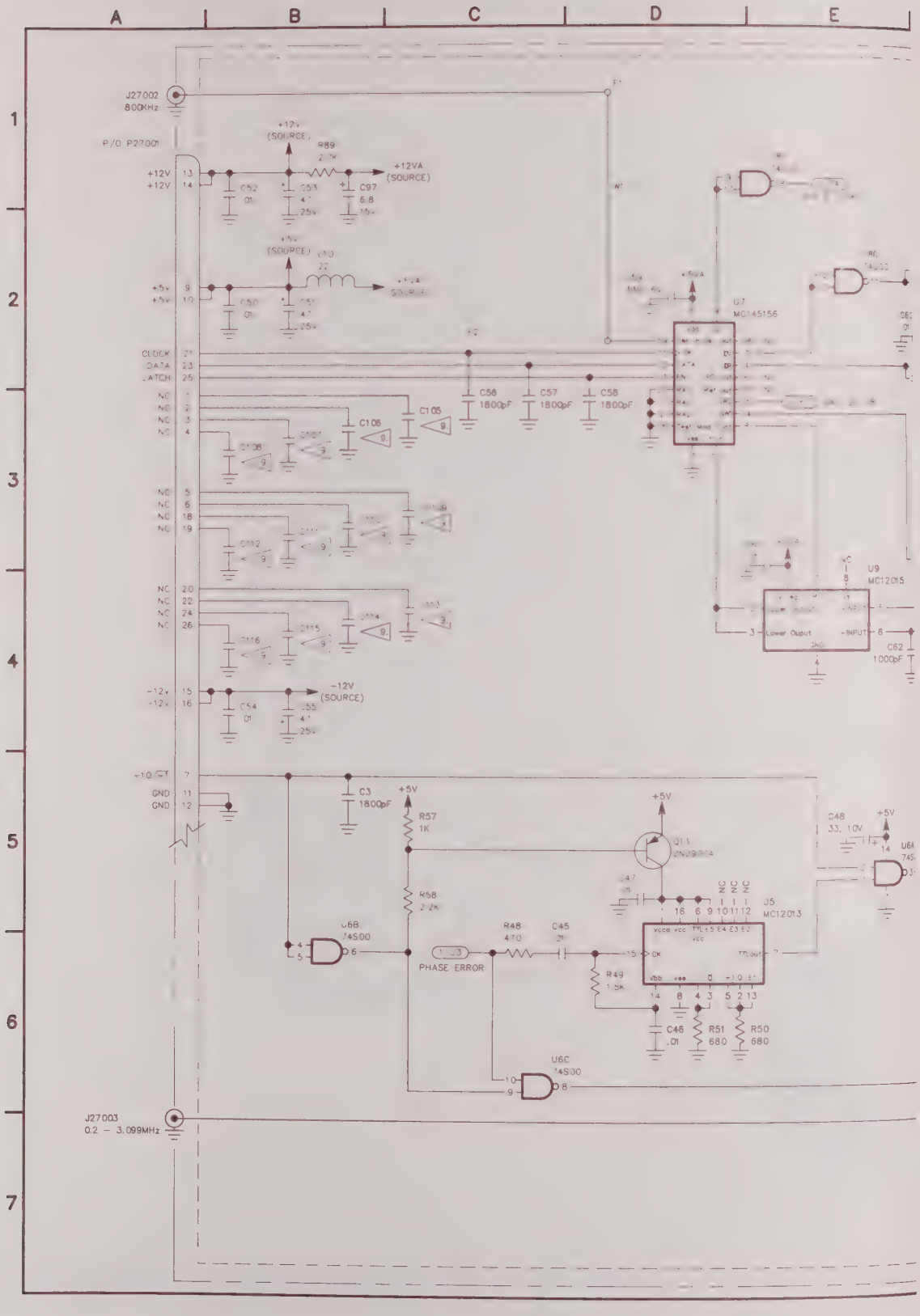
Figure 5-25 Synthesizer #1 Assembly (Sheet 2 of 2) (0000-5313-501-B1)

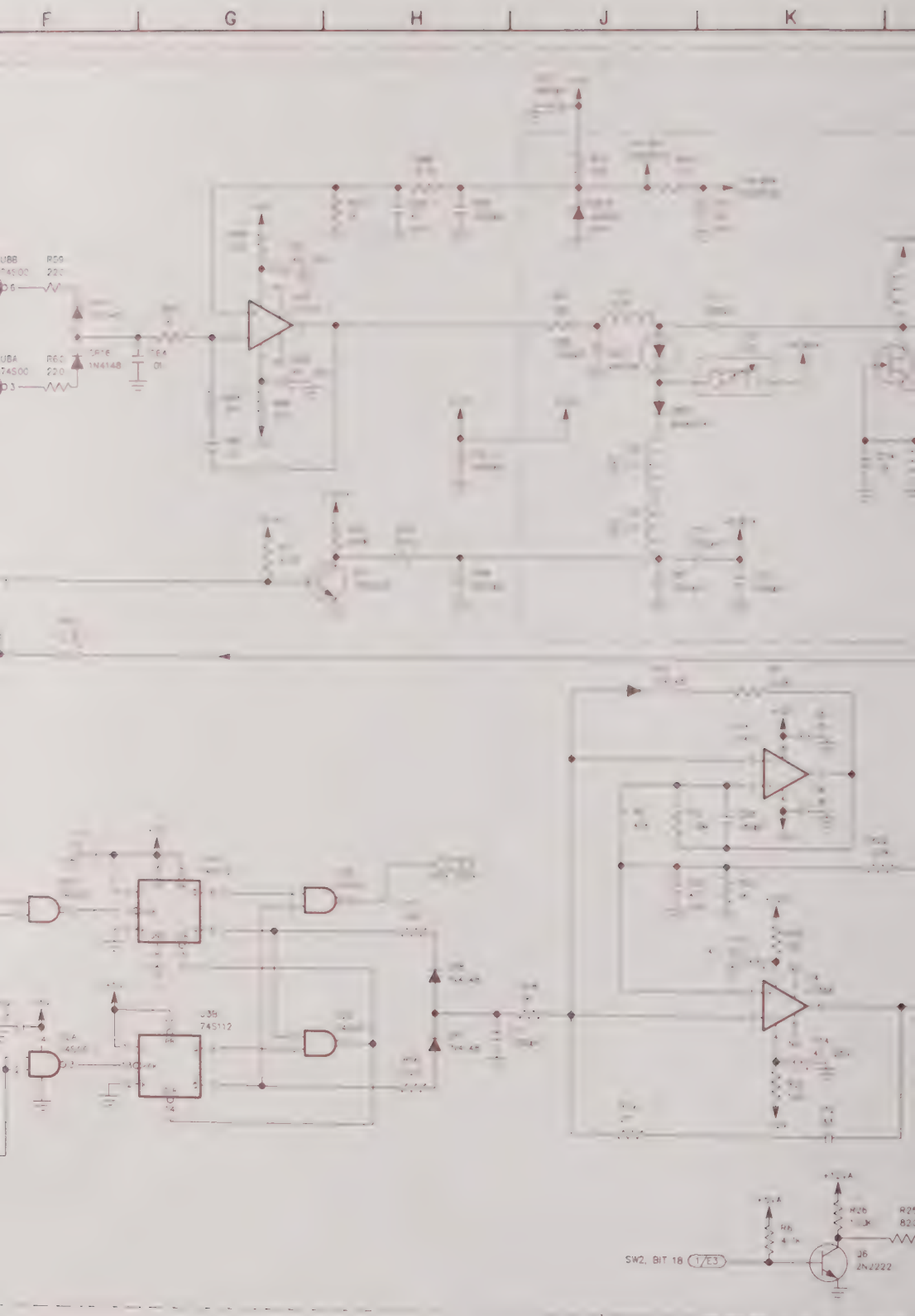


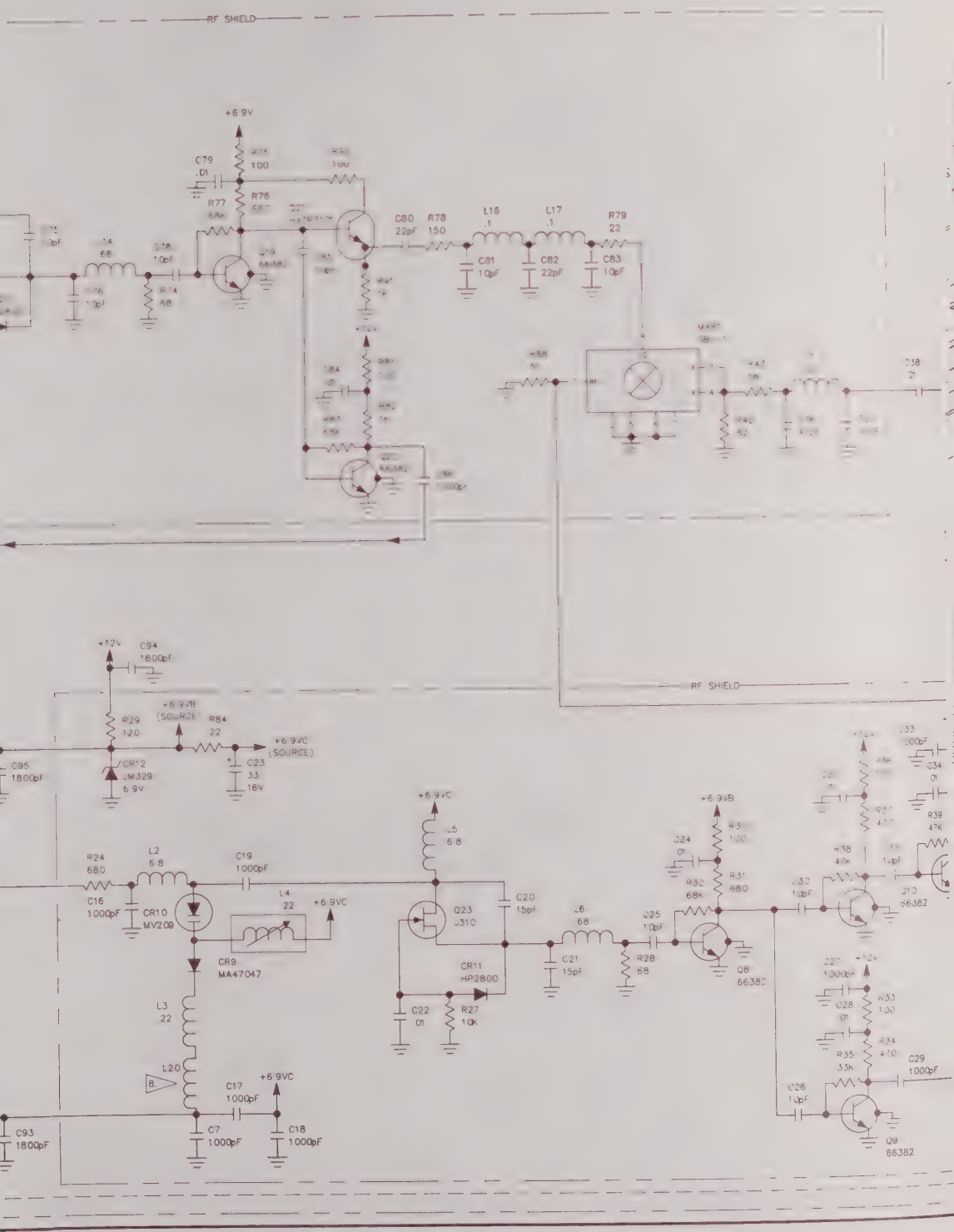
DETAIL **A**

DETAIL **B**

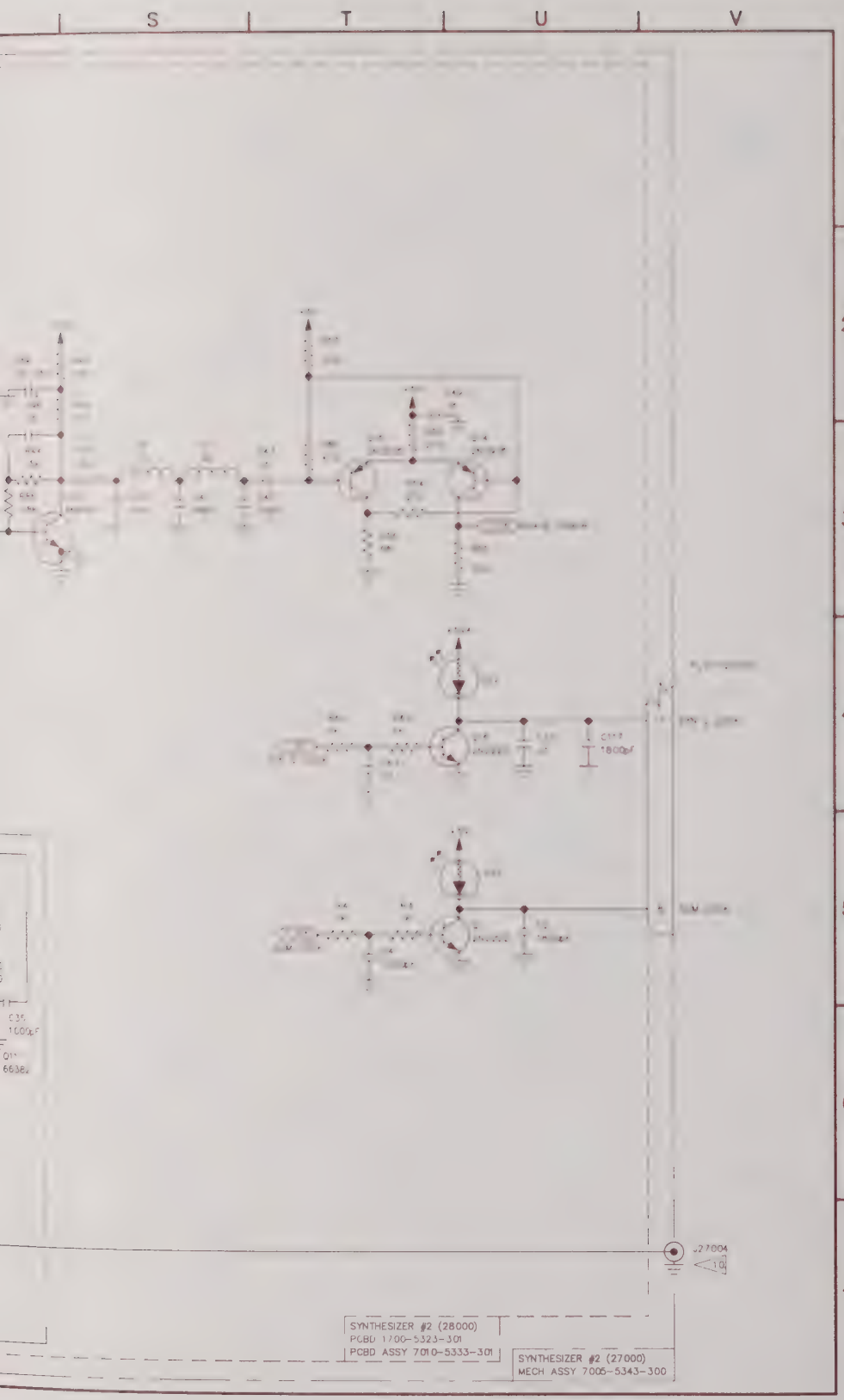
Figure 5-26 Synthesizer #2 Assembly (Sheet 1 of 2)
(0000-5313-301-C6)


A
B
C
D
E
1
2
3
4
5
6
7
J27002
800KHz
P/O P27001
+12V
+12V
+12V (SOURCE)
+12VA (SOURCE)
+5V
+5V
+5V (SOURCE)
CLOCK
DATA
LATCH
NC
NC
NC
NC
C56 1800pF
C57 1800pF
C58 1800pF
C105
C108
C112
C115
U7 MC145156
U9 MC12015
Lower Ouput
-INPUT
C62 1000pF
-12V
-12V (SOURCE)
GND
GND
C3 1800pF
R57 1K
R58 2.2K
U6B 74S00
PHASE ERROR
R48 470
C45
R49 1.5K
U5 MC12013
C46 .01
R51 680
R50 680
U6C 74S00
C48 33, 10V
J27003
0.2 – 3.099MHz


F
G
H
J
K
U39
74S112
SW2, BIT 18
1/E3
J6
2N2222



L
M
N
P
Q
RF SHIELD
+6.9V
C79
.01
R77
R78
C80
22pF
R78
150
L16
.1
L17
.1
R79
22
C81
10pF
C82
22pF
C83
10pF
R74
68
+12V
C94
1800pF
R29
120
+6.9VB
(SOURCE)
R84
22
+6.9VC
(SOURCE)
C23
33
16V
C95
1800pF
CR12
LM329
6.9V
RF SHIELD
+6.9VC
L5
6.8
R24
680
L2
6.8
C19
1000pF
C16
1000pF
CR10
MV209
L4
22
+6.9VC
CR9
MA47047
Q23
J310
C20
15pF
L6
68
C21
15pF
R28
68
C25
10pF
CR11
HP2800
C22
.01
R27
10K
L3
22
L20
B.
C17
1000pF
+6.9VC
C7
1000pF
C18
1000pF
C93
1800pF
+6.9VB
R32
68K
R31
680
Q8
66382
C34
.01
R39
47K
Q10
66382
C28
.01
R35
33K
C29
1000pF
C26
10pF
Q9
66382


S
T
U
V
1
2
3
4
5
6
7
SYNTHESIZER #2 (28000)
PCBD 1700-5323-301
PCBD ASSY 7010-5333-301
SYNTHESIZER #2 (27000)
MECH ASSY 7005-5343-300

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 27000.
   B. PC BD ASSY - 28000.

2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

4. WHEN ÷10/$\overline{÷1}$ IS LOW, THE SUMMING OSCILLATOR IS SWITCHED TO HIGH RANGE WHEN THE SYNTHESIZED OSCILLATOR IS 125.0 MHz AND ABOVE.

5. WHEN ÷10/$\overline{÷1}$ IS HIGH, THE SUMMING OSCILLATOR IS SWITCHED TO HIGH RANGE WHEN THE SYNTHESIZED OSCILLATOR IS 150.0 MHz AND ABOVE.

6. R28092 IS SELECTED AT TEST (S.A.T.), AND USED AS REQUIRED.
   NOMINAL VALUE = 220Ω.

7. R28093 IS SELECTED AT TEST (S.A.T.) AND USED AS REQUIRED.
   NOMINAL VALUE = 47Ω.

8. L28018, L28019 AND L28020 ARE SELECTED AT TEST (S.A.T.)
   NOMINAL VALUE = .12 μH
   RANGE = .10 μH THRU .15 μH.

9. C28105 THRU C28116 ARE SELECTED AT TEST (S.A.T.) AND USED AS REQUIRED.
   NOMINAL VALUE = 1800 pF.

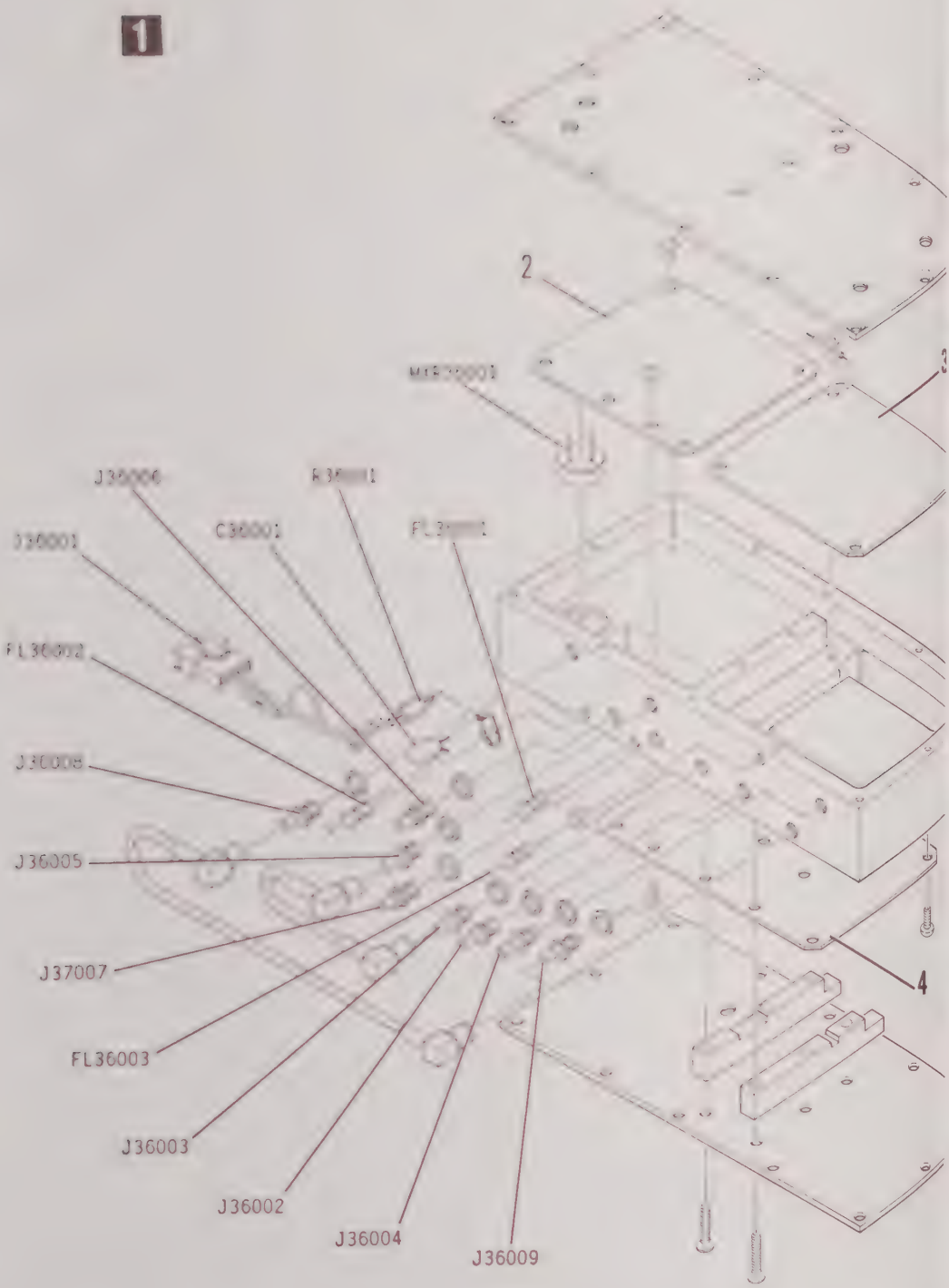
10. FREQUENCY RANGE AT J27004:
    100.71 MHz THRU 160.7 MHz.

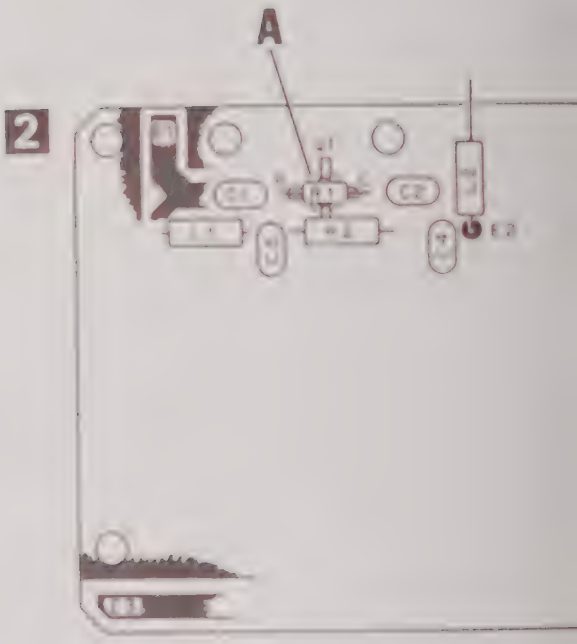
11. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

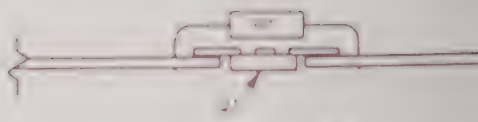
Figure 5-26 Synthesizer #2 Assembly (Sheet 2 of 2) (0000-5313-301-C6)

KEY:

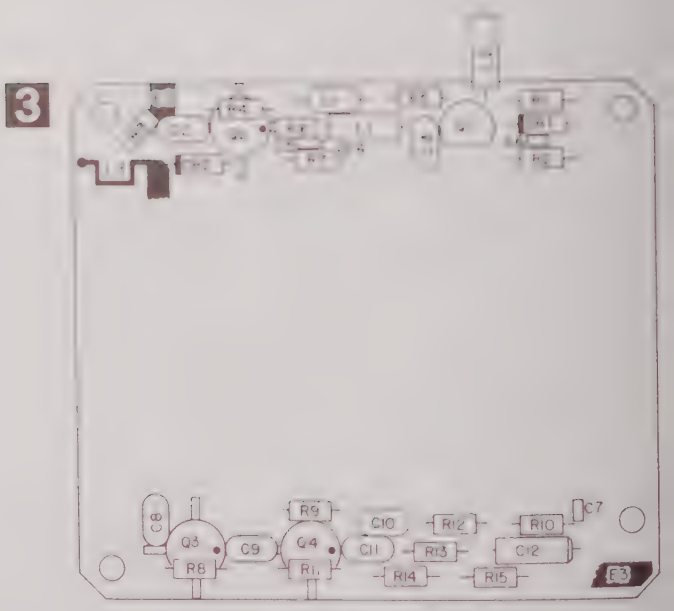
1. Second LO Summing Loop Assy (7005-5344-800-K)
2. Second LO Mixer PC Bd Assy (7010-5334-900-B2)
3. 1000 MHz Multiplier PC Bd Assy (7010-5335-000-B7)
4. 1160 MHz VCO PC Bd Assy (7010-5334-800-G1)


1
2
4
J36006
C36001
J36001
FL36002
J36008
J36005
J37007
FL36003
J36003
J36002
J36004
J36009

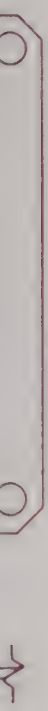




DETAIL A



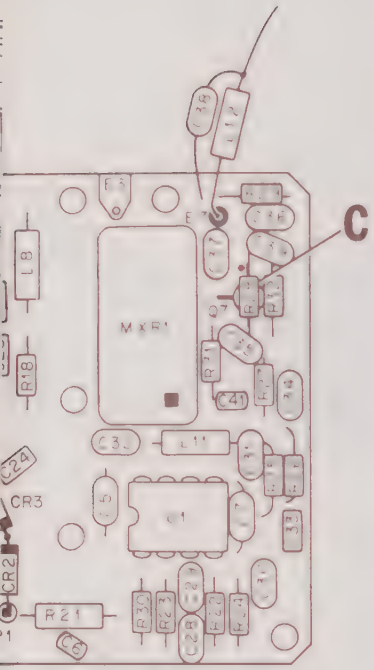
Top View



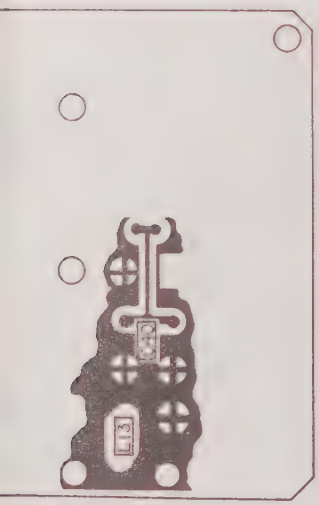
ottom View

Top View

B



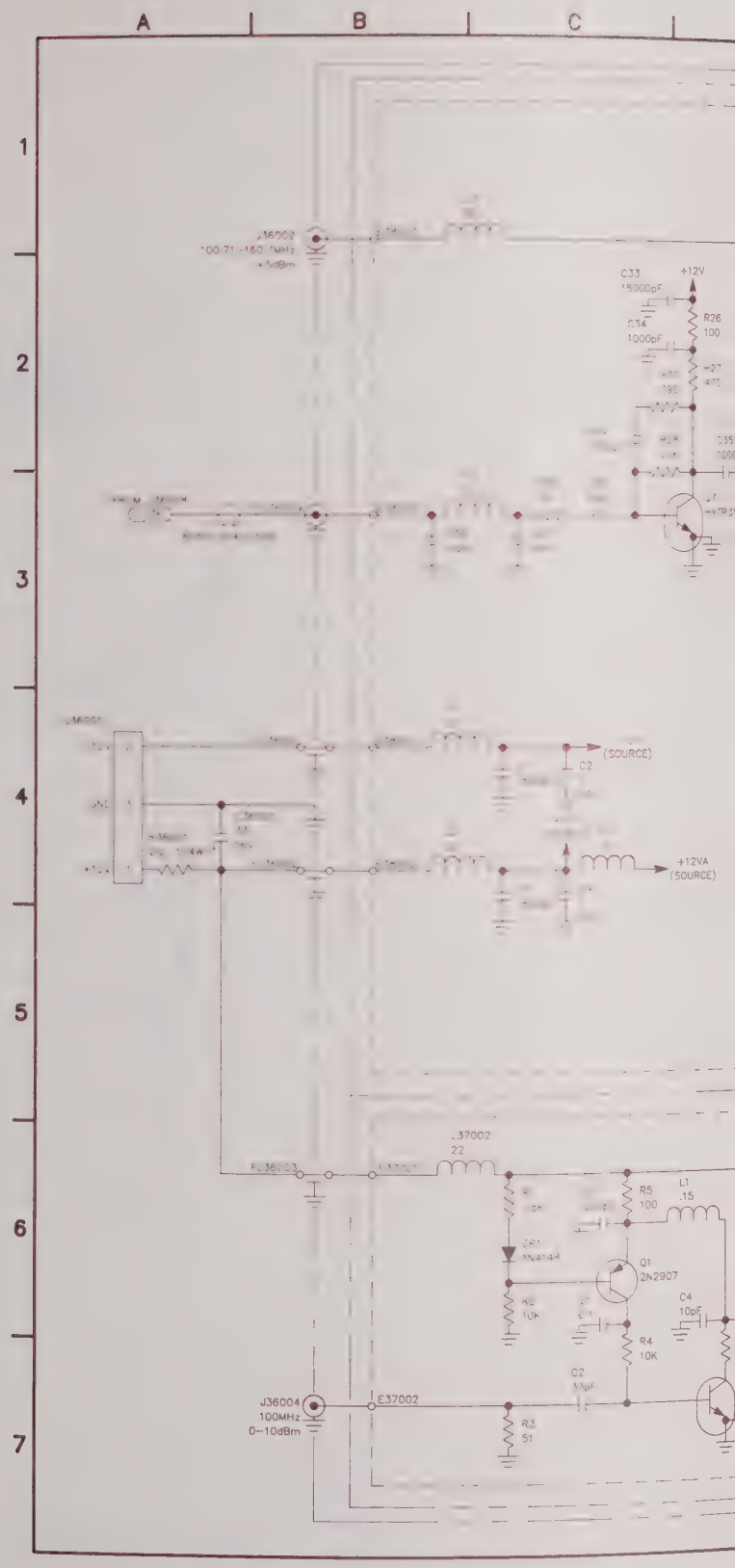
DETAIL **B**



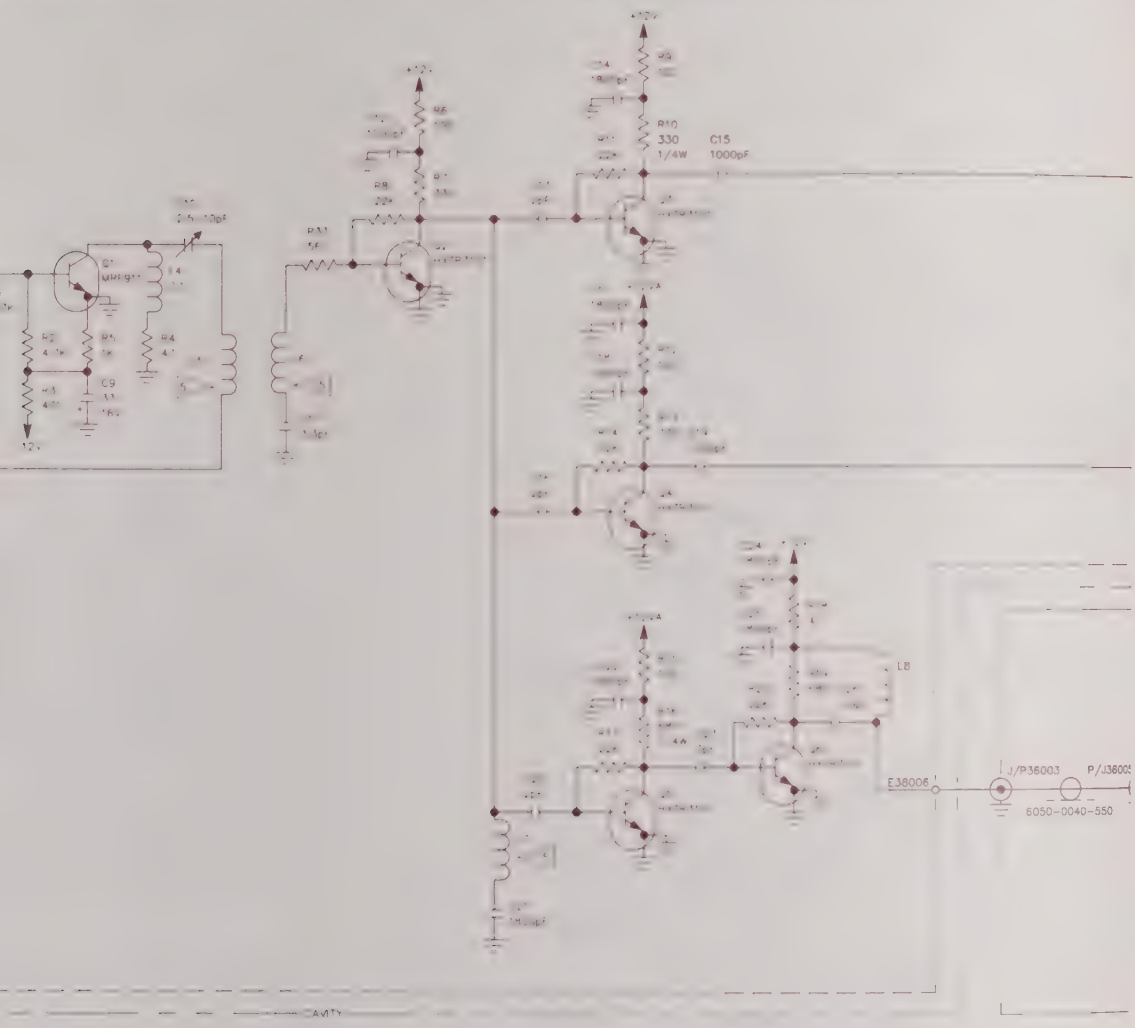
ottom View

DETAIL **C**

Figure 5-27 Second LO Summing Loop Assembly (Sheet 1 of 2) (0000-5314-800-N)


A
B
C
1
2
3
4
5
6
7
C33
1800DpF
+12V
R26
100
C34
1000pF
(SOURCE)
C2
+12VA
(SOURCE)
L37002
22
R5
100
L1
.15
Q1
2N2907
C4
10pF
R4
10K
C2
J36004
100MHz
0–10dBm
E37002
R3
51

1000MHz MULTIPLIER (37000)
PCBD 1700-5325-000
PCBD ASSY 7010-5335-000


K
L
M
N
P
R10
330
1/4W
C15
1000pF
LB
E38006
J/P36003
6050-0040-550

Q
R
S
T
1
2
3
4
5
6
7

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY SERIES:

   A. MECH ASSY - 36000.
   B. 1000 MHz MULTIPLIER PC BD ASSY - 32000.
   C. 1160 MHz VCO PC BD ASSY - 38000.
   D. 2ND L.O. MIXER PC BD ASSY - 18000.

2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

4. C38030 IS SELECTED AT TEST (S.A.T.), NOMINAL VALUE = 4700 pF
   RANGE = 1800 pF THRU 4200 pF.

5. L38005, L38006 & L38007 ARE .2" LENGTH OF 22 GA. BUS WIRE.

6. R37013, R37014 & R37015 ARE SELECTED AT TEST (S.A.T.) AND SHOULD BE CHANGED AT THE SAME TIME TO MAINTAIN 50Ω IMPEDANCE.

   10 dB PAD: R37013 = 82Ω, R37014 = 82Ω, R37015 = 82Ω
   8.5 dB PAD: R37013 = 56Ω, R37014 = 110Ω, R37015 = 110Ω
   7.7 dB PAD: R37013 = 51Ω, R37014 = 120Ω, R37015 = 120Ω

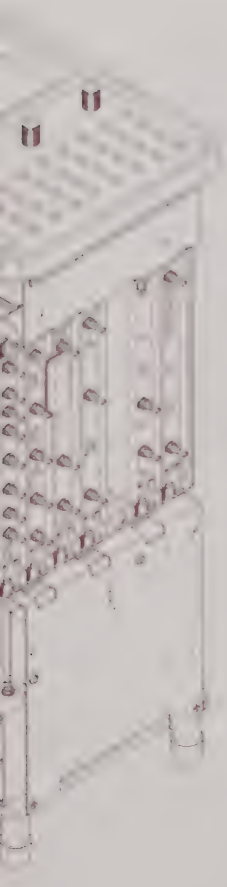
7. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

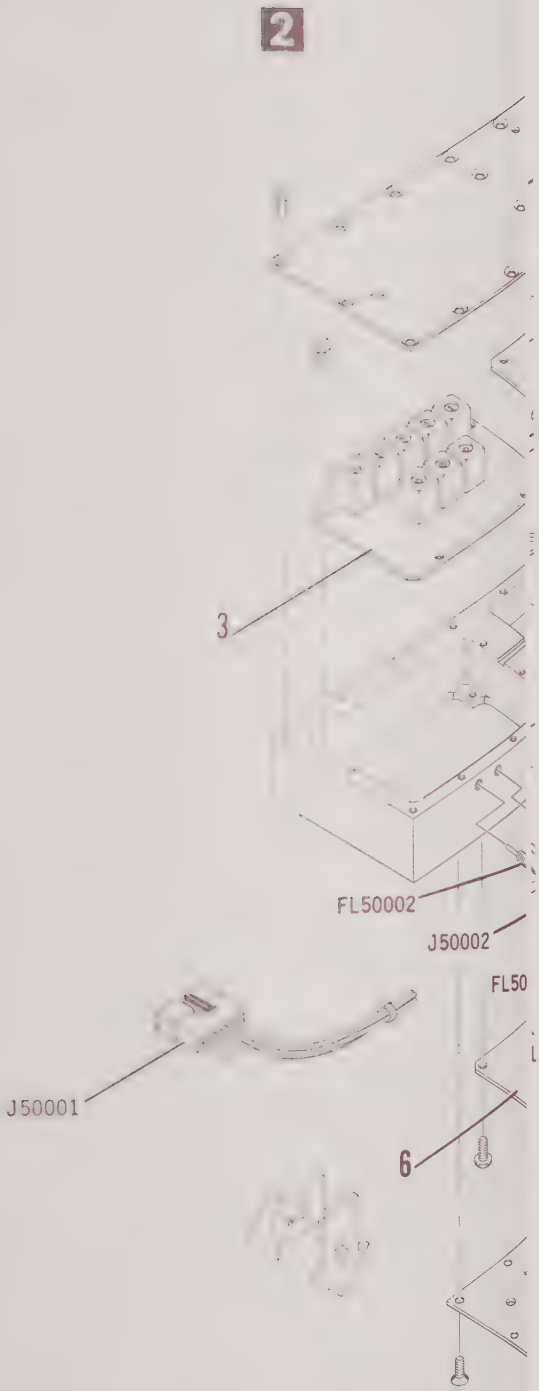
Figure 5-27 Second LO Summing Loop Assembly (Sheet 2 of 2) (0000-5314-800-N)

KEY

1. Tracking Generator Installatio
   (1 of 2) (7001-5343-800-D)
2. Generator Assy (7005-5341-000-
3. Generate Source PC Bd Assy
   (7010-5331-100-B5)
4. Generate Amp PC Bd Assy
   (7010-5331-000-D6)
5. 1000 MHz Low-Pass Filter PC Bd
   (Stripline) (1700-5122-200-A3)
6. 1300 MHz Generate IF PC Bd Ass
   (7010-5336-000-C2)

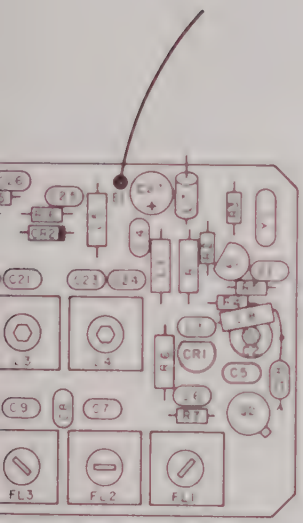
ssy

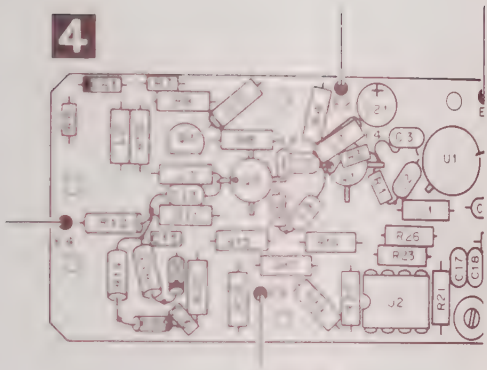




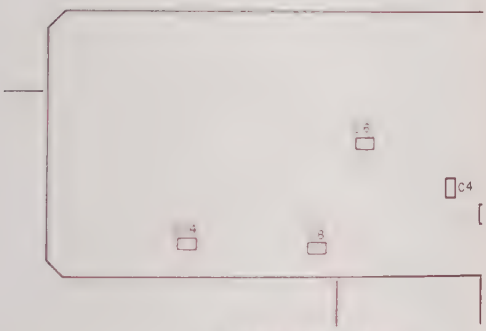
4
5
J50006
J50007
FL50004
FL50005
J50005
FL50003
J50003
J50004
MXR50002
MXR50001

3

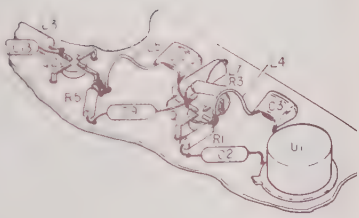




Top View



Bottom View



DETAIL **A**

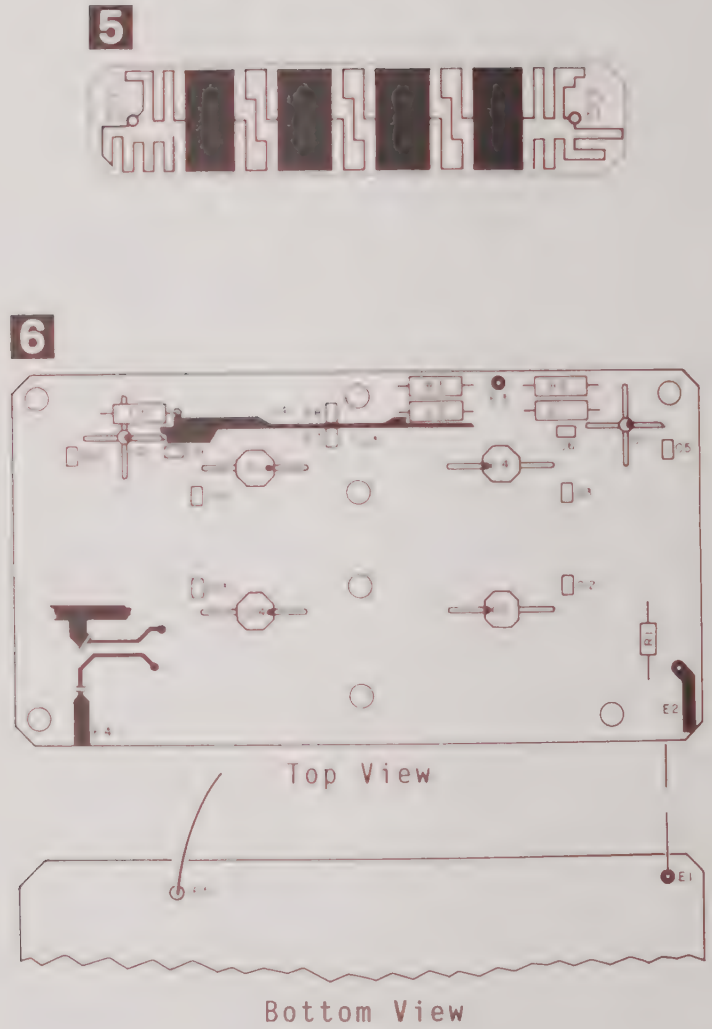
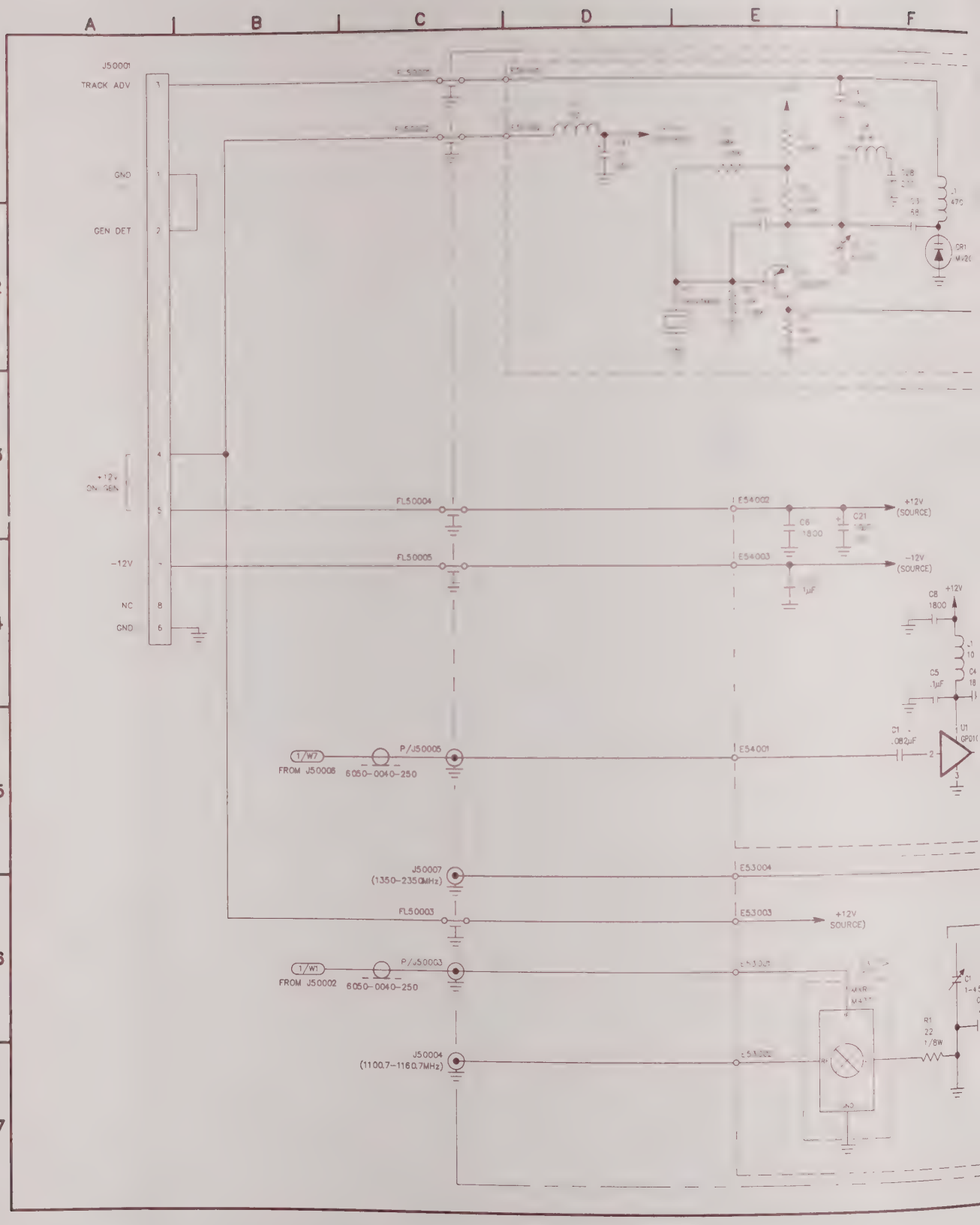
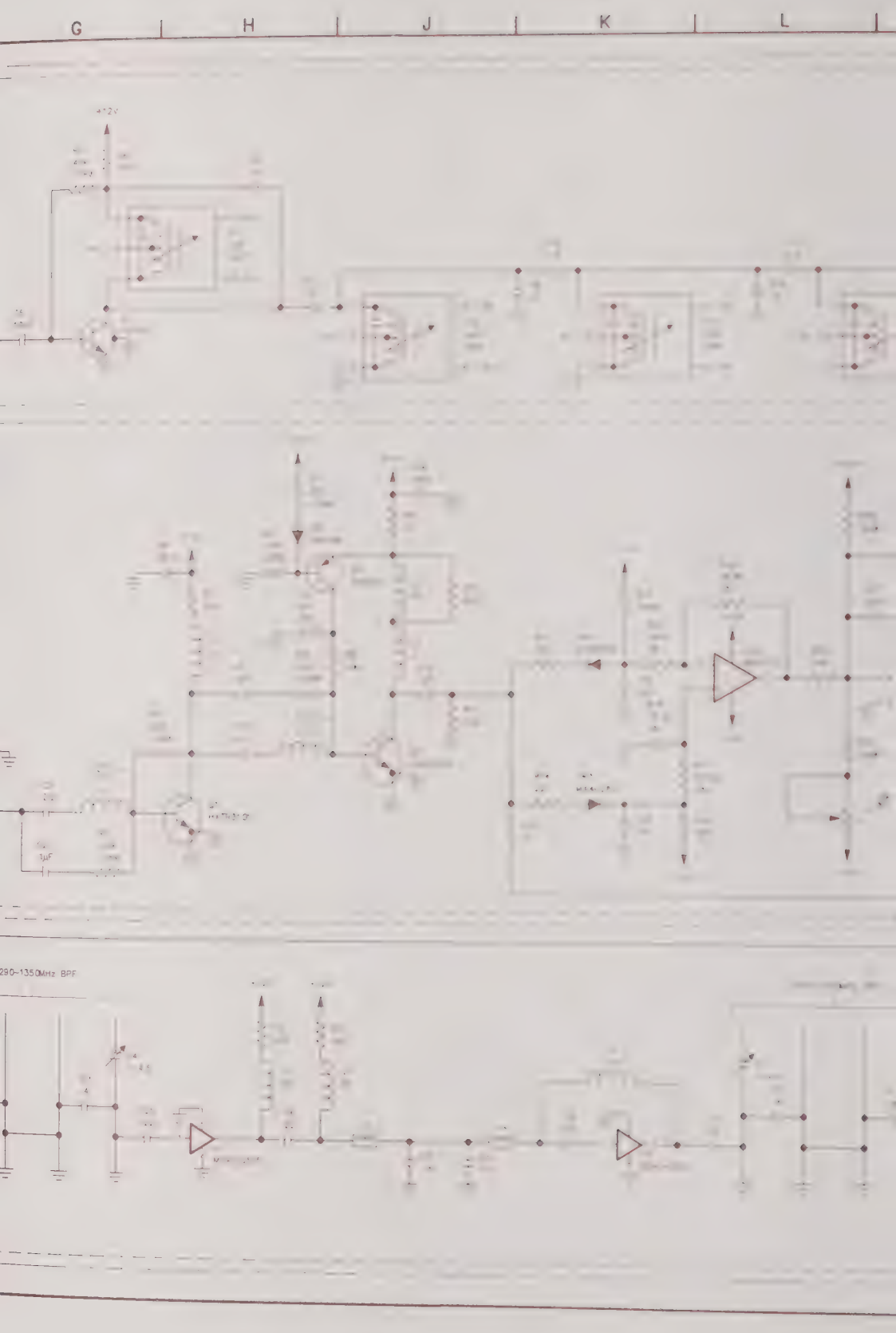
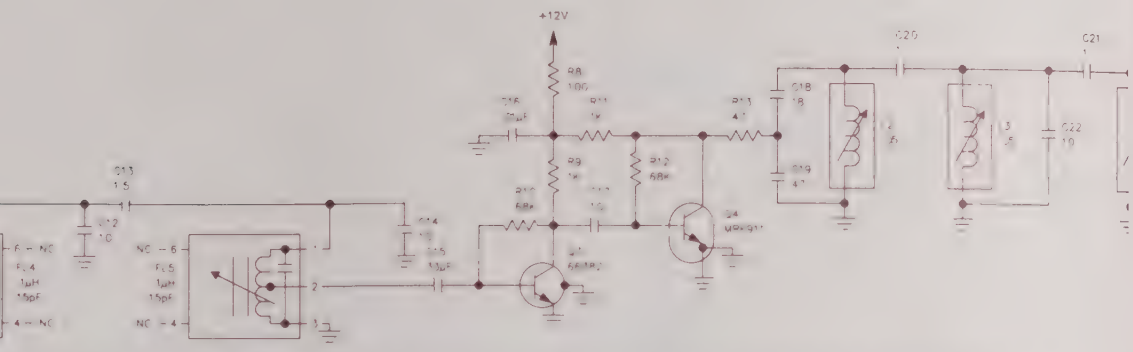


Figure 5-28 Tracking Generator Installation (Sheet 1 of 6) (0000-5311-000-N)


A
B
C
D
E
F
1
2
3
4
5
6
7
J50001
TRACK ADV
GND
GEN DET
+12V ON GEN
-12V
NC
GND
FL50004
FL50005
E54002
E54003
+12V (SOURCE)
-12V (SOURCE)
C6 1800
C21
1µF
C8 1800
C5 .1µF
C4 18
C1 .082µF
U1
1/W7
FROM J50008
P/J50005
6050-0040-250
E54001
J50007 (1350-2350MHz)
E53004
FL50003
E53003
+12V SOURCE)
1/W1
FROM J50002
P/J50003
J50004 (1100.7-1160.7MHz)
R1 22 1/8W

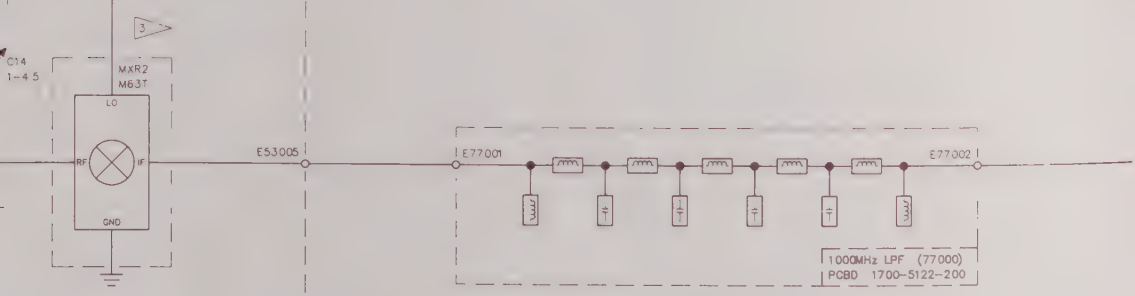

G
H
J
K
L
+12V
3μF
290~1350MHz BPF



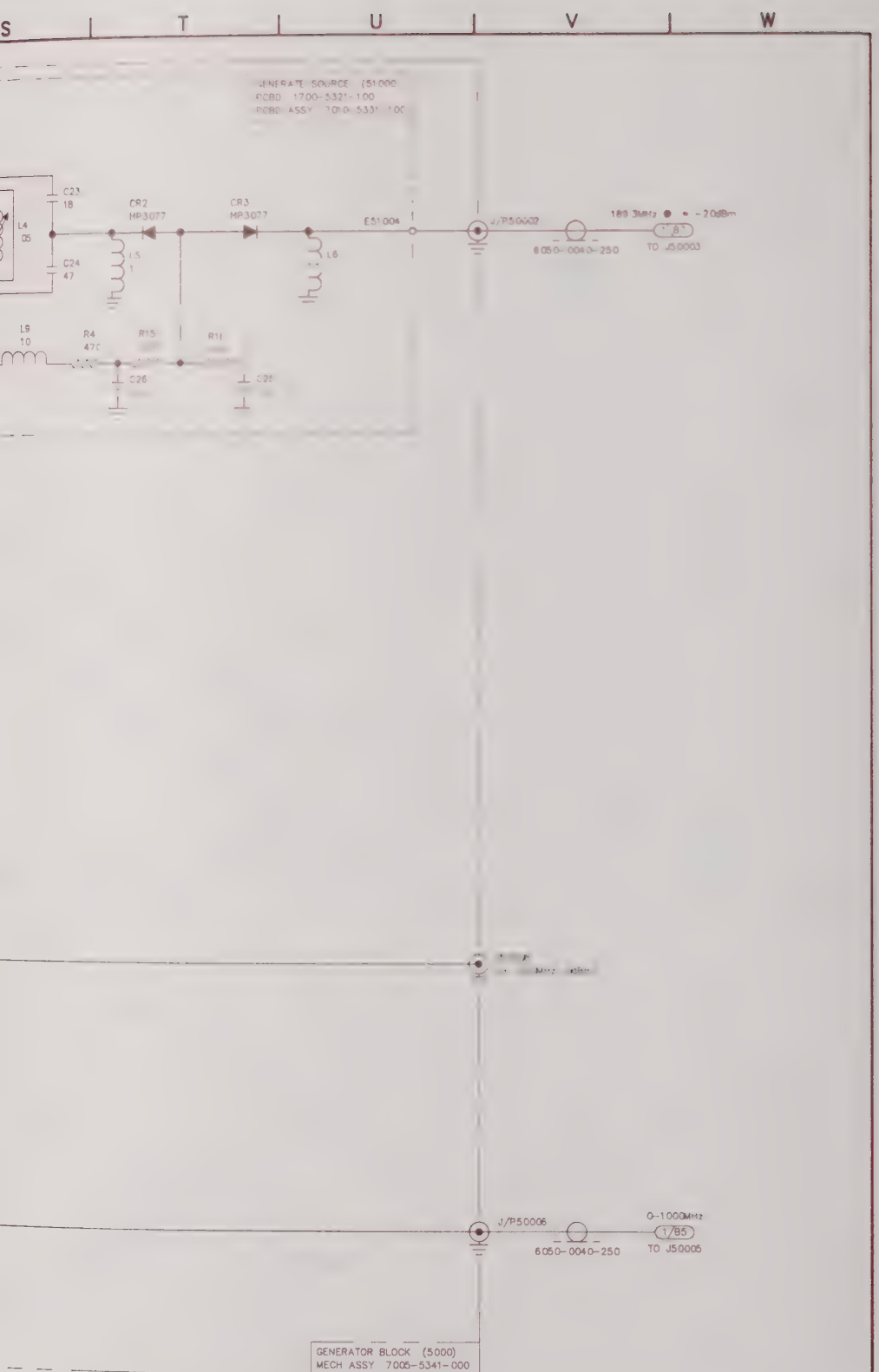
T LEVEL ADJUST

E54004

1300MHz GEN. IF (53000)
PCBD 1700-5326-000
PCBD ASSY 1010-5336-000



1000MHz LPF (77000)
PCBD 1700-5122-200


S
T
U
V
W
GENERATE SOURCE (5100)
PCBD 1700-5321-100
PCBD ASSY 7010-5331-100
C23
18
L4
05
C24
47
CR2
MP3077
CR3
MP3077
L5
1
L6
E51004
J/P50002
6050-0040-250
TO J50003
L9
10
R4
47C
R15
R11
C26
C25
J/P50006
6050-0040-250
0-1000MHz
TO J50005
GENERATOR BLOCK (5000)
MECH ASSY 7005-5341-000

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY THE FOLLOWING SERIES:

   A. MECH ASSY - 50000
   B. GENERATE SOURCE PC BD ASSY - 51000
   C. 1300 MHz GENERATE IF PC BD ASSY - 53000
   D. GENERATE AMP PC BD ASSY - 54000

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. MXR5001 AND MXR5002 ARE INSTALLED AT MECHANICAL ASSEMBLY LEVEL.

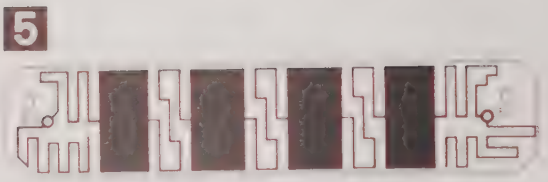
4. L54004 IS 0.4" LENGTH OF C54003 LEAD.

5. L54005 IS 0.4" LENGTH OF C54010 LEAD.

6. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (µF).

7. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (µH).

Figure 5-28 Tracking Generator Installation (Sheet 2 of 6) (0000-5311-000-N)



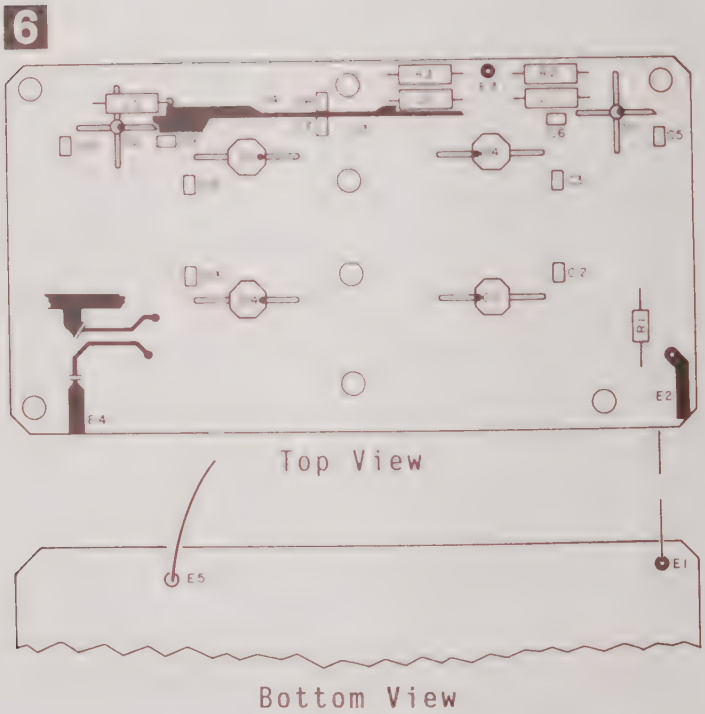
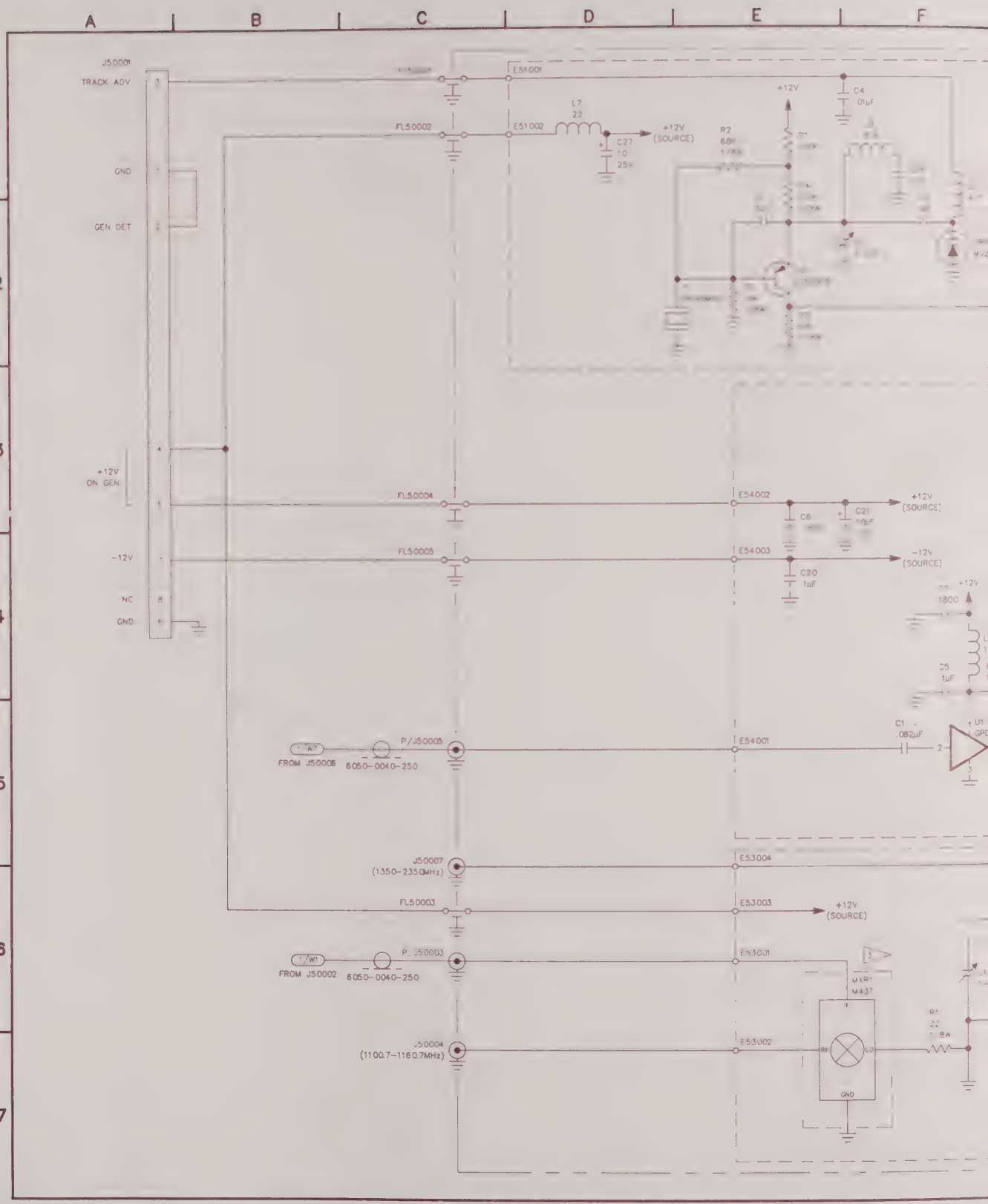
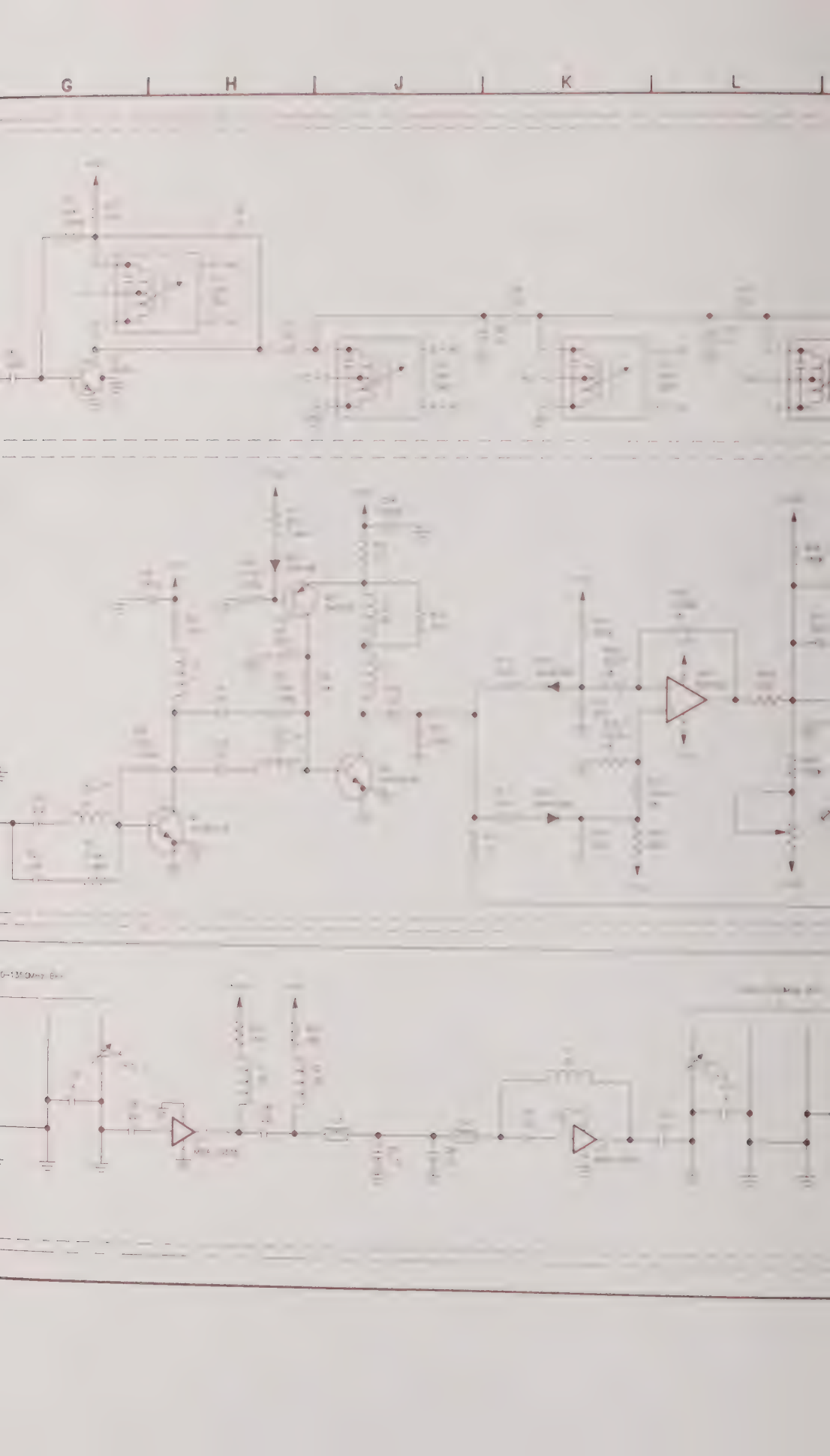
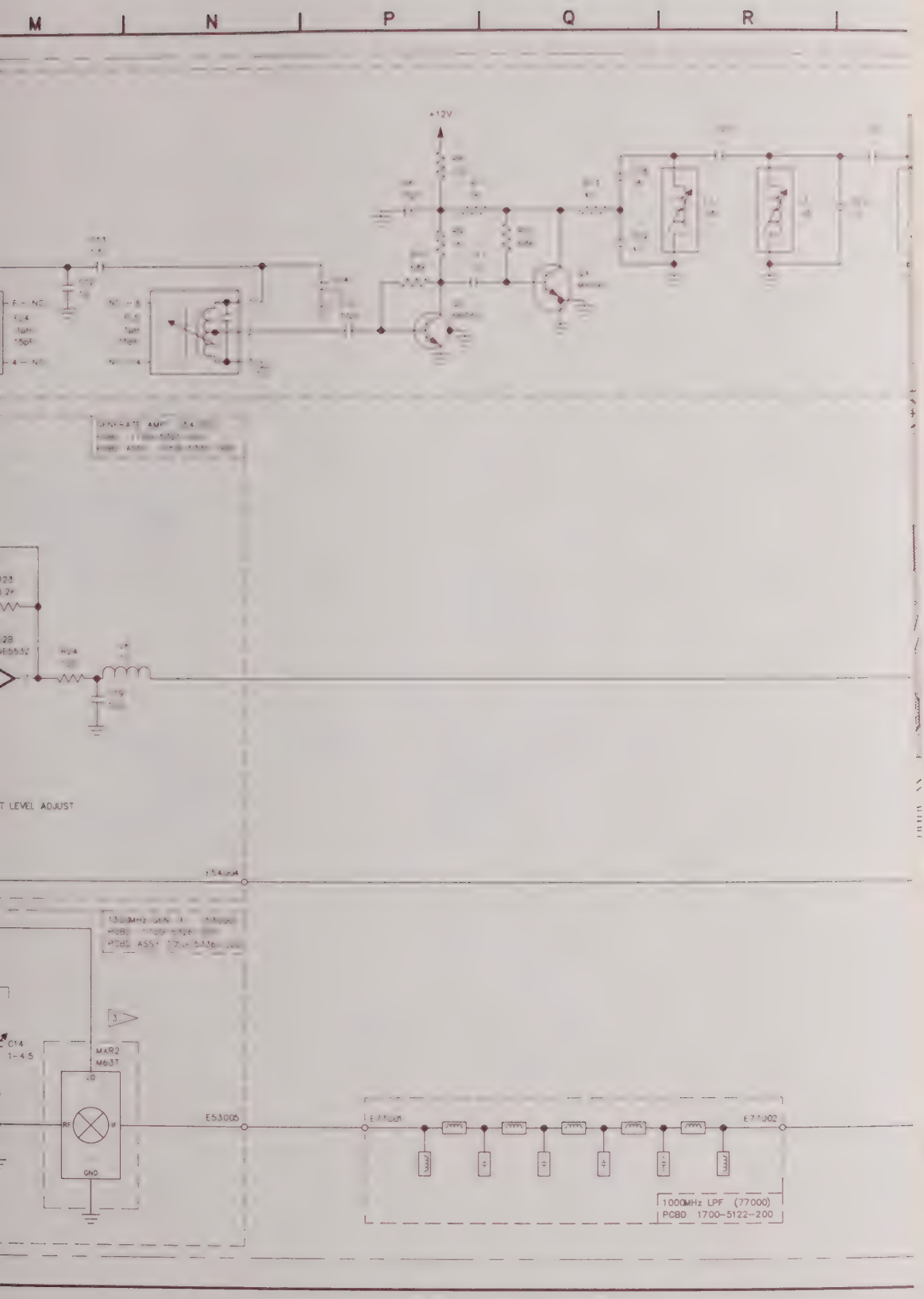
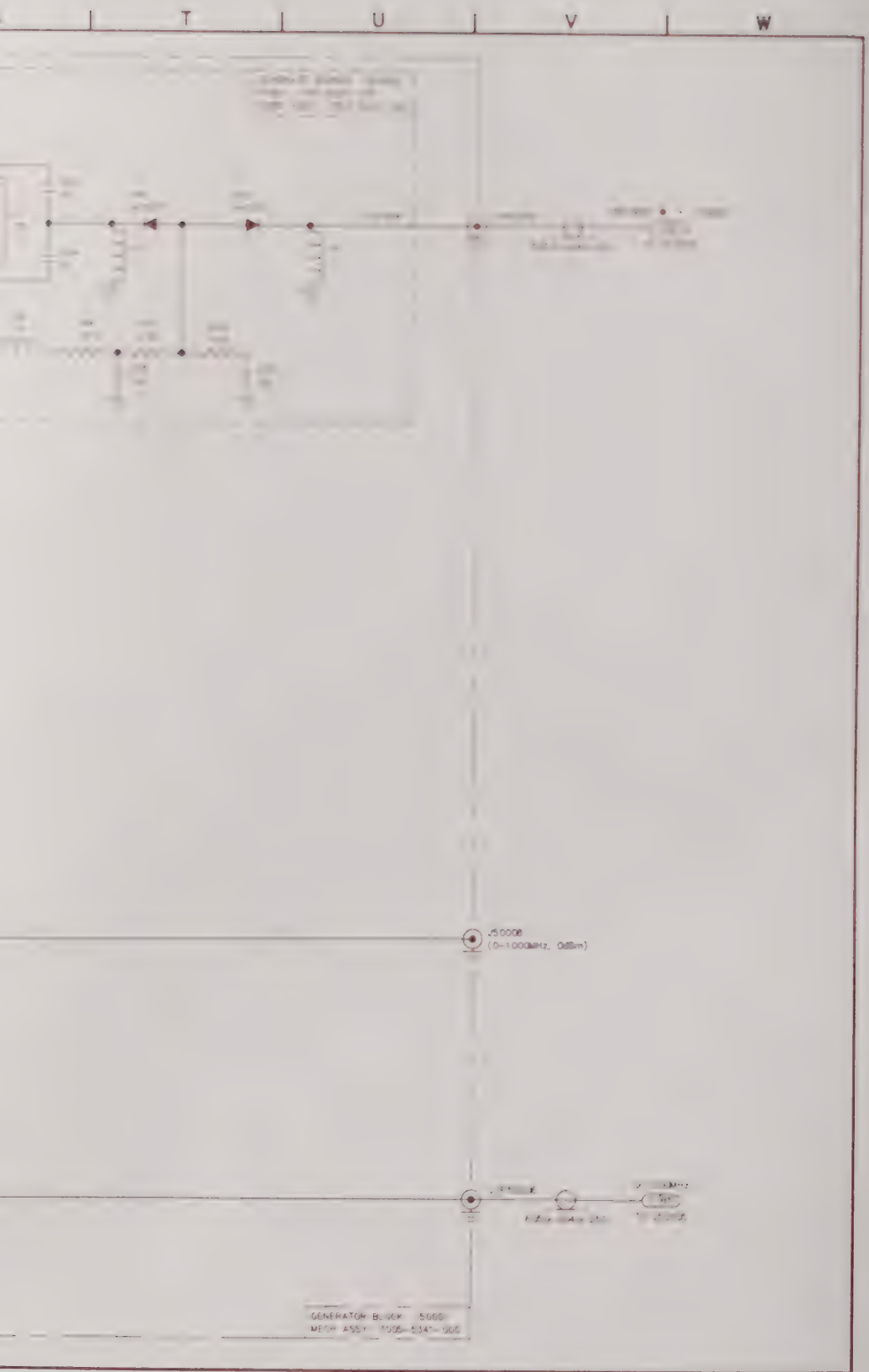


Figure 5-28 Tracking Generator Installation (Sheet 1 of 6) (0000-5311-000-N)


A
B
C
D
E
F
1
2
3
4
5
6
7
J50001
TRACK ADV
GND
GEN DET
+12V ON GEN
-12V
NC
GND
FL50002
E51001
E51002
L7
22
C27
10
25V
+12V (SOURCE)
R2
68K
C4
.01µF
FL50004
E54002
C6
C21
FL50005
E54003
C20
1µF
-12V (SOURCE)
1800
C5
1µF
C1
.082µF
P/J50005
E54001
FROM J50006
6050-0040-250
J50007
(1350-2350MHz)
E53004
FL50003
E53003
P/J50003
E53001
FROM J50002
6050-0040-250
J50004
(1100.7-1160.7MHz)
E53002
MXR
M437
RF
LO
IF
GND
R1
22
1 8W


G
H
J
K
L


M
N
P
Q
R
+12V
T LEVEL ADJUST
MXR2
M63T
RF
IF
GND
E53005
1000MHz LPF (77000)
PCBD 1700-5122-200


T
U
V
W
50.000
(0-1000MHz, 0dBm)

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY THE FOLLOWING SERIES:

   A. MECH ASSY - 50000
   B. GENERATE SOURCE PC BD ASSY - 51000
   C. 1300 MHz GENERATE IF PC BD ASSY - 53000
   D. GENERATE AMP PC BD ASSY - 54000

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. MXR5001 AND MXR5002 ARE INSTALLED AT MECHANICAL ASSEMBLY LEVEL.

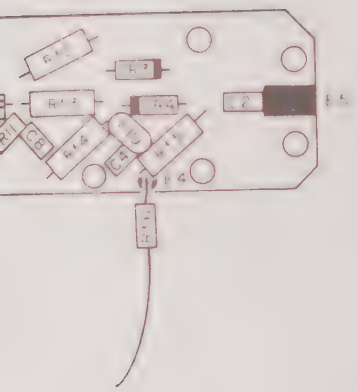
4. L54004 IS 0.4" LENGTH OF C54003 LEAD.

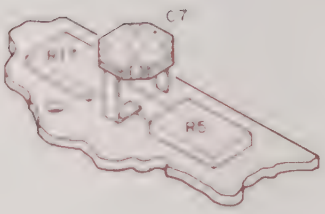
5. L54005 IS 0.4" LENGTH OF C54010 LEAD.

6. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

7. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

Figure 5-28 Tracking Generator Installation (Sheet 2 of 6) (0000-5311-000-N)



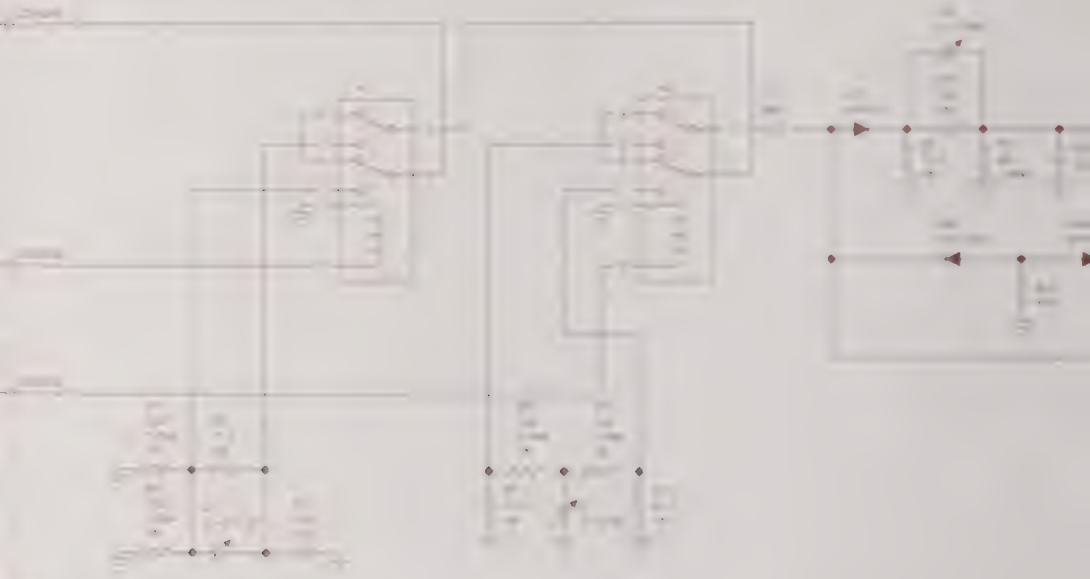


DETAIL **B**

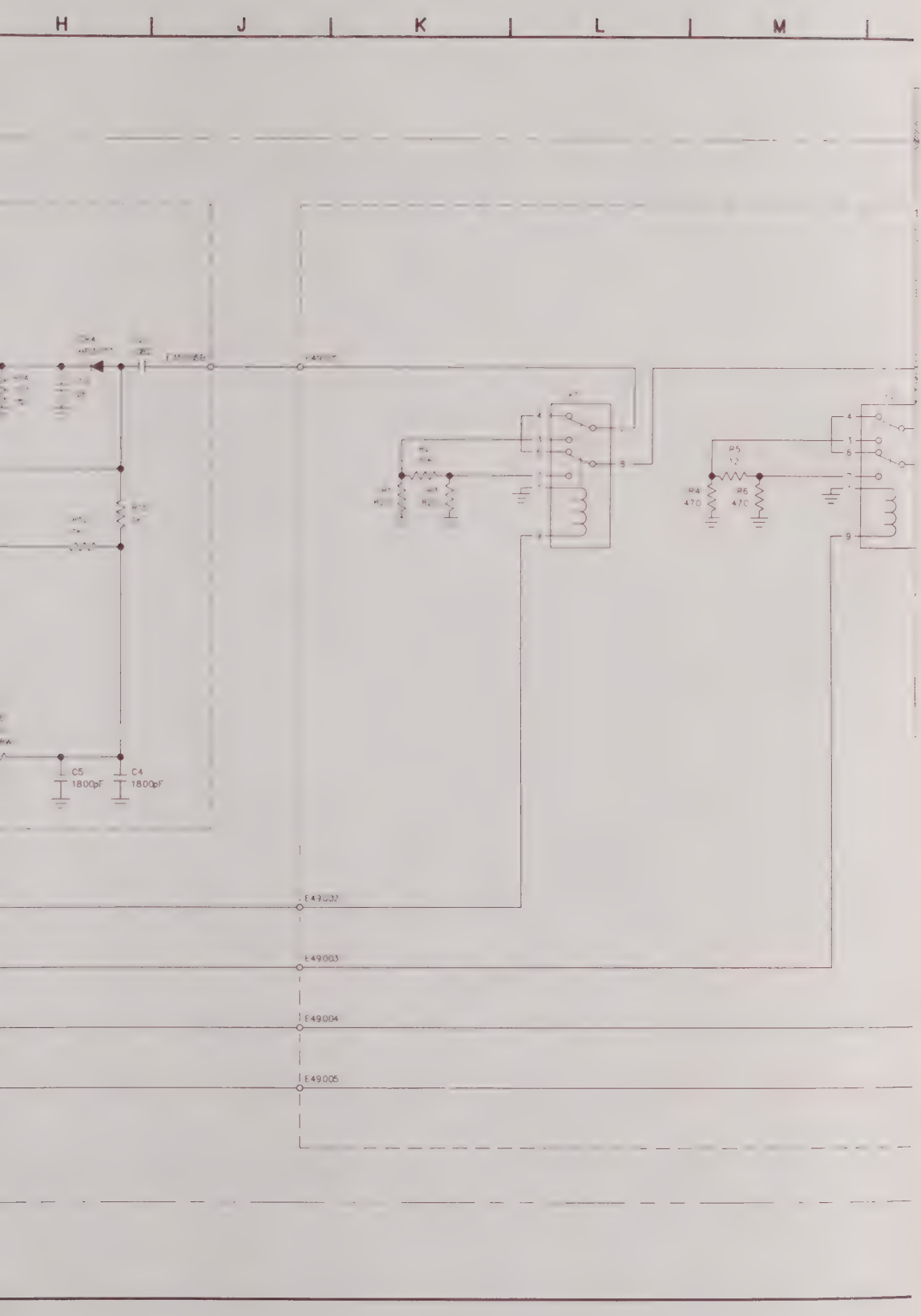
Figure 5-28 Tracking Generator Installation (Sheet 3 of 6) (0000-5310-201-N)

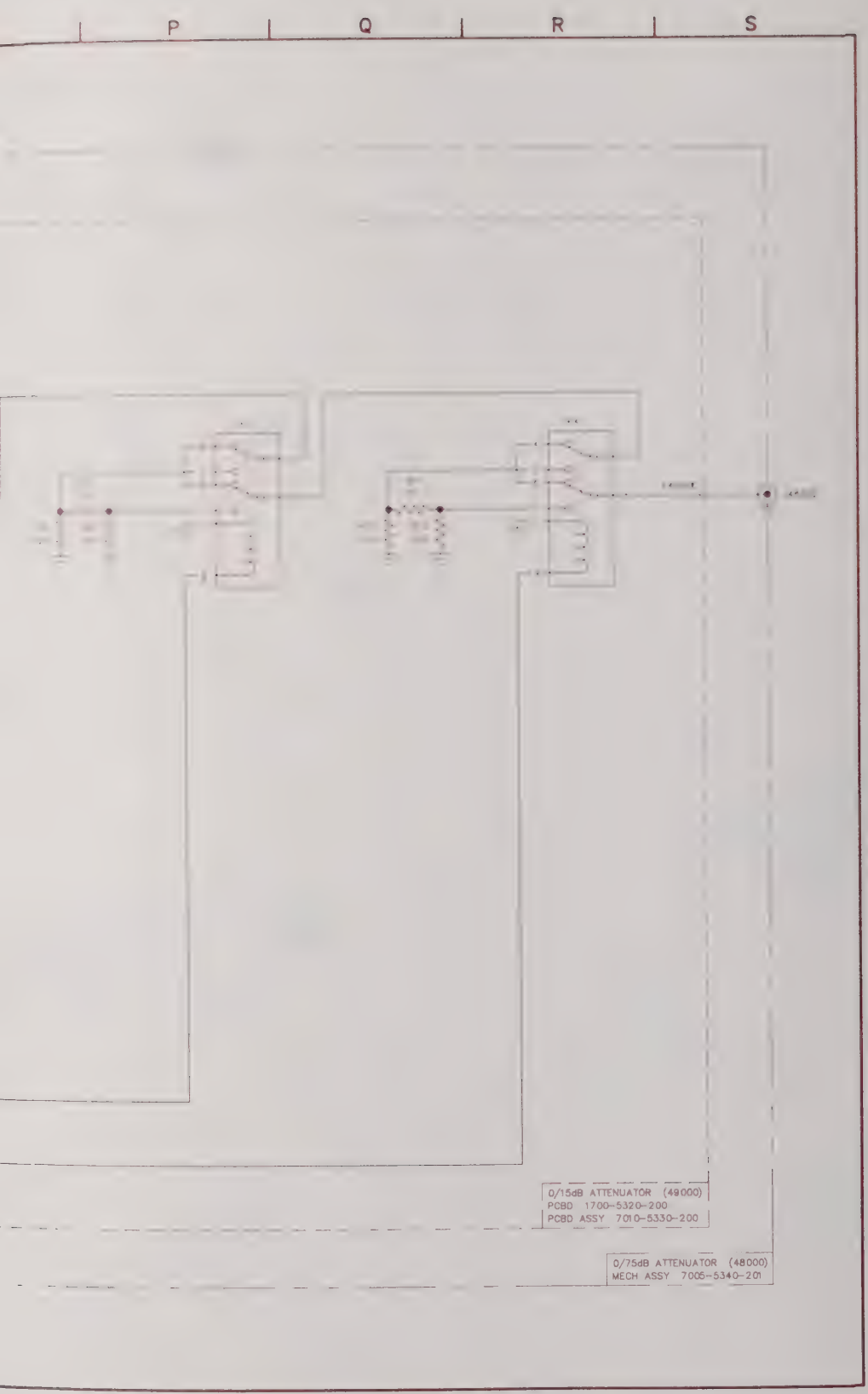
A
B
1
2
3
4
5
6
7
GEN. 1dB DET

C D E F G



0/60dB ATTENUATOR (35000B)
PCBD 1700-5320-100
PCBD ASSY 7010-5330-100


H
J
K
L
M
R5
12
R4
470
R6
470
C5
1800pF
C4
1800pF
E49002
E49003
E49004
E49005


P
Q
R
S
0/15dB ATTENUATOR (49000)
PCBD 1700-5320-200
PCBD ASSY 7010-5330-200
0/75dB ATTENUATOR (48000)
MECH ASSY 7005-5340-201

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY THE FOLLOWING SERIES:

   A. MECH ASSY - 48000
   B. 0-60 dB ATTENUATOR PC BD ASSY - 35000B
   C. 0-15 dB ATTENUATOR PC BD ASSY - 49000

2. ALL RESISTORS ARE 1/4W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (μF).

Figure 5-28 Tracking Generator Installation (Sheet 4 of 6) (0000-5310-201-N)

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY THE FOLLOWING SERIES:

   A. MECH ASSY - 6900B
   B. PC BD ASSY - 6800B

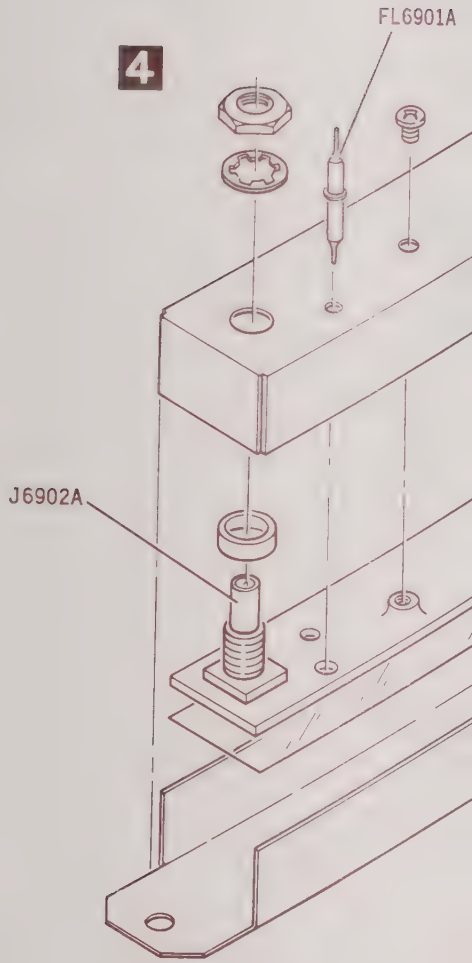
2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

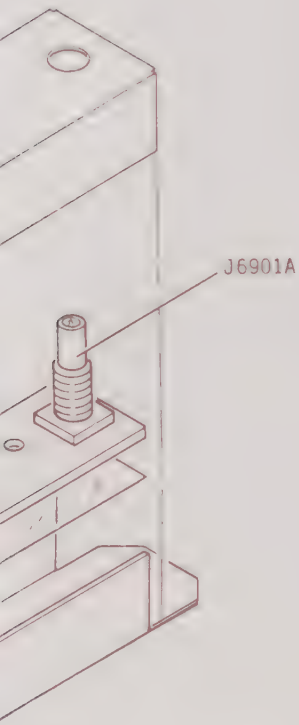
3. R6806 IS SELECTED AT TEST (S.A.T.).
   NOMINAL VALUE = 15Ω
   RANGE = 10Ω THRU 56Ω.

4. ALL CAPACITANCE IS EXPRESSED IN PICOFARADS (pF).

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

Figure 5-28 Tracking Generator Installation (Sheet 5 of 6) (0000-5016-800-A6)

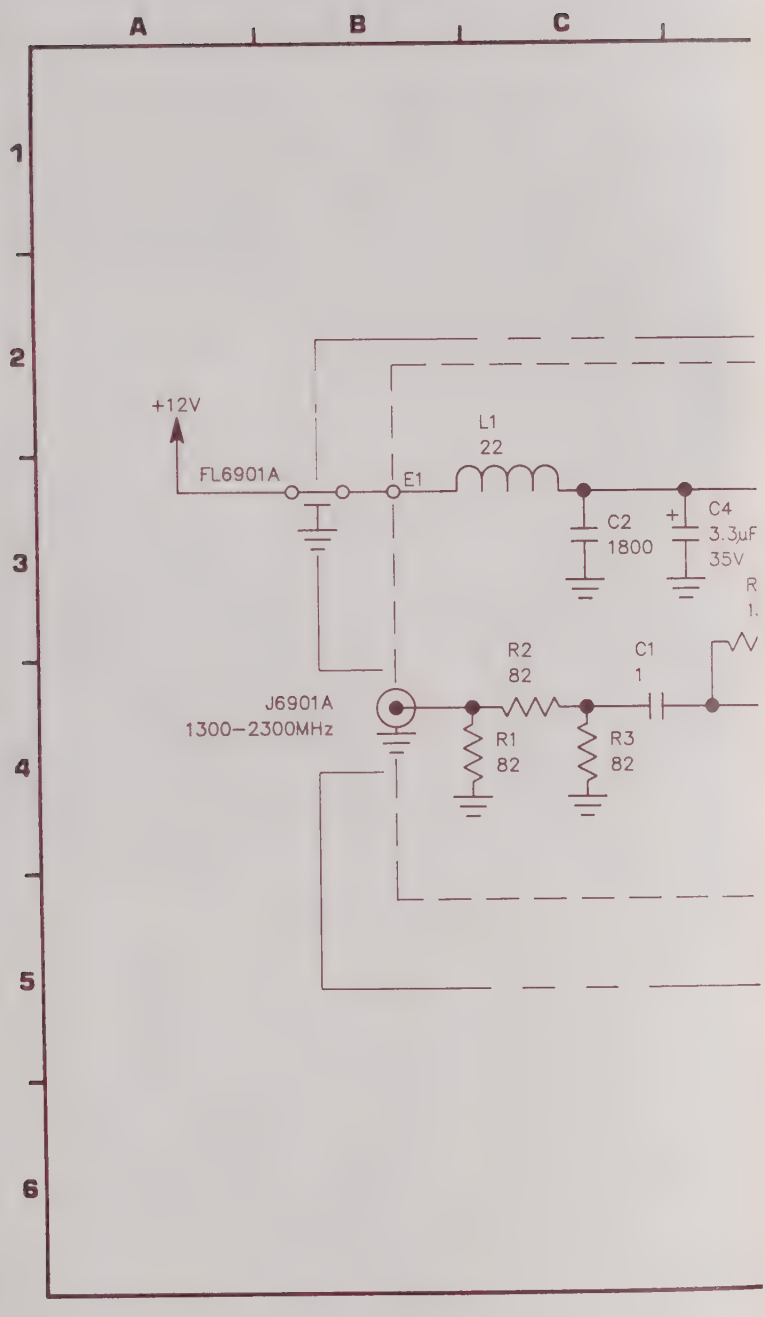

4
FL6901A
J6902A

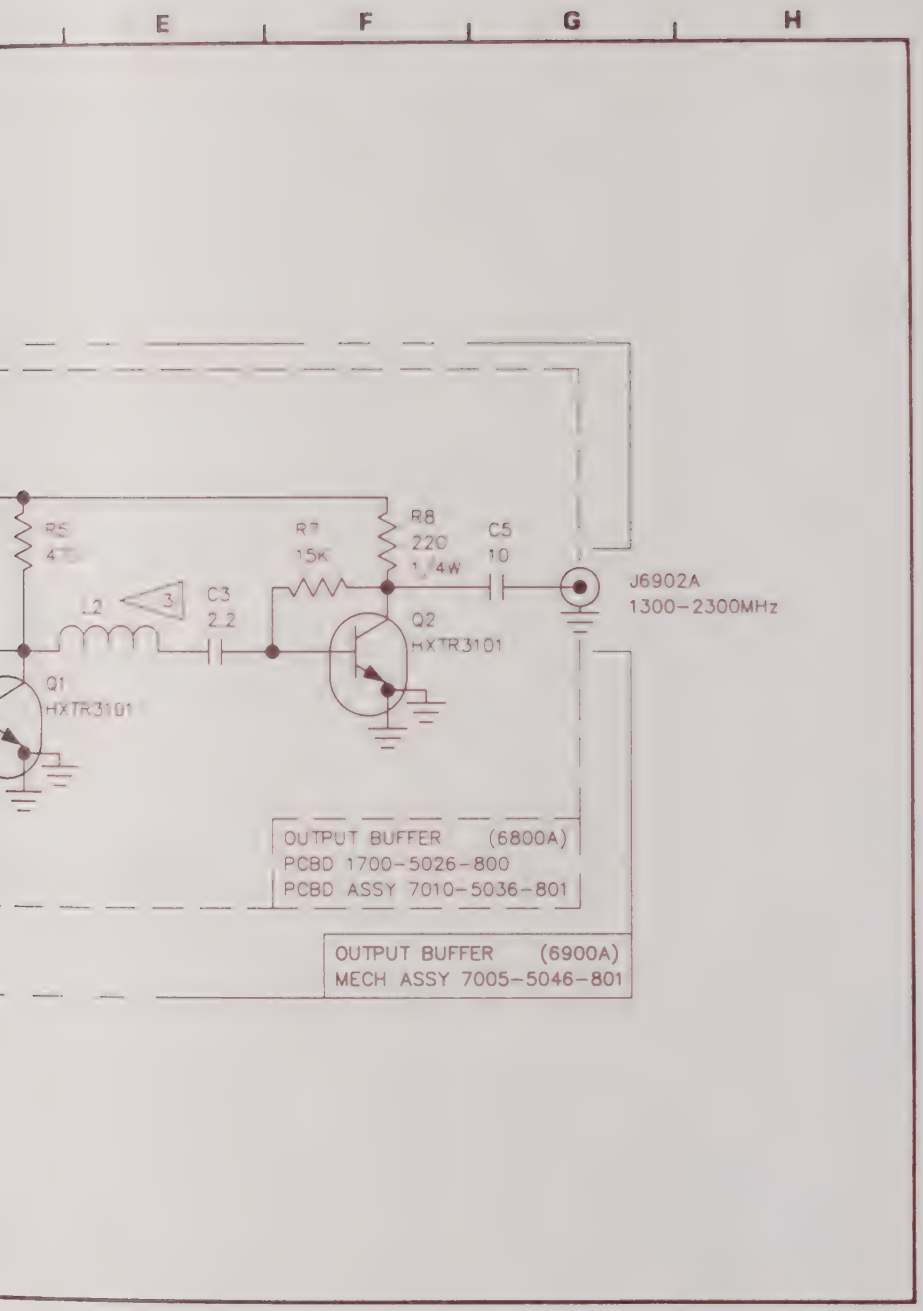


5

Top View

Bottom View


A
B
C
1
2
3
4
5
6
+12V
FL6901A
E1
L1
22
C2
1800
C4
3.3µF
35V
R2
82
C1
1
J6901A
1300–2300MHz
R1
82
R3
82


E
F
G
H
R5
4
R7
15K
R8
220
1/4W
C5
10
J6902A
1300–2300MHz
L2
3
C3
2.2
Q2
HXTR3101
Q1
HXTR3101
OUTPUT BUFFER (6800A)
PCBD 1700–5026–800
PCBD ASSY 7010–5036–801
OUTPUT BUFFER (6900A)
MECH ASSY 7005–5046–801

NOTES (UNLESS OTHERWISE STATED):

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THESE DRAWINGS CARRY THE FOLLOWING SERIES:

   A. MECH ASSY - 6900A
   B. PC BD ASSY - 6800A

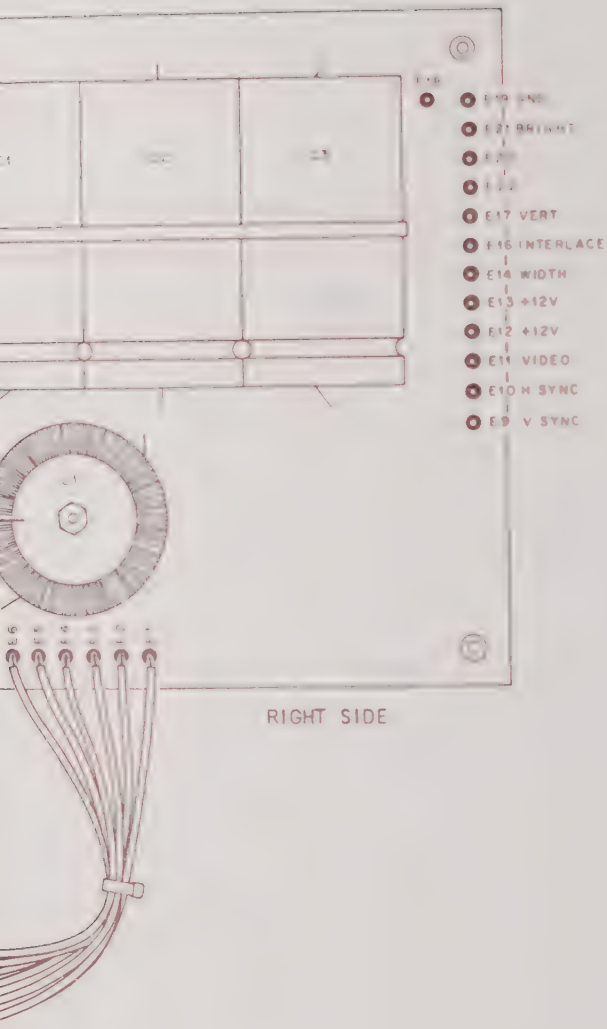
2. ALL RESISTORS ARE 1/8W, 5% TOLERANCE; RESISTANCE IS EXPRESSED IN OHMS (Ω).

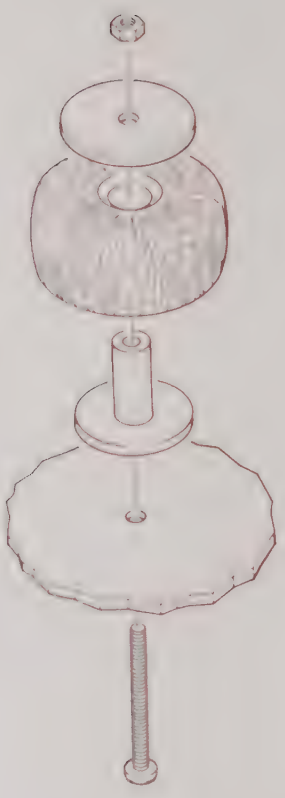
3. L6902 IS .35" LENGTH OF C6903 LEAD.

4. ALL CAPACITANCE IS EXPRESSED IN PICOFARADS (pF).

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS (μH).

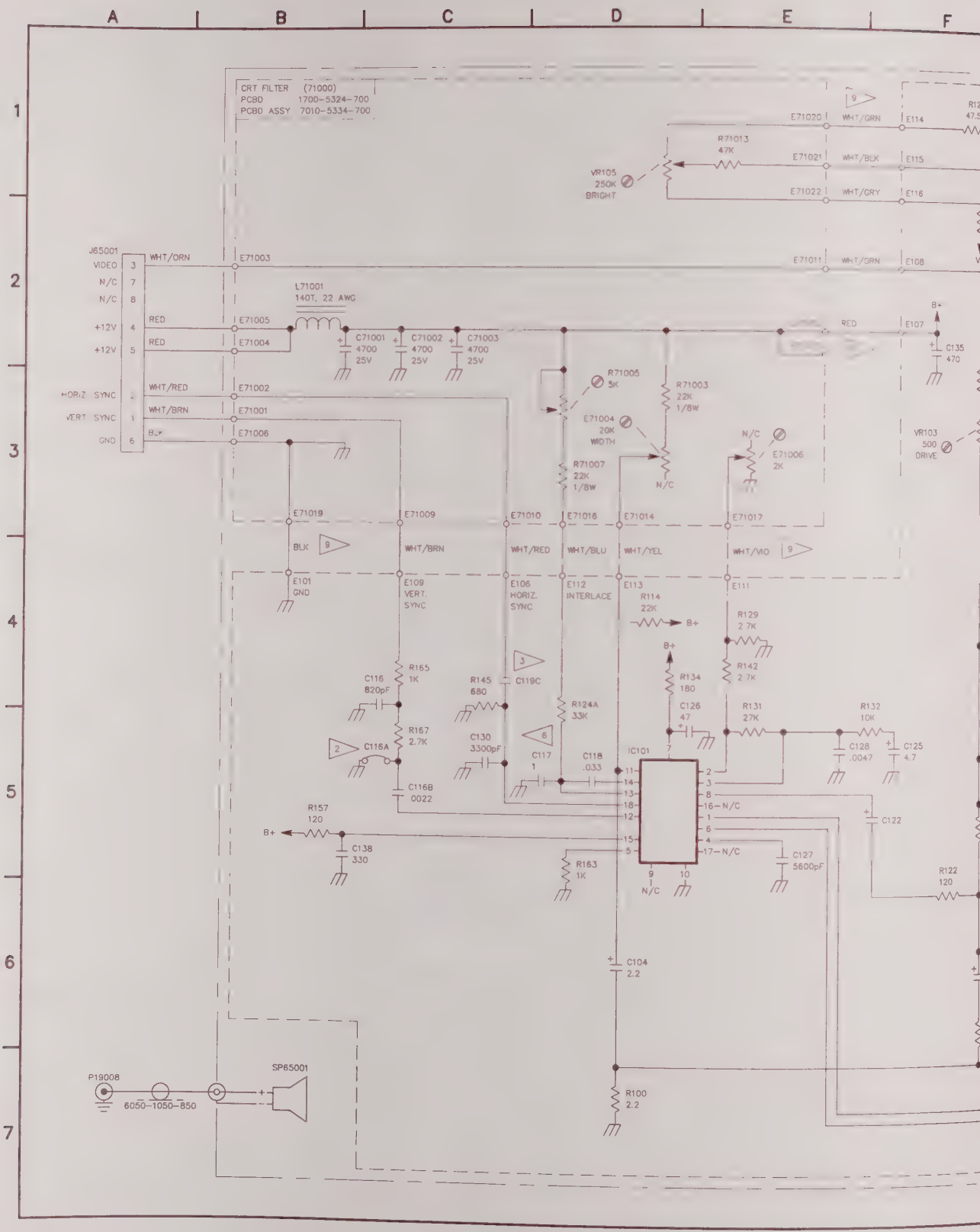
Figure 5-28 Tracking Generator Installation (Sheet 6 of 6) (0000-5016-801-A2)

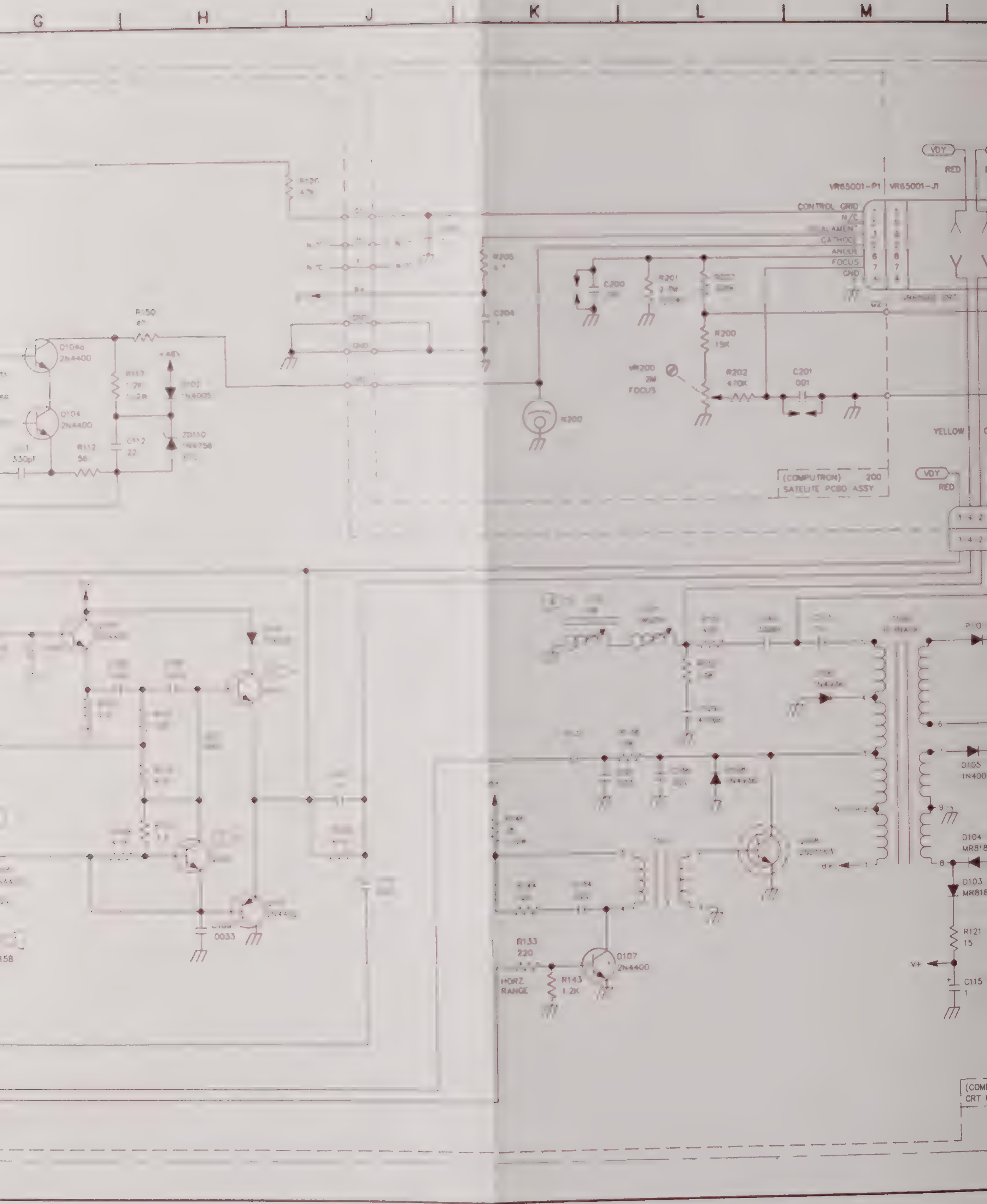




DETAIL **C**

Figure 5-29 CRT Display Assembly (Sheet 1 of 2)
(0000-5314-900)


A
B
C
D
E
F
1
2
3
4
5
6
7
CRT FILTER (71000)
PCBD 1700-5324-700
PCBD ASSY 7010-5334-700
J65001
VIDEO 3
N/C 7
N/C 8
+12V 4
+12V 5
HORIZ SYNC 2
VERT SYNC 1
GND 6
WHT/ORN
RED
RED
WHT/RED
WHT/BRN
BLK
E71003
E71005
E71004
E71002
E71001
E71006
L71001
140T, 22 AWG
C71001 4700 25V
C71002 4700 25V
C71003 4700 25V
R71005 5K
R71003 22K 1/8W
E71004 20K WIDTH
R71007 22K 1/8W
N/C
N/C
E71006 2K
VR105 250K BRIGHT
R71013 47K
E71020
E71021
E71022
WHT/GRN
WHT/BLK
WHT/GRY
E114
E115
E116
E71011
WHT/ORN
E108
RED
E107
B+
C135 470
VR103 500 DRIVE
E71019
E71009
E71010
E71016
E71014
E71017
BLK
WHT/BRN
WHT/RED
WHT/BLU
WHT/YEL
WHT/VIO
E101 GND
E109 VERT. SYNC
E106 HORIZ. SYNC
E112 INTERLACE
E113
E111
R114 22K
B+
R129 2.7K
R142 2.7K
R134 180
B+
C126 47
R131 27K
R132 10K
C128 .0047
C125 4.7
R165 1K
C116 820pF
R167 2.7K
C116A
C116B 0022
R145 680
C119C
C130 3300pF
C117 1
R124A 33K
C118 .033
IC101
N/C
N/C
R157 120
B+
C138 330
R163 1K
C122
C127 5600pF
R122 120
C104 2.2
R100 2.2
P19008
6050-1050-850
SP65001


G
H
J
K
L
M
VDY
RED
VR65001-P1
VR65001-J1
CONTROL GRID
N/C
CATHODE
ANODE
FOCUS
GND
R205
C204
C200
R201
R200
15K
VR200
2M
FOCUS
R202
470K
C201
.001
YELLOW
(COMPUTRON) 200
SATELLITE PCBD ASSY
R150
Q104a
2N4400
Q104
2N4400
330pf
R112
56
D105
1N400
D104
MR818
D103
MR818
R121
15
V+
C115
1
R133
220
HORZ
RANGE
R143
1.2K
Q107
2N4400
.0033

NOTES (UNLESS OTHERWISE STATED):

(NOTES 1 THROUGH 9 REFLECT MODIFICATIONS TO COMPUTRON CRT, AS REQUIRED, BY IFR SYSTEMS, INC.)

1. R158 IS SELECTED AT TEST (S.A.T.): NOMINAL VALUE IS 15 OHMS, RANGE: 6.8 TO 15 OHMS.

2. REPLACE EXISTING C116c (COMPUTRON CRT MAIN PC BD) WITH 22 GA. BUS WIRE, .5" LONG.

3. REPLACE EXIST C119c (COMPUTRON CRT MAIN PC BD) WITH .01 MICROFARAD CAPACITOR.

4. REPLACE EXISTING W6 (COMPUTRON CRT MAIN PC BD) WITH 143K, 1% RESISTOR.

5. REPLACE EXISTING R103 (COMPUTRON CRT MAIN PC BD) WITH 200K POT.

6. C117 IS S.A.T.; CHANGE AS REQUIRED. NOMINAL VALUE OF COMPUTRON PART IS 47 MICROFARADS. SELECT VALUE IS 1.0 MICROFARADS.

7. CHANGE EXISTING Q102 AND Q103 (COMPUTRON CRT MAIN PC BD) FROM 2N4400 TO 2N2222 TRANSISTORS.

8. REMOVE WAX FROM TOP OF EXISTING L102 (COMPUTRON CRT MAIN PC BD); REPLACE WITH MAGNET AND WASHER, AS NEEDED, WITH HEAT SHRINK TUBING.

9. REMOVE VR101, VR105, VR106, AND VR107 FROM COMPUTRON CRT MAIN PC BD. ADD WIRES TO CONNECT IFR CRT FILTER PC BD ASSEMBLY.

10. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING SERIES:
    - MECHANICAL ASSEMBLY: 65000
    - COMPUTRON SATELLITE PC BD ASSEMBLY: 200
    - COMPUTRON CRT MAIN PC BD ASSEMBLY: 100 & 300
    - CRT FILTER PC BD ASSEMBLY: 71000.

11. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE.

12. ALL RESISTANCE IS EXPRESSED IN OHMS.

13. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

Figure 5-29 CRT Display Assembly (Sheet 2 of 2) (0000-5314-900)

APPENDICES

APPENDIX A - A-7550 PERFORMANCE SPECIFICATIONS

A-1 FREQUENCY

Frequency Range:	100 kHz to 1 GHz in 100 Hz steps.
Frequency Display Span:	1 kHz/DIV to 100 MHz/DIV in 1-2-5 sequence. In "0" the analyzer is a fixed-tuned receiver.
Frequency Display Linearity:	Frequency error between any two points on the display is less than ±5% of the indicated frequency separation.
Digital Frequency Readout:	Indicates center frequency at the frequency display span.
Accuracy:	±3% of frequency display span plus 0.0025% of frequency selected.
Resolution:	
Bandwidth Ranges: (at 3 dB)	300 Hz, 3 kHz, 30 kHz, 300 kHz and 3 MHz.
Accuracy:	±30% of bandwidth selected.
Filter Shape Factor:	60 dB/3 dB ratio <5:1, 300 Hz <12:1.
Video Filter:	Post-detection filter used to average displayed noise. 30 kHz and 300 Hz bandwidths selectable.
Residual FM (typical):	<30 Hz RMS peak at scan/DIV settings below 200 kHz/DIV.
Noise Sidebands (typical):	>65 dB below peak cw signal at 5X resolution bandwidth setting from cw signal. (With 300 Hz video filter).

A-2 AMPLITUDE

Measurement Range:	-120 dBm to +30 dBm.
Spurious:	For input signals ≥3 MHz and ≤30 dBm: - from 10 kHz to 100 kHz @ -75 dBm (max) - from 100 kHz to 1 MHz @ -85 dBm (max) - from 1 MHz to 2 MHz @ -115 dBm (max)

Displayed Dynamic Range:	70 dB in 10 dB/DIV log scale. 16 dB in 2 dB/DIV log scale. 8 divisions with linear amplitude scale.
Amplitude Scale Linearity:	10 dB/DIV log ±0.15 dB/dB, but not more than ±2.5 dB over 70 dB dynamic range. 2 dB/DIV log ±0.4 dB/2 dB, but not more than ±1.5 dB over 14 dB dynamic range. Linear demodulation linearity ±2% of full scale.
Frequency Response:	±2 dB over 10 MHz to 1000 MHz range from the center of amplitude excursions.
Amplitude Variation between Bandwidth:	±1 dB; except ±2 dB for 300 Hz.

A-3 INPUT

Impedance:	50Ω nominal, 75Ω optional.
Attenuator:	60 dB range in 10 dB steps.
Accuracy:	±0.5 dB/10 dB steps.
Maximum Input Levels:	4 volts DC or +30 dBm with maximum input attenuation. +20 dBm for all other conditions.

A-4 OUTPUT

Calibrator:	
Frequency:	100 MHz ±.0025%, crystal controlled.
Amplitude:	-30 dBm ±1 dB.
Sweep Out:	0 to 5V ramp (nominal).
Video Out:	0 to 800 mV riding on DC level.

A-5 GENERAL CHARACTERISTICS

Temperature Range:	0° to 50° C.
Power Requirements:	
Line:	106 to 266 VAC, 50 to 400 Hz at 55 watts typical (no options).
External D.C.:	12 to 30 VDC nominal. 4 Amps at 12V typical (no options). 2 Amps at 28V typical (no options).

A-6 TRACKING GENERATOR (OPTIONAL)

Frequency Range:	100 kHz to 1 GHz
Output Level:	0 dBm to -75 dBm in 1 dB steps.
Flatness:	±2 dB
Residual FM:	<100 Hz RMS peak
Output Impedance:	50Ω nominal (75Ω optional)
Spurious:	Harmonics: 20 dBc or lower. Non-harmonics: 40 dBc or lower.

A-7 RECEIVER (OPTIONAL)

Range: 100 kHz to 1 GHz

Center Frequency Resolution: 100 Hz

Sensitivity: 2 µV typical

Selectivity: (at 3 dB)

Mode	Receiver Bandwidth
FM 2	200 kHz
FM 1	15 kHz
SSB	6 kHz
AM 1	6 kHz
AM 2	15 kHz

Adjacent Channel Rejection: (at 3 dB)

Receiver Bandwidth	40 dB DOWN AT
200 kHz	±300 kHz
15 kHz	±27 kHz
6 kHz	±12 kHz

A-8 QUASI-PEAK DETECTOR (OPTIONAL)

Frequency Range	Bandwidth at 6 dB	Charge Constant	Time (ms)	Discharge Constant	Time (ms)
<150 kHz	200 Hz	TC1	45 ms	TC1	500
150 kHz to 30 MHz	9 kHz	TC2	1 ms	TC2	160
>30 MHz	120 kHz	TC3	1 ms	TC3	550

A-9 +20 dB AMP (ACCESSORY)

Frequency Range: 10 MHz to 1 GHz

Gain: +20 dB (nominal)

APPENDIX B - TEST EQUIPMENT REQUIREMENTS

B-1 GENERAL

This appendix contains a list of test equipment suitable for performing the maintenance procedures in this manual. Any other equipment meeting the specifications listed in this appendix may be substituted for the recommended models. Note that the equipment listed in this appendix may exceed the minimum specification requirements for some of these procedures.

B-2 RECOMMENDED TEST EQUIPMENT

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Oscilloscope	Tektronix 465B	DC to 100 MHz 5 mV/div vertical trace 2 nS/div sweep rate Dual Trace
Spectrum Analyzer (for Quasi-peak)	Tektronix 7613 Frame Tektronix 7L13/U Spectrum Analyzer (IFR A-7550)	Variable Persistence Storage Oscilloscope Frequency Range: 1 kHz to 2.5 GHz Resolution Bandwidth: 30 Hz to 3 MHz (Frequency Range: 10 kHz to 1000 MHz)
Digital Multimeter	Fluke Model 8010A	3½ digit, ±0.1% basic DC accuracy
RF Power Meter with Power Detector	Boonton RF Microwattmeter Model 42 BD	Frequency Range: 200 kHz to 18 GHz Power Range: 1.0 nW to 10 mW Accuracy: ±0.25% fs ±0.15 dB ±10 nW
	Boonton Power Sensor Model 41-4A	Frequency Range: 200 kHz to 7 GHz Power Range: 1 nW to 10 mW Accuracy: ±0.3 dB >10 nW
Power Supply	B&K 1601	Regulation: .1% or 1 mV Ripple: 5 mV Voltage Range: 0-50 VDC @ 0-2 A

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Function Generator	Wavetek 182A	Frequency Range: .004 Hz to 4 MHz Functions: Sine, Triangle & Square High Level Output: 20 Vp-p (10 Vp-p into 50Ω)
RF Signal Generator	Hewlett Packard 8640B, Fluke 6060A or equivalent	Frequency Range: 1 to 1000 MHz Resolution: 0.1 to 100 Hz Accuracy: 2×10^{-6} RF Output: +20 to -130 dBm
Modulation Meter	Boonton Model 8200	Frequency Range: 10 MHz to 2.0 GHz
		Accuracy: FM: ±2% of reading from 30 Hz to 100 kHz
		Accuracy: AM: ±2% of reading from 10 Hz to 90% AM and 5% of reading below 10% and above 90%; from 30 Hz to 100 kHz
		Resolution: 0.1% of full scale for FM and AM
Electronic Counter	Hewlett-Packard Model 5315A	Frequency Range: 0 to 100 MHz Sensitivity: 10 mV RMS
Wattmeter	Sierra 174A-1	Frequency Range: 25 to 1000 MHz
		VSWR: 25-512 MHz: 1.10 max 512-1000 MHz: 1.20 max Accuracy Indent Power: 25-512 MHz: ±5% of full scale 512-1000 MHz: ±7% of full scale

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
1 dB Step Attenuator	Weinchel Model 9621	Frequency: 20-80 MHz, 1.0-1.2 GHz Impedance: 50Ω Accuracy: 1 dB ±.14 dB
10 dB Step Attenuator	Weinchel Model 9682-1	Attenuation Range: 0-127 dB Accuracy: ±.25 dB or 1.25% from .5 MHz to 1 GHz whichever is greater
Power Supply	LAMBDA LK-351-FM	Regulation: .015% or 1 mV Ripple: 500 µV Voltage Range: 0-36 VDC @ 25.0 A
Distortion Analyzer	Sound Technology Model 1700B	Frequency Range: 10 Hz to 110 kHz Accuracy: .002% distortion AC Voltage Accuracy: 2%
Frequency Counter	Fluke 1910A or equivalent	Range: 1 to 1000 Hz Resolution: .1 Hz
Pulse Generator	WaveTech 145 or equivalent	Range: 1 to 1000 PRF Pulse Width: Variable, .1 µS to 100 µS
Impulse Generator	Electrometrics C16-25 or equivalent	Frequency Spectrum Flatness: Within 1 dB, 0 to 1000 MHz
Solid State Switcher	Watkins-Johnson SI or equivalent	ON/OFF Ratio: 0 to 80 dB

APPENDIX C- PREVENTIVE MAINTENANCE RECOMMENDATIONS

Preventive maintenance on A-7550 test sets primarily consists of cleaning and visual inspection of components. External cleaning of the test set is recommended as often as necessary. Internal cleaning should be performed on a more limited basis, preferably when the set is in a disassembled state for routine calibration, troubleshooting or repair. Test set disassembly for the sole purpose of internal cleaning is not recommended.

C-1 EXTERNAL CLEANING

1. Clean front panel and case with a soft lint-free cloth moistened with rubbing alcohol.

2. To remove tar or oil from outside case, safety solvent may be used.

   CAUTION: DO NOT ALLOW SAFETY SOLVENT TO CONTACT FRONT PANEL CONTROL AREA. SOLVENT CAN CAUSE DAMAGE TO FRONT PANEL CONTROLS, MARKINGS ETC.

C-2 INTERNAL CLEANING AND INSPECTION

NOTE: The following procedures require removing the case from test set.

CAUTION: DELIBERATELY MOVING (HOWEVER SLIGHT) DISCRETE COMPONENTS ON CIRCUIT BOARDS, ETC. SHOULD BE AVOIDED.

DO NOT OPEN INTERNAL MODULES FOR SOLE PURPOSE OF CLEANING.

1. Remove dust with hand-controlled dry air jet of 15 psi (1.054 kg/cm^2) and wipe internal chassis parts and frame with soft lint-free cloth moistened with alcohol.

1. (Continued)

WARNING! DO NOT USE COMPRESSED AIR IN EXCESS OF 15 PSI. USE EXTREME CARE WHEN USING COMPRESSED AIR IN THE VICINITY OF CRT, IN ORDER TO MINIMIZE POSSIBILITY OF CRT IMPLOSION. OBSERVE FOLLOWING PRECAUTIONS:

a. MANUALLY REMOVE ANY LARGE DIRT/DUST PARTICLES CRT, AS OPPOSED TO USING COMPRESSED AIR.

b. DO NOT USE COMPRESSED AIR IN A DIRTY, CLUTTERED ENVIRONMENT. REMOVE ANY DEBRIS OR SMALL OBJECTS IN THE IMMEDIATE WORK AREA THAT MAY BECOME AIRBORNE DUE TO PRESSURIZED AIRFLOW.

c. IF POSSIBLE, USE AN AIR HOSE NOZZLE EQUIPPED WITH A SPRING LOADED ON/OFF VALVE, AS OPPOSED TO ONE THAT REMAINS OPEN OR CLOSED CONTINUOUSLY.

d. MAKE SURE COMPRESSED AIR HOSE IS FILTERED, TO PREVENT POSSIBLE OIL OR WATER DROPLETS FROM STRIKING CRT AT HIGH SPEEDS.

2. Inspect CHASSIS for:

a. Tightness of subassemblies and chassis mounted connectors.

b. Corrosion or damage to metal surfaces.

3. Inspect CAPACITORS for:

a. Loose mounting, deformities or obvious physical damage.

b. Leakage or corrosion around leads.

4. Inspect CONNECTORS for:

a. Loose or broken parts, cracked insulation and bad contacts. (DO NOT disassemble connectors needlessly within test set.)

5. Inspect POTENTIOMETER CONTROLS for:

a. Free rotation. If rotation feels rough, check control with an ohmmeter.

6. Inspect readily accessible PRINTED CIRCUIT BOARDS for:

a. Corrosion or damage to connectors.

6. (Continued)

   b. Damage to all mounted components including crystals and I.C.'s.

   c. Accumulation of dirt, dust or other foreign material.

7. Inspect RESISTORS for:

   a. Cracked, broken, charred or blistered bodies.

   b. Loose or corroded solder connections.

8. Inspect SEMICONDUCTORS for:

   a. Cracked, broken, charred or discolored bodies.

   b. Seals around leads being in place and in good condition.

9. Inspect TOGGLE SWITCHES for:

   a. Loose levers or terminals and switch body contact to frame.

   b. Bent or loose line switch contacts.

10. Inspect TRANSFORMER for:

    a. Signs of excessive heating.

    b. Broken or charred insulation and loose mounting hardware.

11. Inspect WIRING for:

    a. Broken or loose ends and connections.

    b. Proper dress relative to other chassis parts.

    NOTE: All laced wiring should be tight with ends securely tied.

APPENDIX D - SPECIAL ACCESSORY TEST EQUIPMENT

D-1 GENERAL

This appendix contains recommendations for constructing special equipment necessary for performing certain test procedures in this manual.

D-2 BATTERY LOAD SIMULATOR

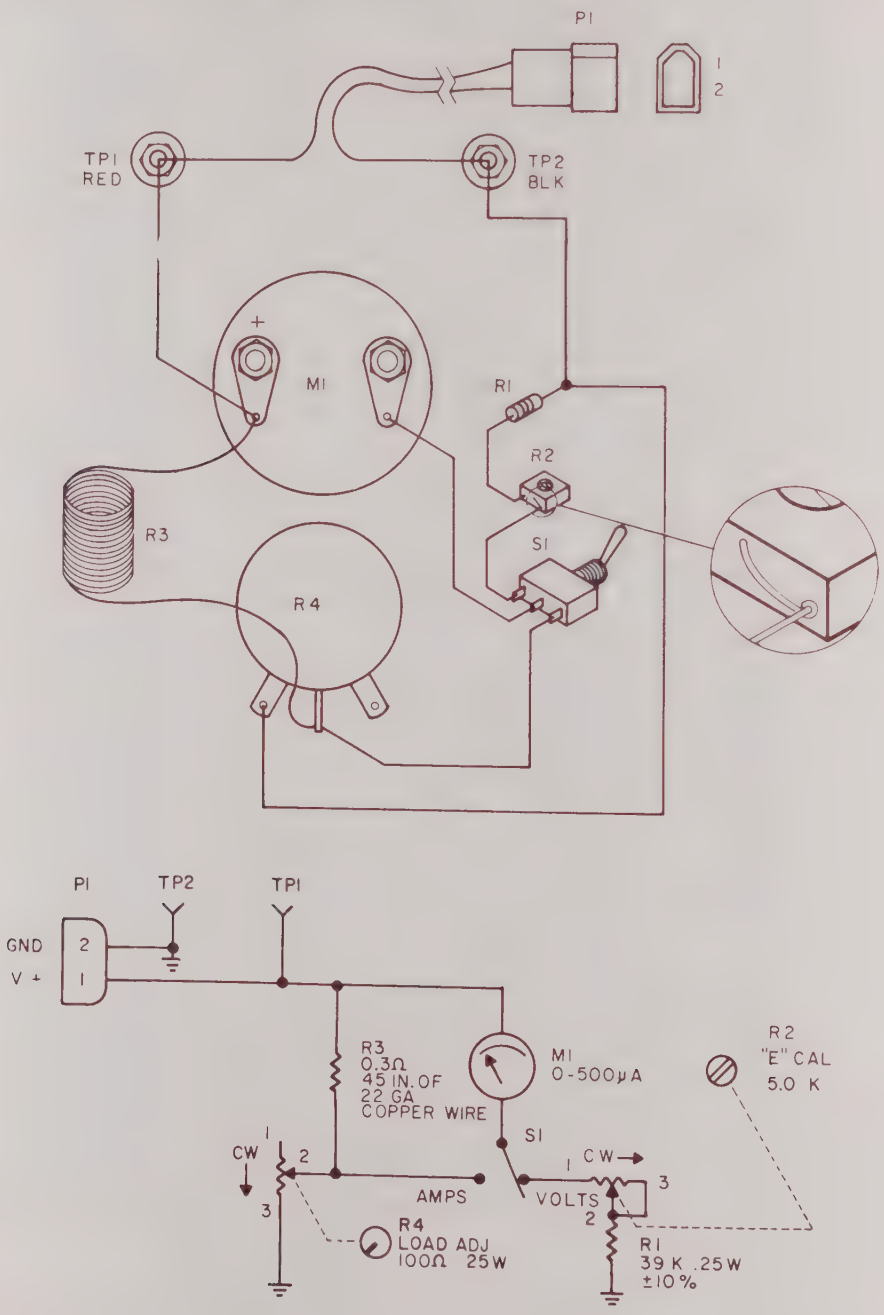
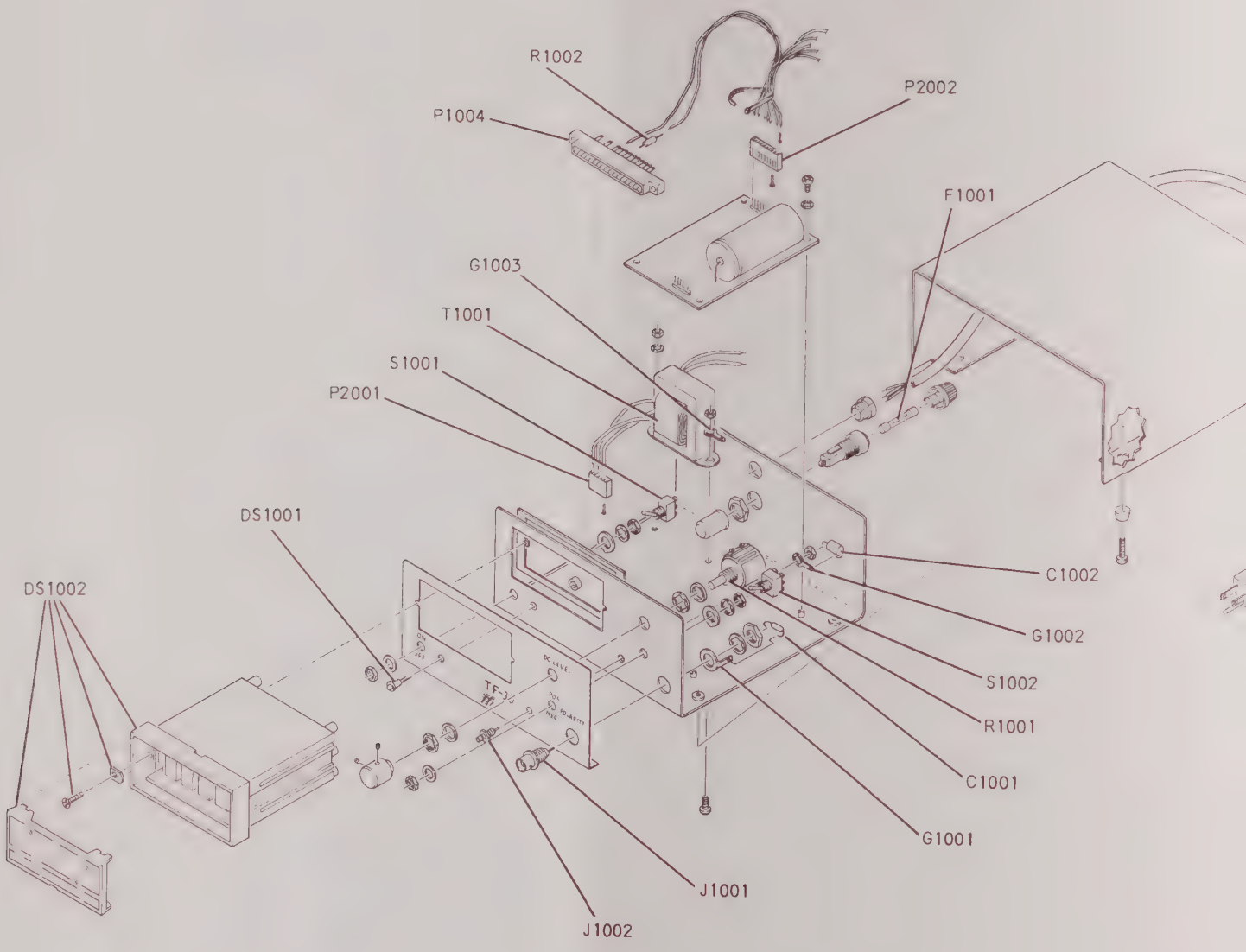


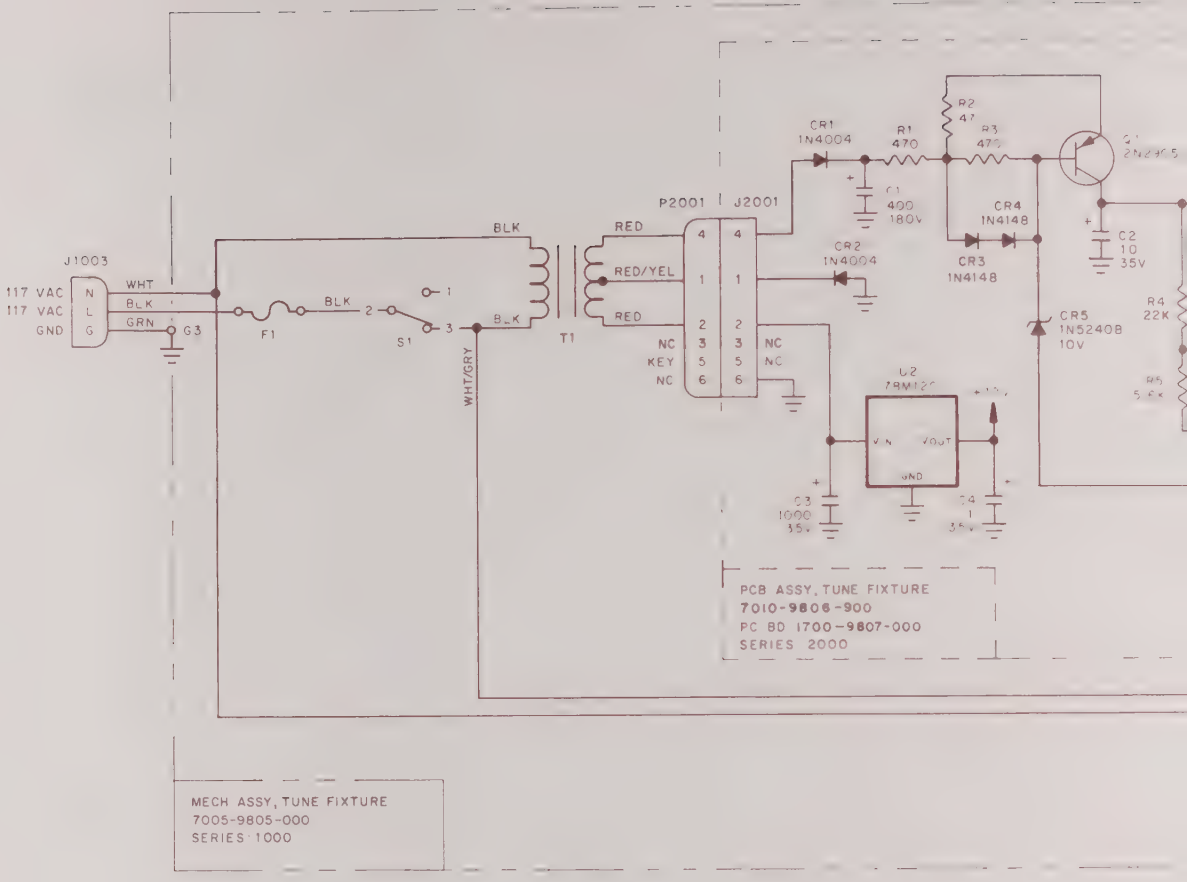
Figure D-1 Circuit Schematic and Diagram of Battery Load Simulator

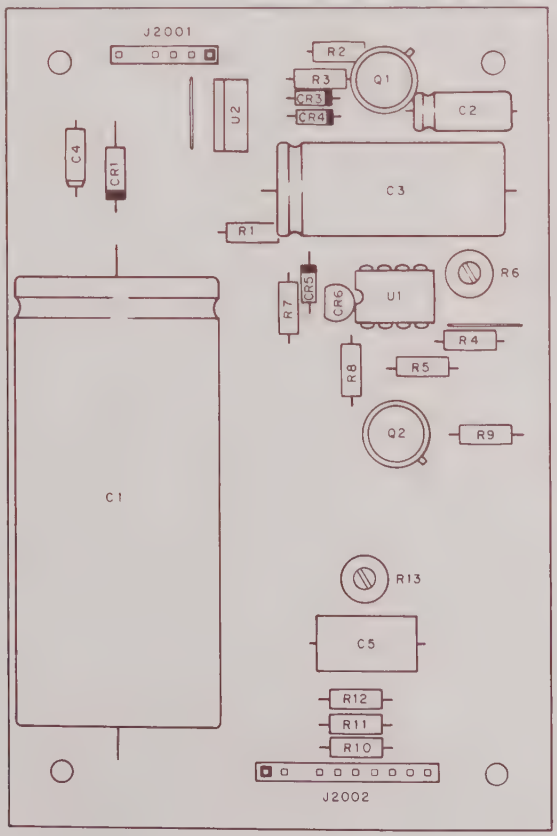
D-3 TF-30 TUNE FIXTURE

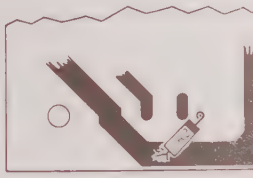


REF DES	DESCRIPTION	IFR PART NO.	QTY
	TUNE FIXTURE ASSEMBLY		
J1001	CONNECTOR, BNC	2113-0000-020	1
J1002	CONNECTOR, SMB	2123-0000-038	1
J1003	CABLE ASSY, AC POWER	6041-0000-001	1
P1004	CONNECTOR, CARD EDGE	2122-0000-018	1
P2001	CONNECTOR, WAFER	2115-0000-006	1
P2002	CONNECTOR, WAFER	2115-0000-013	1
C1001	CAPACITOR .10 µF, 50 V	1521-0000-008	1
C1002	CAPACITOR .15 µF, 50 V	1646-1540-098	1
DS1001	LED GRN	4950-0300-200	1
DS1002	DISPLAY, DIGITAL VOLTMETER	4600-0000-006	1
F1001	FUSE, FAST BLO 1 A, 250 V		1
G1001	LUG, GND 3/8"	2850-0000-025	1
G1002	LUG, GND 3/8"	2850-0000-041	1
G1003	LUG, GND #4 INT TOOTH	2850-0000-014	1
R1001	RESISTOR, VAR 10 K	4770-8810-300	1
R1002	RESISTOR 5%, 1/4 W, 1 K	4702-0102-003	1
S1001	SWITCH, TOGGLE	5114-0000-001	1
S1002	SWITCH, TOGGLE	5114-0000-004	1
T1001	TRANSFORMER	5604-0000-002	1
	TUNE FIXTURE, PC BD	7010-9806-900	1
J2001	CONNECTOR, WAFER	2115-1001-006	1
J2002	CONNECTOR, WAFER	2115-0000-016	1
C2001	CAPACITOR 400 µF, 180 V	1580-4010-800	1
C2002	CAPACITOR 10 µF, 35 V	1580-1000-350	1
C2003	CAPACITOR 1000 µF, 35 V	1580-1020-358	1
C2004	CAPACITOR 1 µF, 35 V	1507-0105-118	1
C2005	CAPACITOR 1 µF, 50 V	1502-0105-007	1
CR2001	DIODE, RECT IN4004	4815-0000-002	1
CR2002	DIODE, RECT IN4004	4815-0000-002	1
CR2003	DIODE, SIGNAL IN4148	4815-0000-003	1
CR2004	DIODE, SIGNAL IN4148	4815-0000-003	1
CR2005	DIODE, ZENER 10 V	4818-0000-001	1
CR2006	DIODE, ZENER 6.9 V	4818-0000-015	1
Q2001	TRANSISTOR 2N2905	4801-0000-004	1
Q2002	TRANSISTOR 2M2405	4801-0000-002	1
R2001	RESISTOR 5%, 1/4 W, 470 OHM	4702-0471-003	1
R2002	RESISTOR 5%, 1/4 W, 47 OHM	4702-0470-003	1
R2003	RESISTOR 5%, 1/4 W, 470 OHM	4702-0471-003	1
R2004	RESISTOR 5%, 1/4 W, 22 K	4702-0223-003	1
R2005	RESISTOR 5%, 1/4 W, 5.6 K	4702-0562-003	1
R2006	RESISTOR, VAR 2 K	4752-0202-002	1
R2007	RESISTOR 5%, 1/4 W, 1 K	4702-0102-003	1
R2008	RESISTOR 5%, 1/4 W, 330 OHM	4702-0331-003	1
R2009	RESISTOR 5%, 1/4 W, 3.3 K	4702-0332-003	1
R2010	RESISTOR 5%, 1/4 W, 100 OHM	4702-0101-003	1
R2011	RESISTOR 1%, 1/4 W, 100.00 OHM	4706-1003-001	1
R2012	RESISTOR 1%, 1/4 W, 909.00 OHM	4706-9090-001	1
R2013	RESISTOR, VAR 200 OHM	4752-0201-002	1
U2001	IC, DUAL J-FET OP AMP LF412	3135-0000-054	1
U2002	IC, REGULATOR 78M12C	5750-0000-010	1
	WIRE, BUS 22 GA	1050-0000-073	

Figure D-2 TF-30 Tune Fixture Assembly (Sheet 1 of 2)


J1003
117 VAC
117 VAC
GND
N
L
G
WHT
BLK
GRN
G3
F1
BLK
S1
1
2
3
BLK
T1
BLK
WHT/GRY
RED
RED/YEL
RED
NC
KEY
NC
P2001
J2001
CR1
1N4004
R1
470
R2
47
R3
47
C1
400
180V
CR2
1N4004
CR4
1N4148
CR3
1N4148
C2
10
35V
CR5
1N5240B
10V
R4
22K
R5
5.6K
U2
7805T
VIN
VOUT
GND
C3
1000
35V
C4
1
35V
PCB ASSY, TUNE FIXTURE
7010-9806-900
PC BD 1700-9807-000
SERIES 2000
MECH ASSY, TUNE FIXTURE
7005-9805-000
SERIES 1000


J2001
R2
R3
CR3
CR4
Q1
C2
U2
C4
CR1
C3
R1
R6
CR5
CR6
U1
R7
R4
R8
R5
Q2
R9
C1
R13
C5
R12
R11
R10
J2002



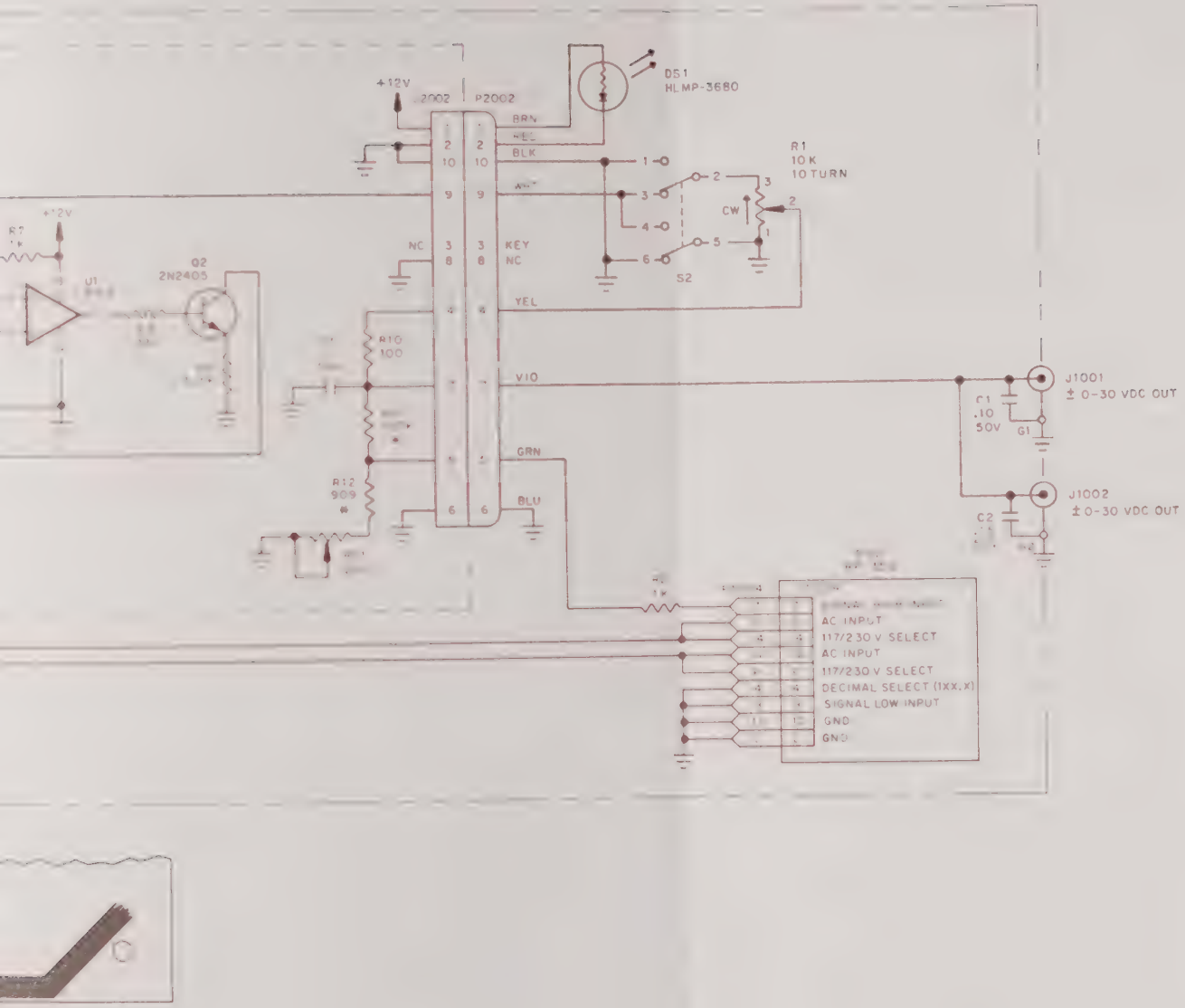


Figure D-2 TF-30 Tune Fixture Assembly (Sheet 2 of 2)

D-4 REMOVABLE 20 dB TEST POINT

FABRICATE 20 dB TEST POINT AS FOLLOWS:

1. SOLDER RESISTOR TO FIRST SMB CONNECTOR.

2. SOLDER RF SHIELD TO FIRST SMB CONNECTOR.

3. USING ACCESS HOLE, SOLDER RESISTOR TO SECOND SMB CONNECTOR.

4. SOLDER SECOND SMB CONNECTOR TO RF SHIELD.

5. SOLDER BUS WIRE TO FIRST SMB CONNECTOR.

6. TRIM BUS WIRE TO LENGTH REQUIRED TO CONTACT TEST POINT BEING ACCESSED.

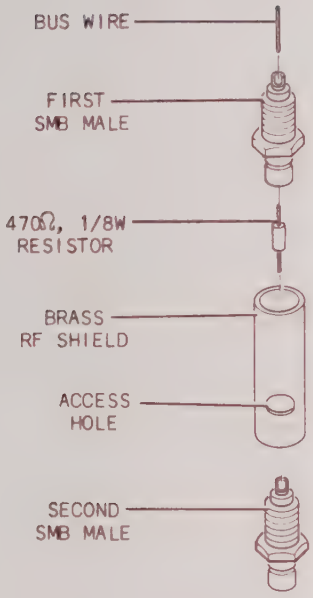


Figure D-3 20 dB Test Point

D-5 QUASI-PEAK INLINE TEST FILTERS

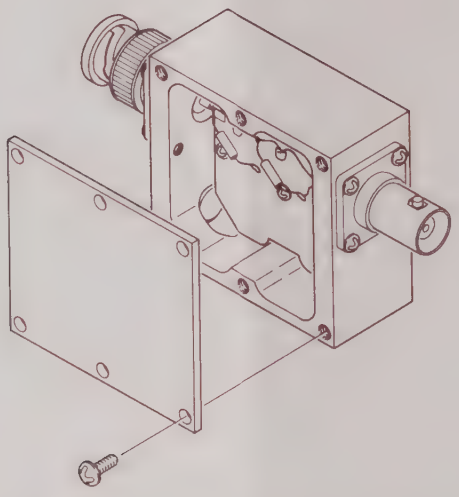


Figure D-4 Filter Enclosure

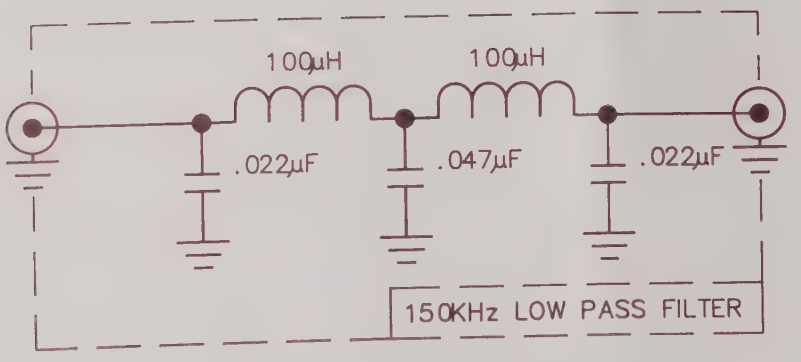


Figure D-5 150 kHz Low-pass Filter

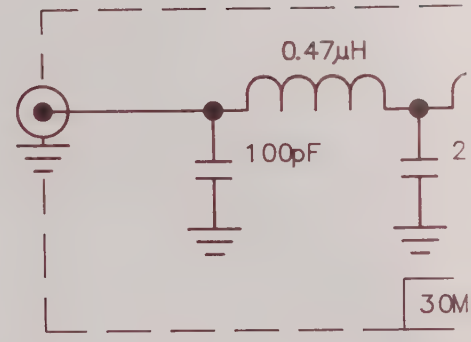
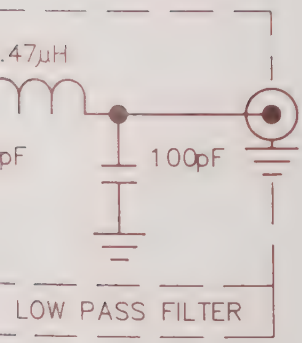


Figure D-6 30 MHz L



-pass Filter

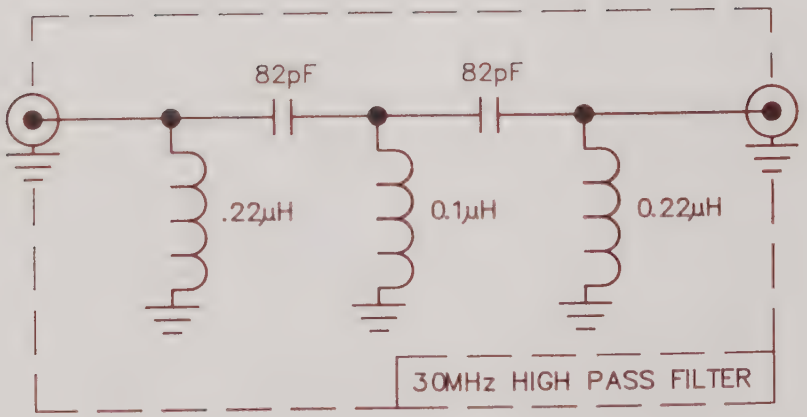


Figure D-7 30 MHz High-pass Filter

APPENDIX E- ABBREVIATIONS AND REFERENCE DESIGNATORS

E-1 TEXT ABBREVIATIONS

A	- Ampere (Amp)
AC	- Alternating Current
ADC (A/D)	- Analog-to-Digital Converter
AGC	- Automatc Gain Control
AM	- Amplitude
AMP	- Amplifier, Amplitude, Ampere
A/N	- Alphanumeric
Assy	- Assembly
ATTEN	- Attenuator, Attenuation
AUTO CAL	- Automatic Calibration
BATT	- Battery
BCUR	- Buffered Cursor
Bd	- Board
BW	- Bandwidth
CAL	- Calibration
CAL OUT	- Calibration Output
cm	- Centimeter
COAX	- Coaxial Cable
COMP	- Compare
CPU	- Central Processing Unit
CRT	- Cathode Ray Tube
CTC	- Counter-Timer Circuit
CW	- Continuous Wave
DAC (D/A)	- Digital-to-Analog Converter
dB	- Decibels
dBc	- Decibels relative to a carrier
dBm	- Decibels relative to milliamps
dBmV	- Decibels relative to millivolts
dBµV	- Decibels relative to microvolts
DC	- Direct Current
DIV (Div)	- Division(s)
ECL	- Emitter Coupler Logic
e.g.	- for example
EMC	- Electro-Magnetic compatibility
EPROM	- Eraseable Programmable Read-only Memory
EXT AMP	- External Amplifier
F	- Farad
FET	- Field-effect Transistor
FIFO	- First-in First-out
FM	- Frequency Modulation
freq (f)	- Frequency

GEN	- Generator
GHz	- GigaHertz
GPIB	- General Purpose Interface Bus (IEEE 488-1978)
Hz	- Hertz
IC	- Integrated Circuit
i.e.	- that is
IEEE	- Institute of Electrical and Electronic Engineers
IEEE 488-1978	- An IEEE communications standard (GPIB)
IF	- Intermediate Frequency
IORQ	- Input-output request
K	- kilo - 1,000
kg	- kilogram
kHz	- kiloHertz
LIN	- Linear
LO	- Local Oscillator
LOG AMP	- Logarithmic Amplifier
LPF	- Low-pass Filter
LSB	- Least Significant Bit
MHz	- MegaHertz
MREQ	- Memory request
MSB	- Most Significant Bit
ns (nsec)	- nanosecond
nW	- nanowatt
PC	- Printed Circuit
pF	- picoFarad
PkHold	- peak hold (mode)
p-p	- peak-to-peak
prf	- pulse repetition frequency
PROM	- Programmable read-only memory
psi	- pounds per square inch
PWR	- power
Q	- Logical output level of a flip-flop
RAM	- Random Access Memory
RCVR	- Receiver
REF	- Reference
REF CAL OUT	- Reference Calibration Output
REF FREQ	- Reference Frequency
RES B/W	- Resolution Bandwidth
RF	- Radio Frequency
RFSH	- Refresh
RMS	- Root mean square
ROM	- Read-only Memory
RS-232	- A data communications standard

S/N	- Serial Number
SSB	- Single Side Band
SYN/SYNTH	- Synthesizer
TC	- Time Constant
TSR	- Time Sharing Receiver
TTL	- Transistor-to-Transistor Logic
V	- Voltage, Volts
VAC	- Volts, Alternating Current
VCO	- Voltage Controlled Oscillator
VDC	- Volts, Direct Current
VERT	- Vertical
V p-p	- Voltage peak-to-peak
VRMS	- Volts, Root Mean Square
*VRS	- Vertical Raster Scan
VSWR	- Voltage Standing-wave ratio
µV	- Microvolt

E-2 REFERENCE DESIGNATORS

AT	Attenuator, Pad, Isolator
B	Motor, Fan
BR	Bridge Rectifier
BT	Battery
C	Capacitor
CP	Coupler
CR	Diode, Varactor
CX	Coax Cable
DET	Detector
DS	Lamp, Alphanumeric Display, LED, etc.
E	Connection, Inseparable, Elect.
F	Fuse
FL	Filter, Feedthrough Cap, Coupling Transformer
G	Oscillator
HY	Circulator
J	Jack (fixed half of connector pair)
JTB	Jumper Terminal Block
K	Relay
L	Inductor, Ferrite Bead
M	Meter
MXR	Mixer
P	Plug (Moveable half of connector pair)
PC	Printed Circuit Board
Q	Transistor
R	Resistor
RN	Resistor Network
RT	Thermistor
S	Switch
SP	Speaker
T	Transformer

TP	Test Point
U	Opto-Isolator, I.C., Voltage Regulator, Incapsulated Circuit (i.e., Circuit Combiner)
X	Socket
Y	Crystal
YFL	Crystal Filter
Z	Tune Pole, Tuneable Bandpass Filter

*IFR SYSTEMS, INC. TRADEMARK

APPENDIX F - dBm TO MICROVOLT CONVERSION CHART

dBm	µV	dBm	µV	dBm	µV
0	223,607	-47	1,000	-94	4.46
-1	199,290	-48	890	-95	3.98
-2	177,617	-49	793	-96	3.54
-3	158,302	-50	707	-97	3.16
-4	141,086	-51	630	-98	2.82
-5	125,743	-52	562	-99	2.51
-6	112,069	-53	501	-100	2.24
-7	99,882	-54	446	-101	1.99
-8	89,020	-55	398	-102	1.78
-9	79,339	-56	354	-103	1.58
-10	70,711	-57	316	-104	1.41
-11	63,021	-58	282	-105	1.26
-12	56,168	-59	251	-106	1.12
-13	50,059	-60	224	-107	1.00
-14	44,615	-61	199	-108	0.890
-15	39,764	-62	178	-109	0.793
-16	35,439	-63	158	-110	0.707
-17	31,585	-64	141	-111	0.630
-18	28,150	-65	126	-112	0.562
-19	25,089	-66	112	-113	0.501
-20	22,361	-67	100	-114	0.446
-21	19,929	-68	89.0	-115	0.398
-22	17,762	-69	79.3	-116	0.354
-23	15,830	-70	70.7	-117	0.316
-24	14,109	-71	63.0	-118	0.282
-25	12,574	-72	56.2	-119	0.251
-26	11,207	-73	50.1	-120	0.224
-27	9,988	-74	44.6	-121	0.199
-28	8,902	-75	39.8	-122	0.178
-29	7,934	-76	35.4	-123	0.158
-30	7,071	-77	31.6	-124	0.141
-31	6,302	-78	28.2	-125	0.126
-32	5,617	-79	25.1	-126	0.112
-33	5,006	-80	22.4	-127	0.100
-34	4,462	-81	19.9	-128	0.0890
-35	3,976	-82	17.8	-129	0.0794
-36	3,544	-83	15.8	-130	0.0707
-37	3,159	-84	14.1	-131	0.0630
-38	2,815	-85	12.6	-132	0.0562
-39	2,509	-86	11.2	-133	0.0501
-40	2,236	-87	10.0	-134	0.0446
-41	1,993	-88	8.90	-135	0.0398
-42	1,776	-89	7.93	-136	0.0354
-43	1,583	-90	7.07	-137	0.0316
-44	1,411	-91	6.30	-138	0.0282
-45	1,257	-92	5.62	-139	0.0251
-46	1,121	-93	5.01	-140	0.0224

APPENDIX G - A-7550 SPECTRUM ANALYZER ACCESSORY ITEMS

G-1 GENERAL

Items shown in this Appendix can be purchased to facilitate some of the functions of the A-7550 Spectrum Analyzer, such as changing the power requirements or maintaining the unit. Other items serve a particular need of some users, such as the Camera Mount, which provides an environment for photographing waveforms, or the heavy duty Carrying Case, which can be used to transport the A-7550 Spectrum Analyzer to remote regions for operation. One accessory item, the +20 dB External Amplifier, is included in Section 5 of this manual, as its function is closely related to the Tracking Generator option.

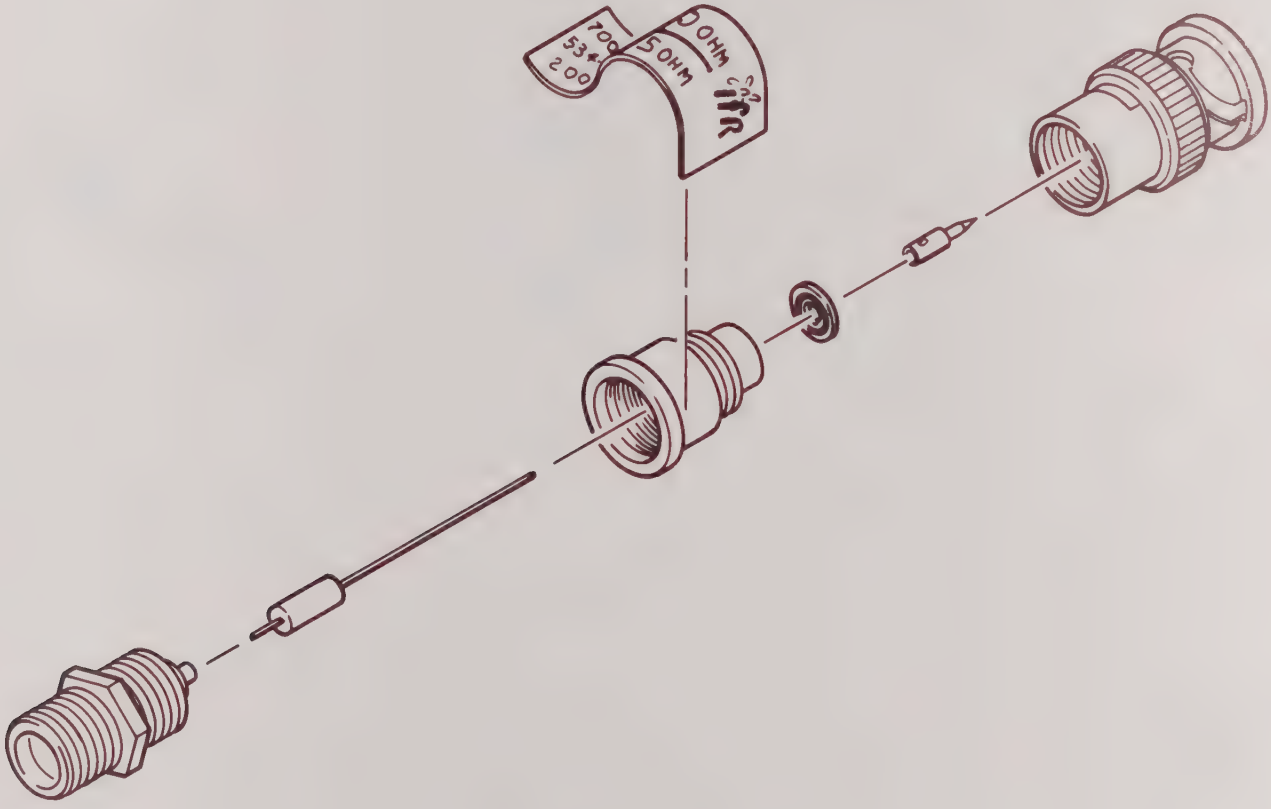


Figure G-1 75 Ohm Adapter (BNC-to-BNC) (AC1100)

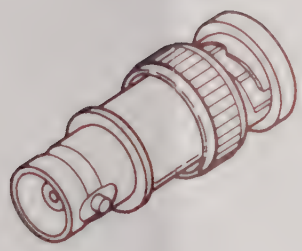
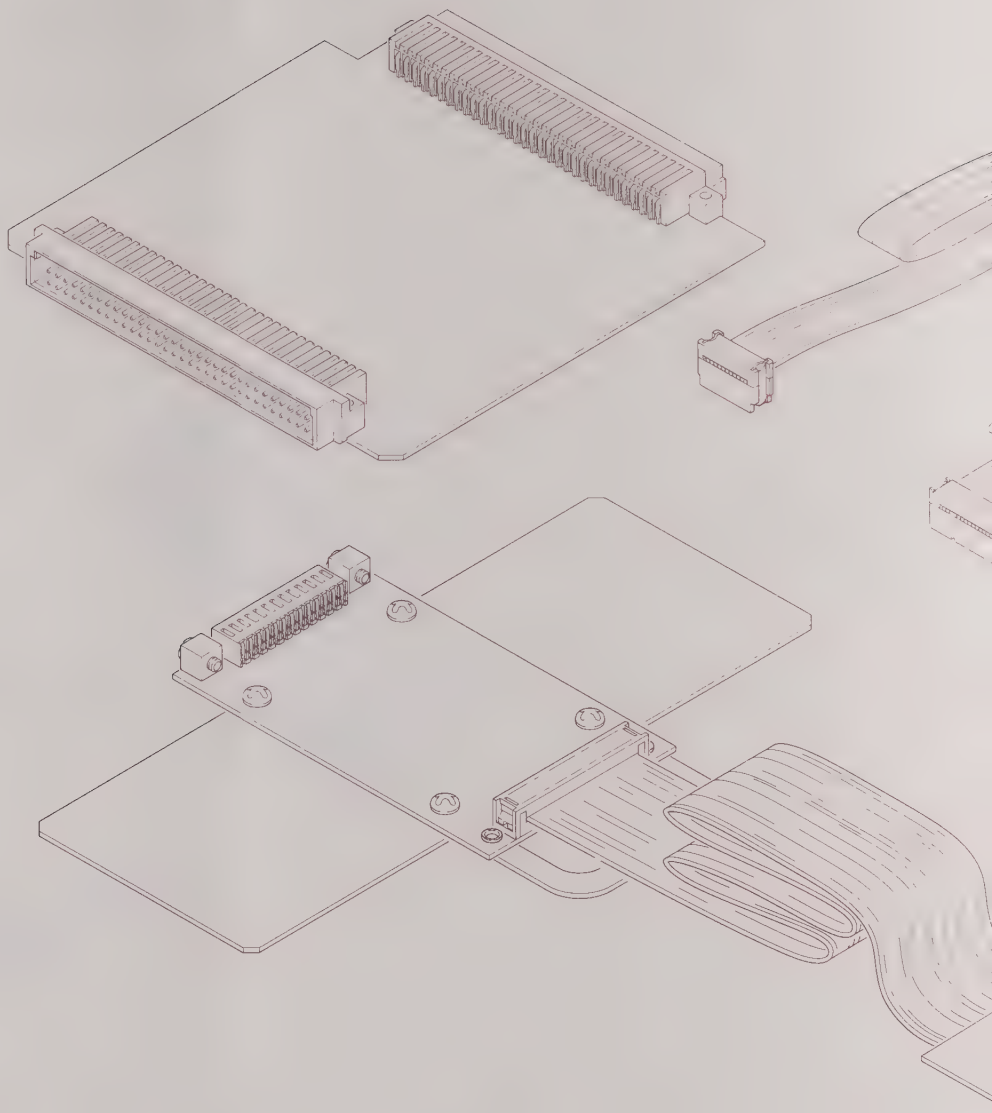


Figure G-2 75 Ohm Adapter (BNC-to-Female) (AC4200)



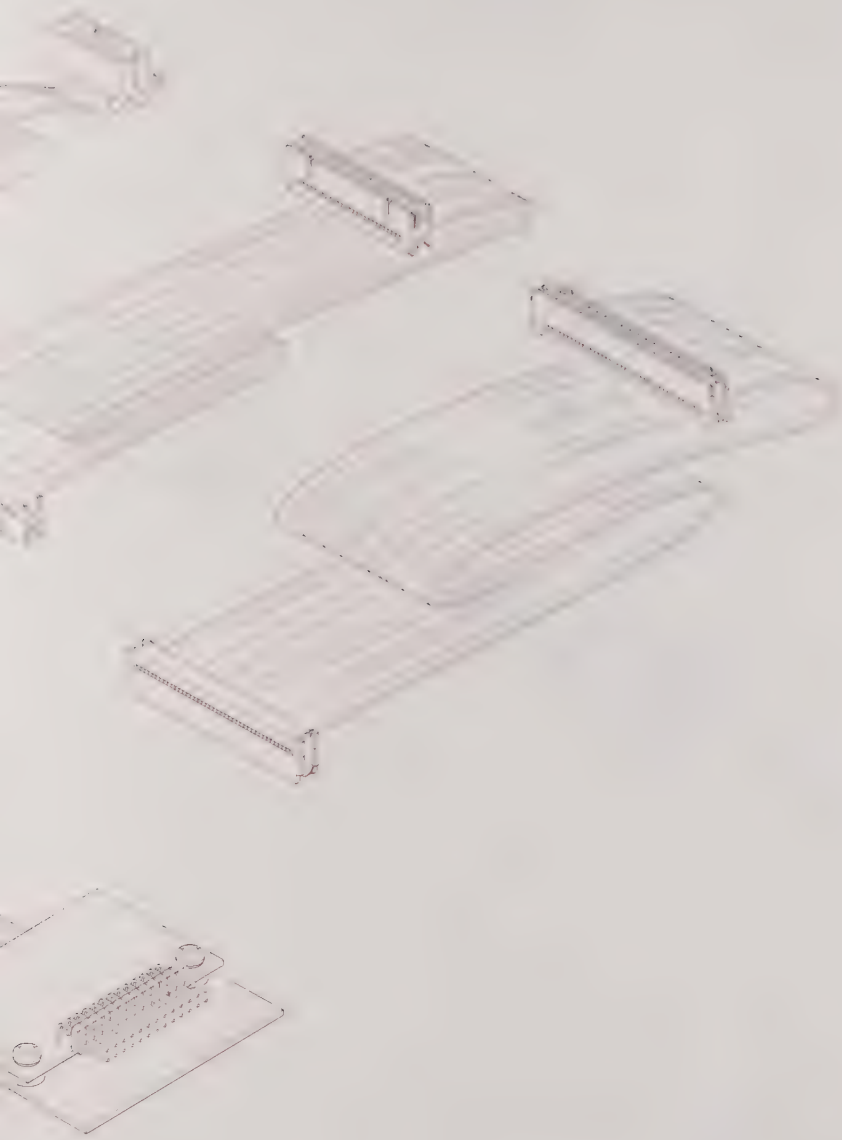


Figure G-3 Maintenance Kit
(AC0400)

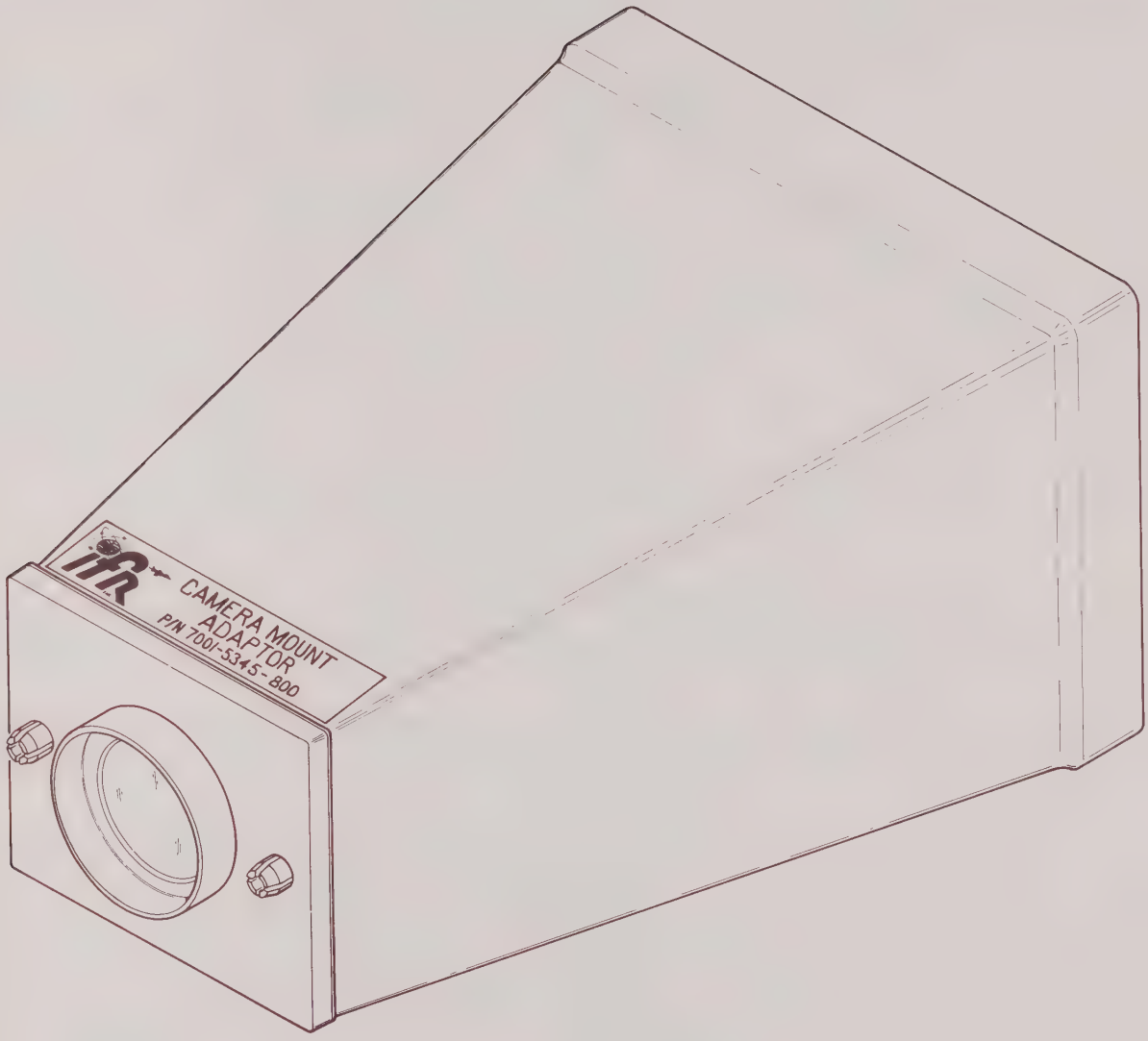


Figure G-4 Camera Mount
(AC5800)

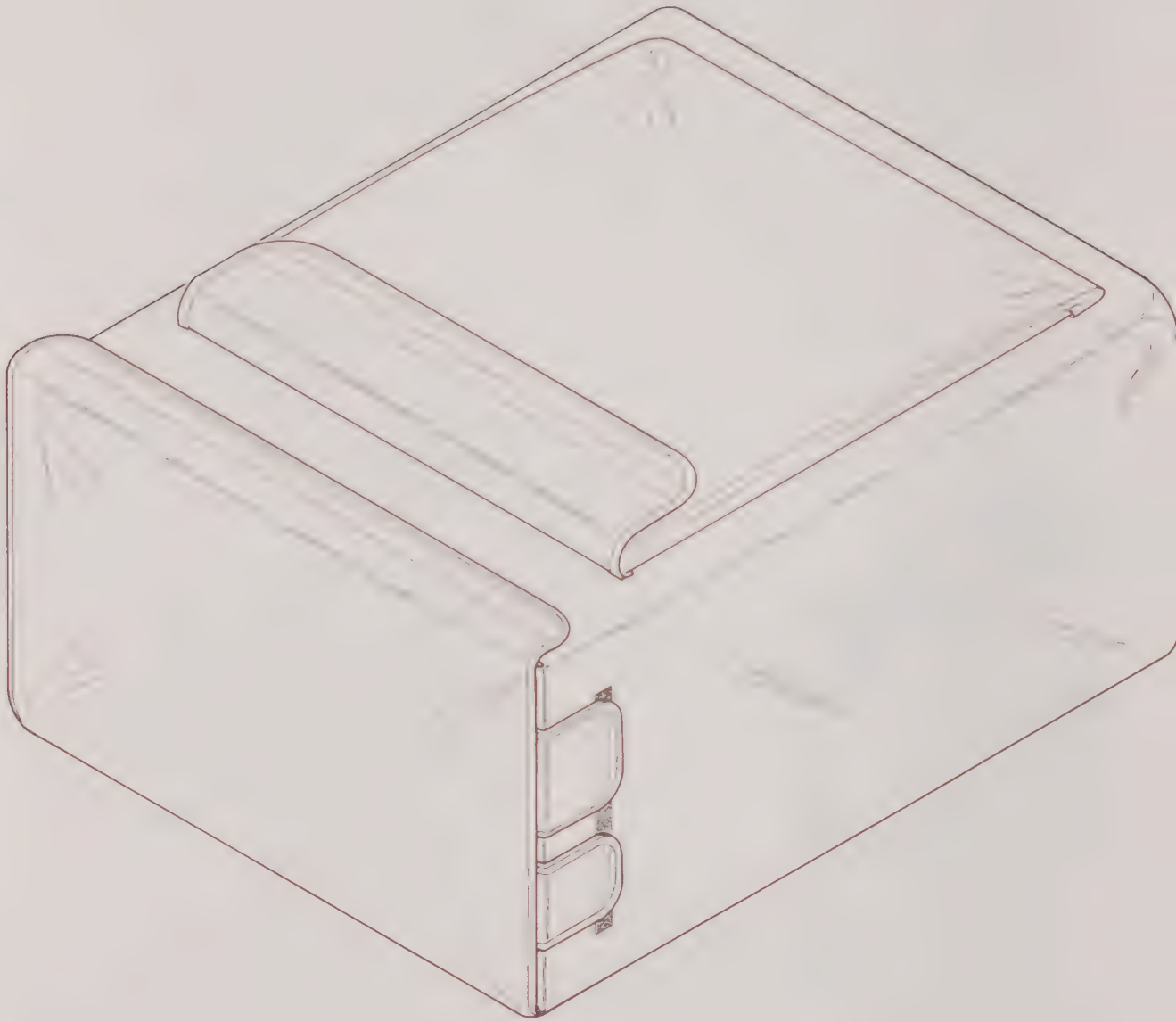


Figure G-5 Soft Padded Carrying Case (AC5004)

APPENDIX H - REPACKING FOR SHIPMENT

H-1 SHIPPING INFORMATION

IFR test sets returned to factory for calibration, service or repair must be repackaged and shipped subject to the following conditions:

Do not return any products to factory without first receiving authorization from IFR Customer Service Department.

CONTACT: Customer Service Dept.
IFR Systems, Inc.
10200 West York Street
Wichita, Kansas 67215

Telephone: (800)-835-2350
TWX: 910-741-6952

All test sets must be tagged with:

A. Owner's identification and address.
B. Nature of service or repair required.
C. Model No.
D. Serial No.

Sets must be repackaged in original shipping containers using IFR packing models. If original shipping containers and materials are not available, contact IFR Customer Service Dept. for shipping instructions.

All freight costs on non-warranty shipments are assumed by customer. (See "Warranty Packet" for freight charge policy on warranty claims.)

H-2 REPACKING PROCEDURE (Reference - Figure H-1)

A. Make sure bottom packing mold is seated on floor of shipping container.

B. Carefully wrap test set with polyethylene sheeting to protect finish.

C. Place test set into shipping container, making sure set is securely seated in bottom packing mold.

D. Place top packing mold over top of set and press down until mold rests solidly on bottom packing mold.

E. Close shipping container lids and seal with shipping tape or an industrial stapler. Tie all sides of container with break-resistant rope, twine or equivalent.

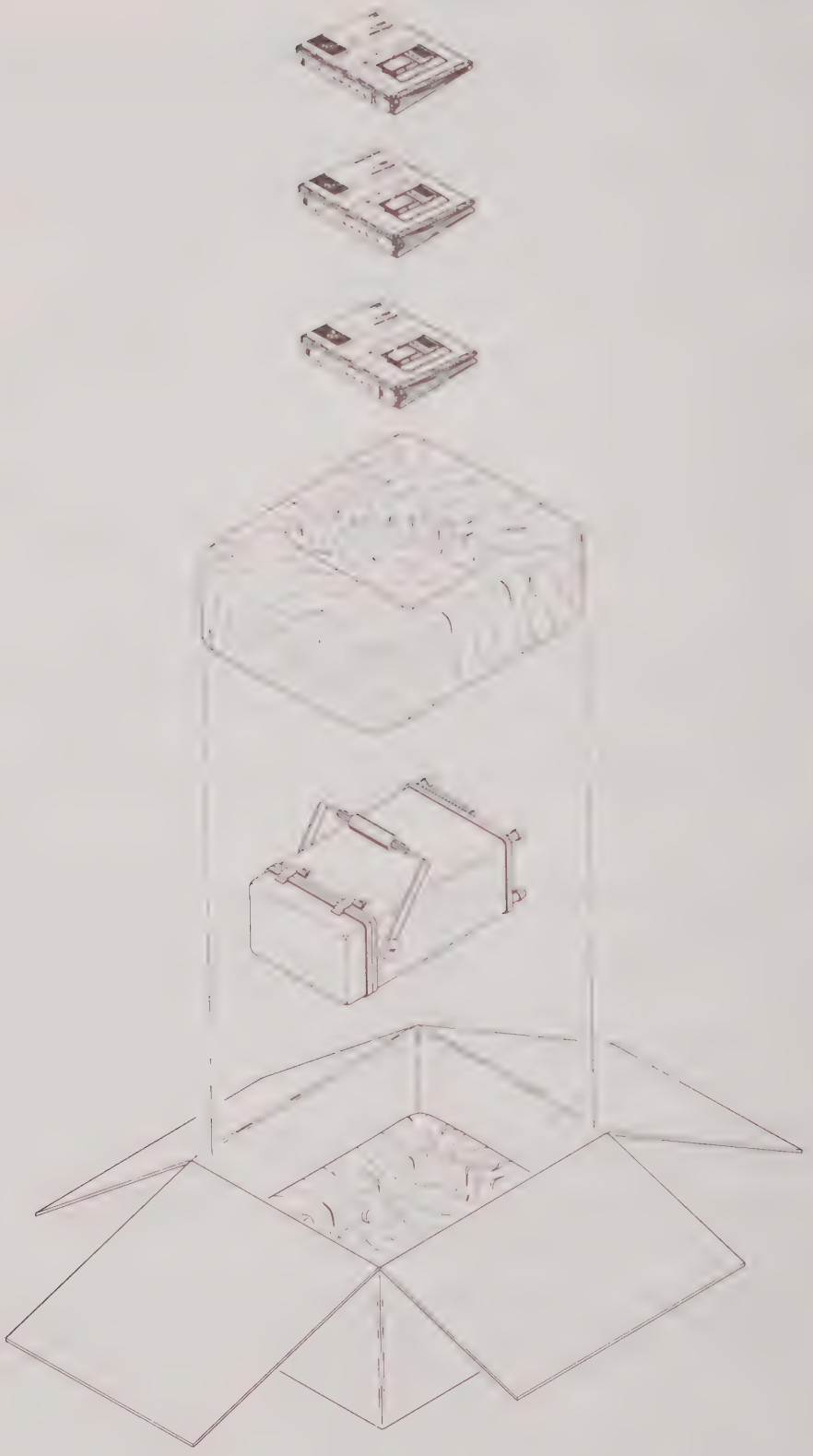


Figure H-1 Shippable A-7550 Spectrum Analyzer

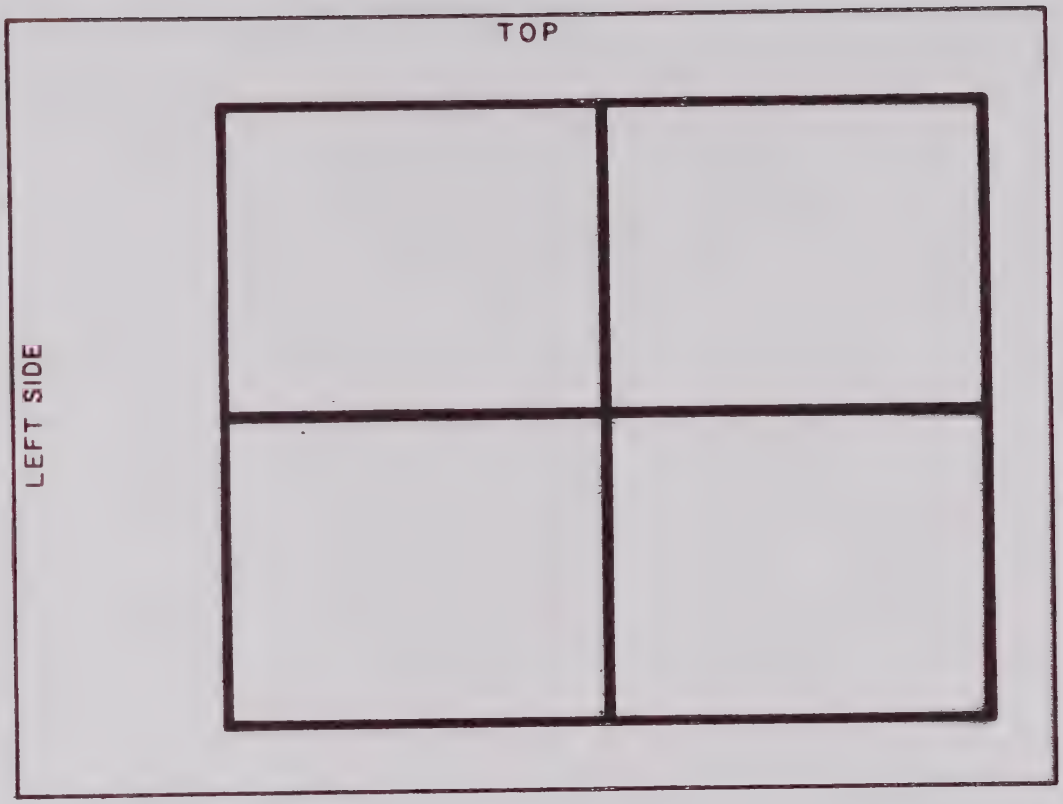


Figure 4-3 Overlay For CRT Calibration

TEMPLATE PAGE